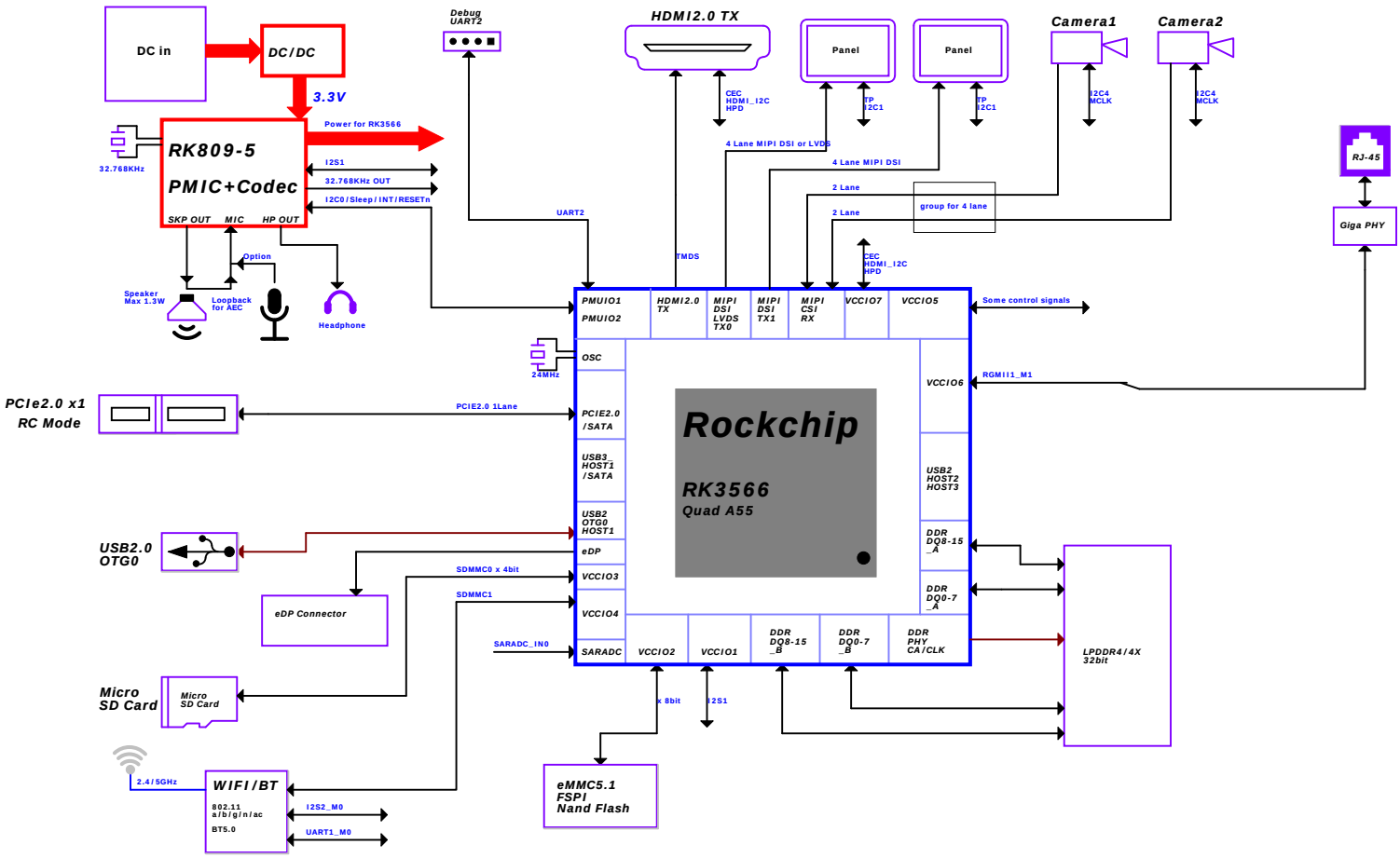
Revision History

Version	Date	By	Change Dsecription	Approved
V0.1	2020-08	Zhangdz	1: Revision preliminary version;	
V1.0	2021-07-10	Skyth	1: SOQuartz SOM production release;	
V1.0a	2021-08-16	Skyth	1: resuffle SD detected pin factor in SD boot capability	

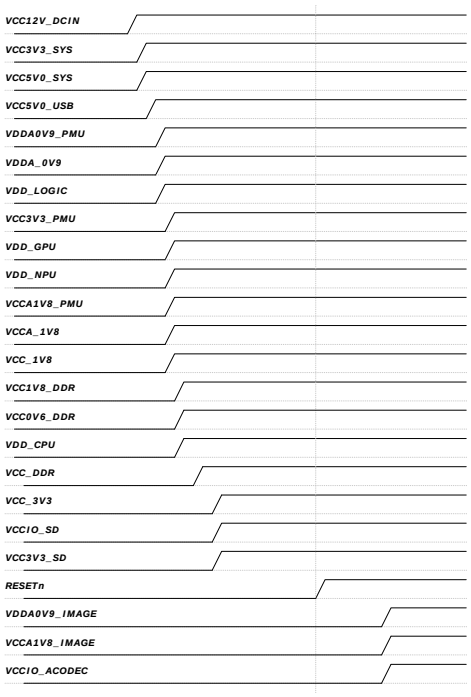
PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	01.Revision History				
Date:	Monday, August 16, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	1 of 26

RK3566 Ref Block Diagram



PINE64	PINE64
Project:	SOQuartz SOM Schematic-20210816
File:	02.Block Diagram
Date:	Monday, August 16, 2021
Rev:	V1.1
Designed by:	David.J
Reviewed by:	Default
Sheet	2 of 36

Power Sequence
&Power Path assignment



Power Source	PMIC Channel	Supply Limit	Power Supply Name	Time Slot	Default Voltage	Work Status	Sleep Status
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0.9V	OFF	OFF
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0.9V	OFF	OFF
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	OFF	OFF
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	1.8V	OFF	OFF
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF
	RK809_RESETn			Slot:4+5			
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	ON
VCC3V3_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF

IO Power Domain Map

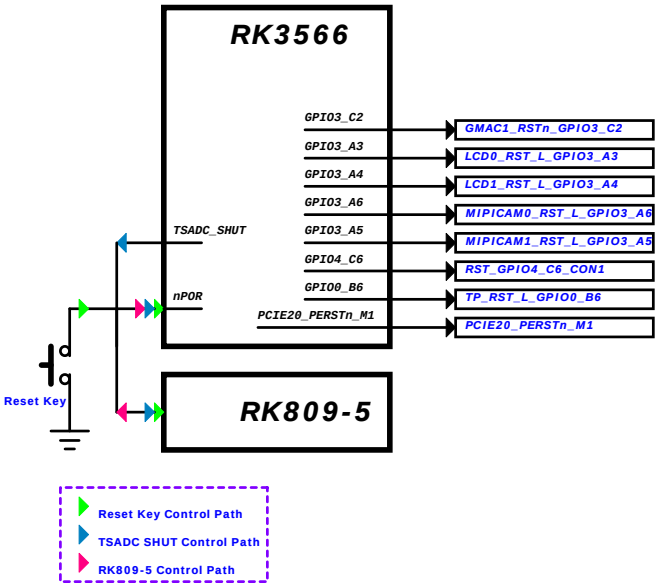
Refer to the actual design!

IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage		Voltage	Notes
		3.3V	1.8V	Supply Power Net Name	Power Source		
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO4	VCC_1V8	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_3V3	3.3V	
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC_1V8	1.8V	
VCCIO7	1N8	YES	YES	VCCIO7	VCC_3V3	3.3V	

PINE64 PINE64

Project:	SOQuartz SOM Schematic-20210816				
File:	03.Power Sequence/IO Domain Map				
Date:	Monday, August 16, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	3 of 26

RESET Signal MAP

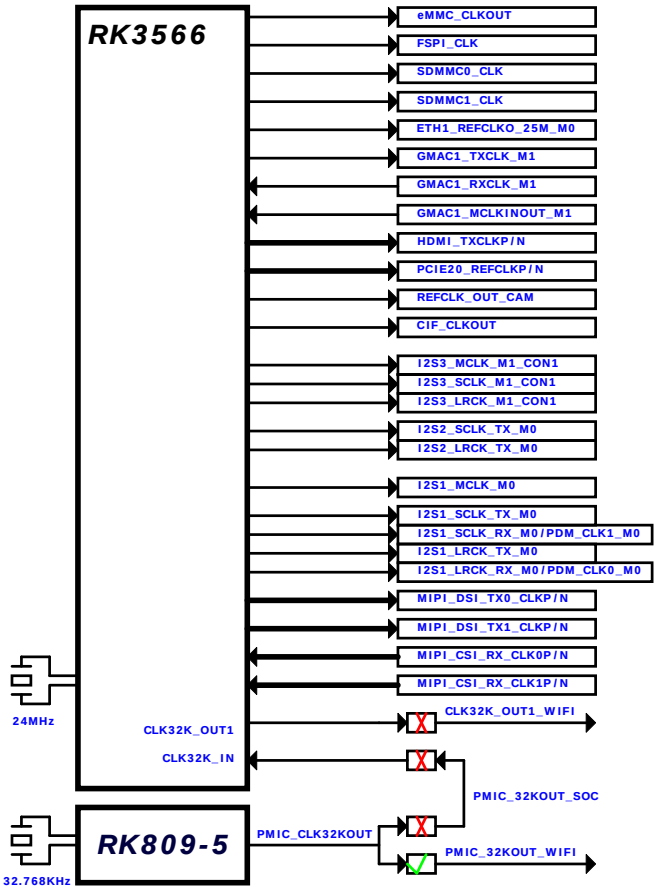


Reset Key Control Path

TSADC SHUT Control Path

RK809-5 Control Path

Clock Map

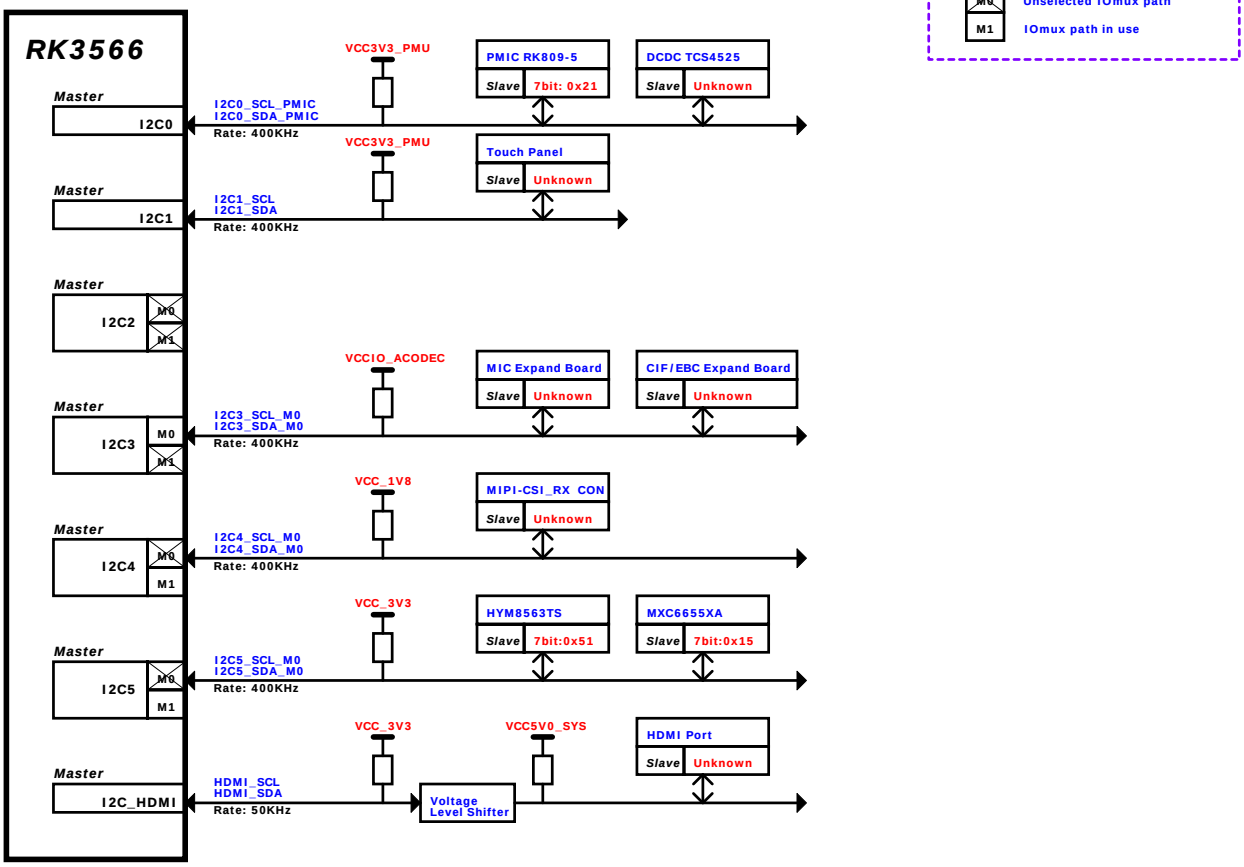


Single End

Differential

PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	04.Reset Map/Clock Map				
Date:	Monday, August 16, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	4 of 26

I2C MAP

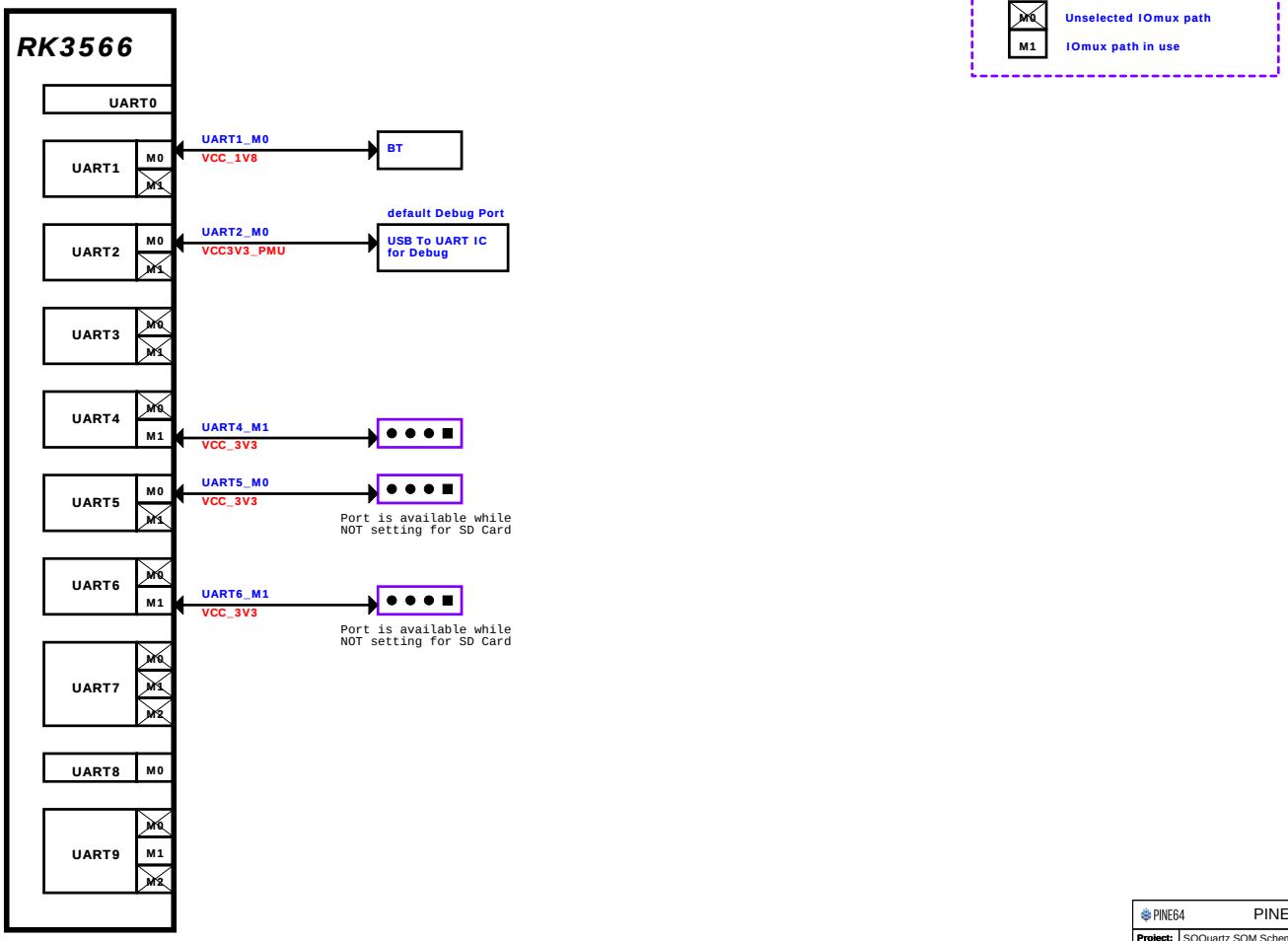


M0 Unselected IOmux path

M1 IOmux path in use

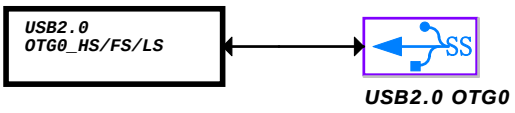
PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	05.I2C Bus Map				
Date:	Monday, August 16, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	5 of 26

UART MAP

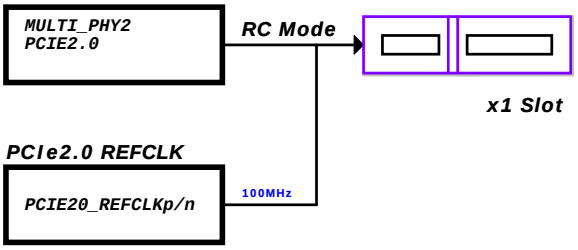


PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	06.UART Map				
Date:	Monday, August 16, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	6 of 26

USB2.0 OTG0

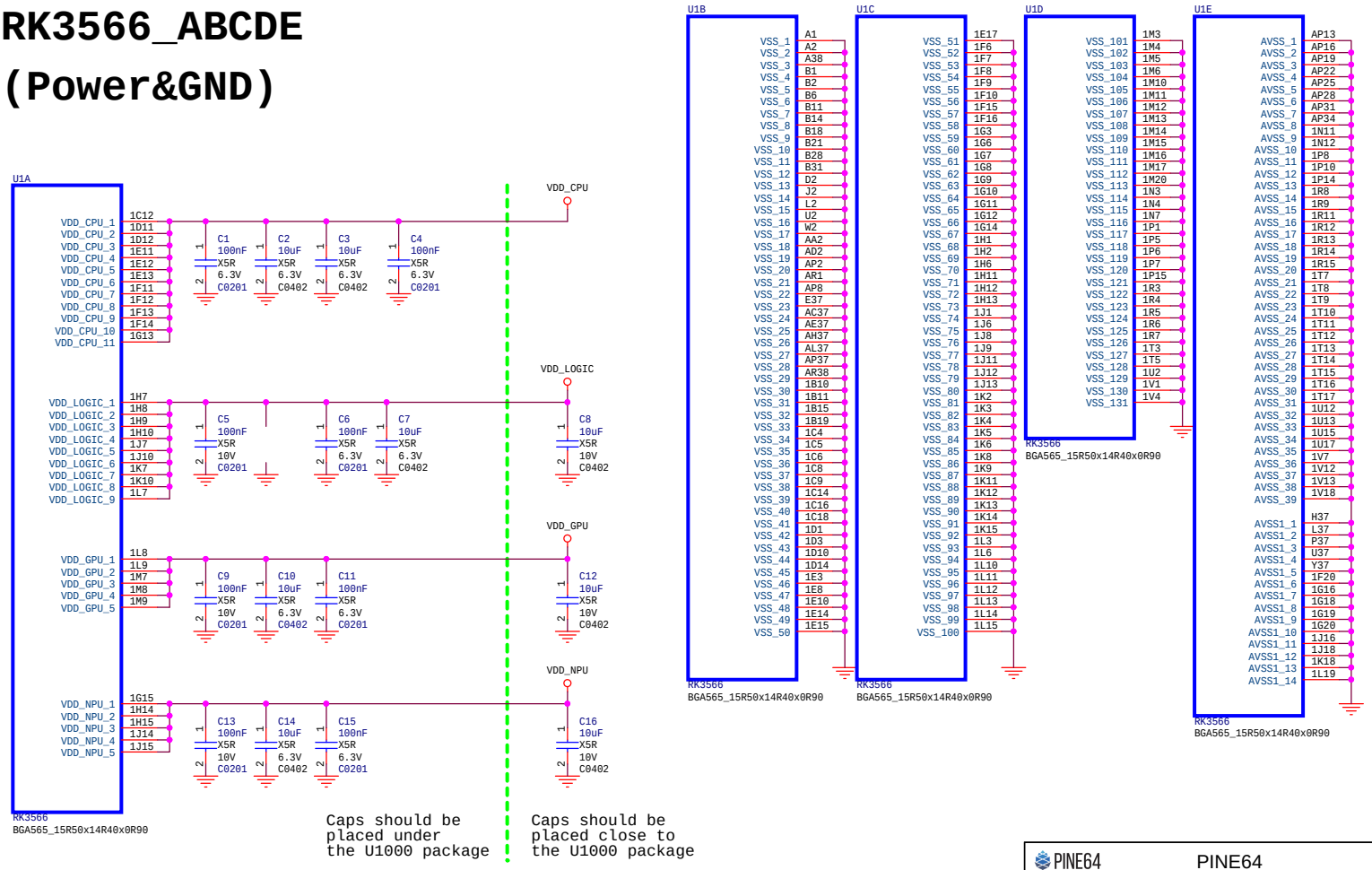


PCIE2.0 x1 Lane



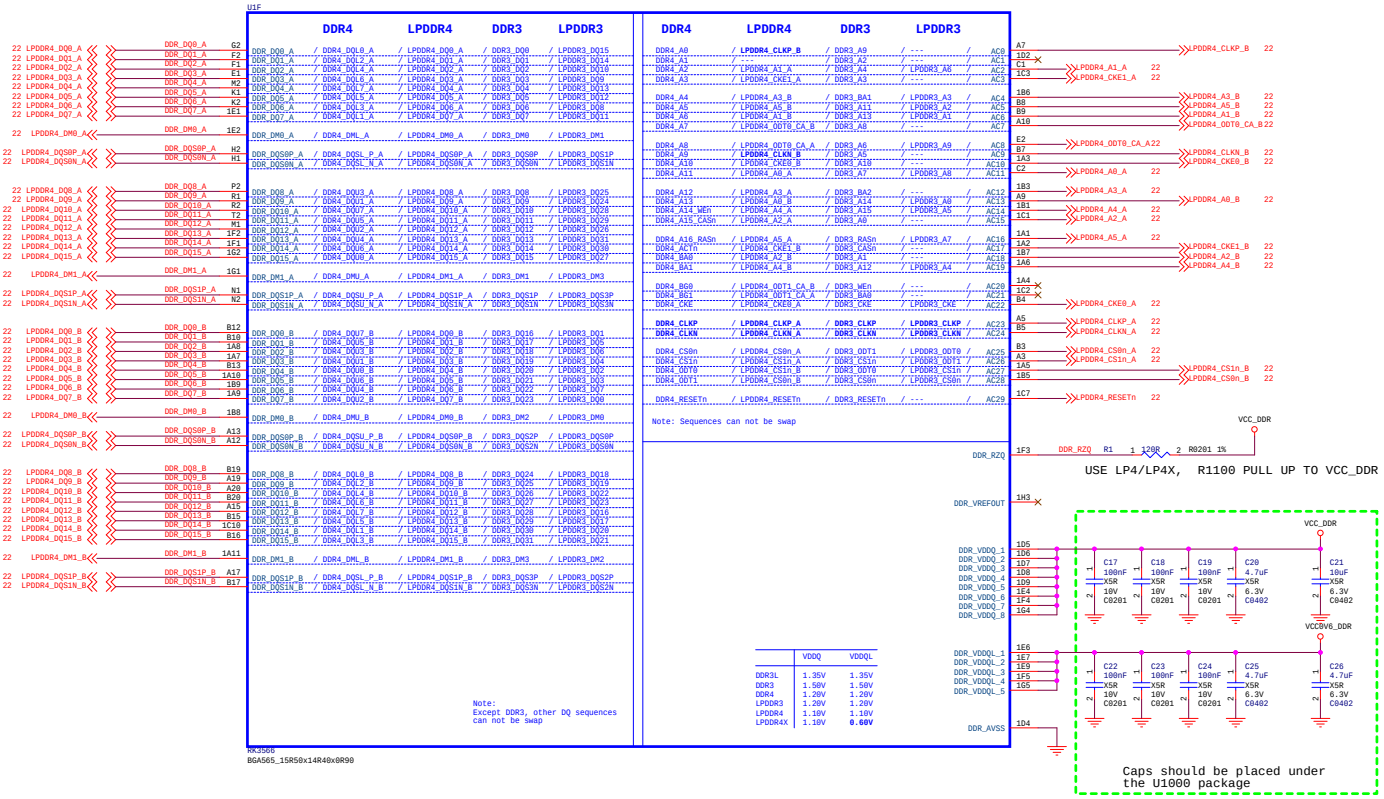
PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	07.USB/PCIE Function Map				
Date:	Monday, August 16, 2021			Rev:	V1.1
Designed by:	DanielJ	Reviewed by:	Default	Sheet:	7 of 26

RK3566_ABCDE (Power&GND)



PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	**08.RK3566_Power/GND**				
Date:	Monday, August 16, 2021			**Rev:**	V1.1
Designed by:	Daniel.J	**Reviewed by:**	Default	**Sheet:**	8 of 26

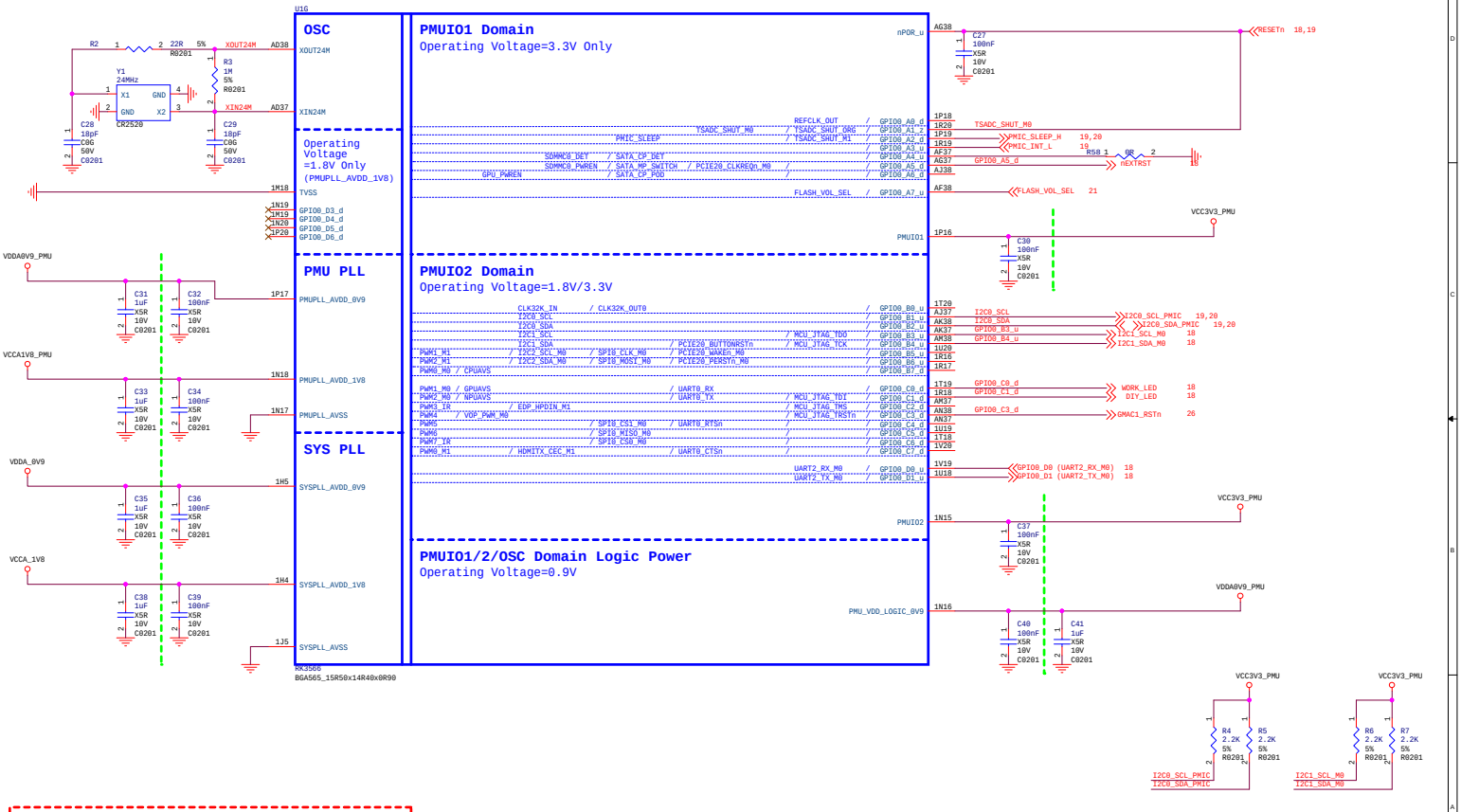
RK3566_F(DDR PHY)



	VDDQ	VDDQL
DDR3L	1.35V	1.35V
DDR3	1.50V	1.50V
DDR4	1.20V	1.20V
LPDDR3	1.20V	1.20V
LPDDR4	1.10V	1.10V
LPDDR4X	1.10V	**0.60V**

PINE64	PINE64
Project:	SOQuartz SOM Schematic-20210816
File:	**09.RK3566_DDR PHY**
Date:	Monday, August 16, 2021
Rev:	V1.1
Designed by:	Daniel.J
Reviewed by:	Default
Sheet:	9 of 26

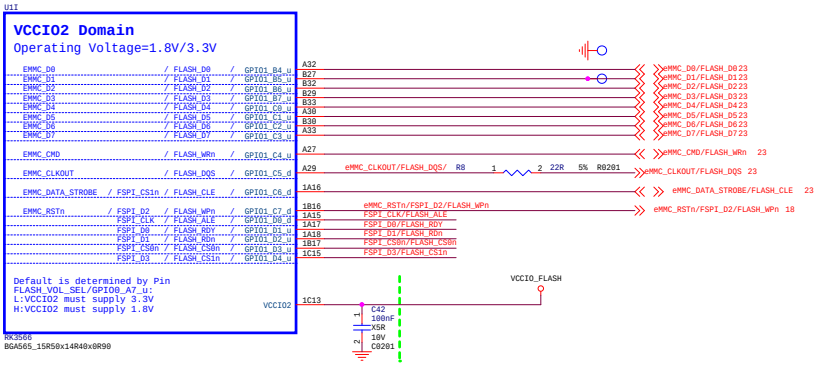
RK3566_G(OSC/PLL/PMUIO1/2)



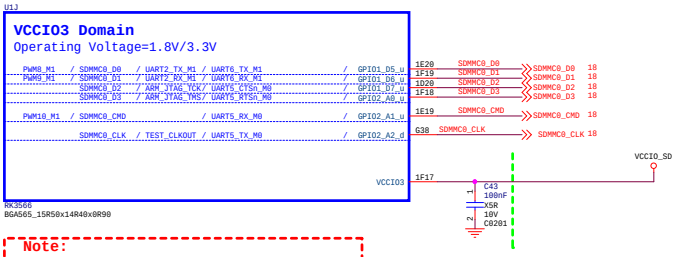
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	10.RK3566_OSC/PLL/PMUIO				
Date:	Monday, August 16, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	10 of 26

RK3566_I(VCCIO2 Domain)

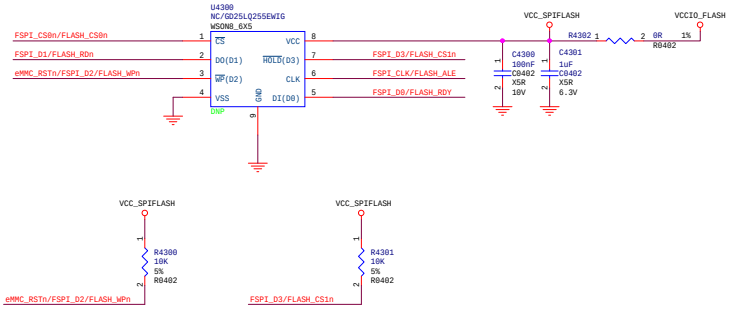


RK3566_J(VCCIO3 Domain)



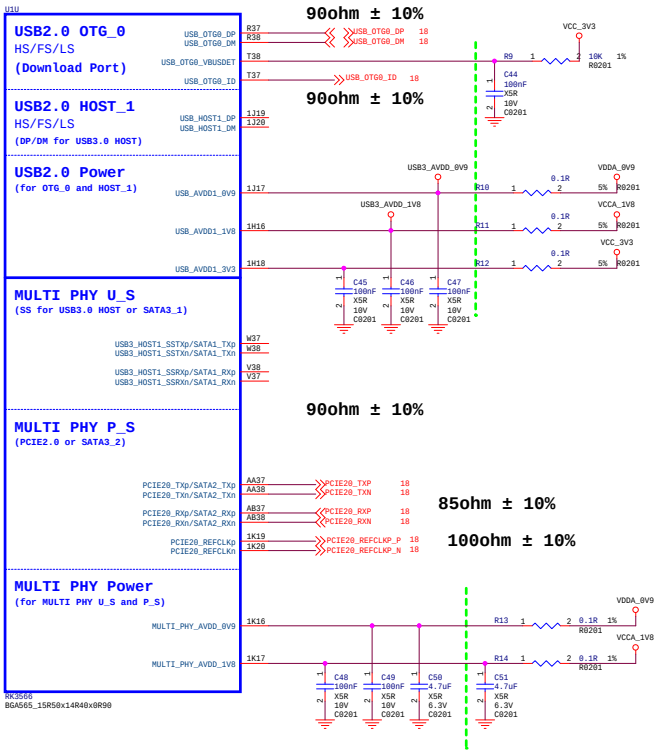
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

default VCC = 1.8V



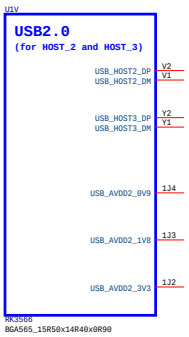
PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	**11.RK3566_Flash/SD Controller**				
Date:	Monday, August 16, 2021			**Rev:**	V1.1
Designed by:	Daniel.J	**Reviewed by:**	Default	**Sheet:**	11 of 26

RK3566_U(USB3.0/PCIe2.0 x1)



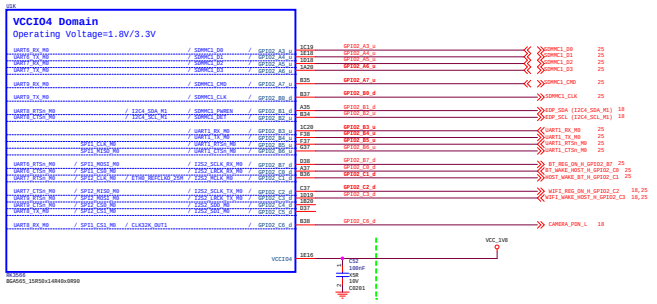
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3566_V(USB2.0 HOST)



PINE64	PINE64
Project:	SOQuartz SOM Schematic-20210816
File:	**12.RK3566_USB/PCIe PHY**
Date:	Monday, August 16, 2021 — **Rev:** V1.1
Designed by: Daniel.J — **Reviewed by:** Default — **Sheet:** 12 of 26	

RK3566_K(VCCIO4 Domain)



For WIFI

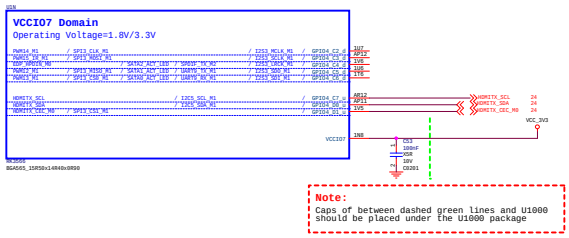
WIFI_WAKE_HOST
WIFI_REG_ON

For BT

BT_REG_ON
BT_WAKE_HOST
HOST_WAKE_BT

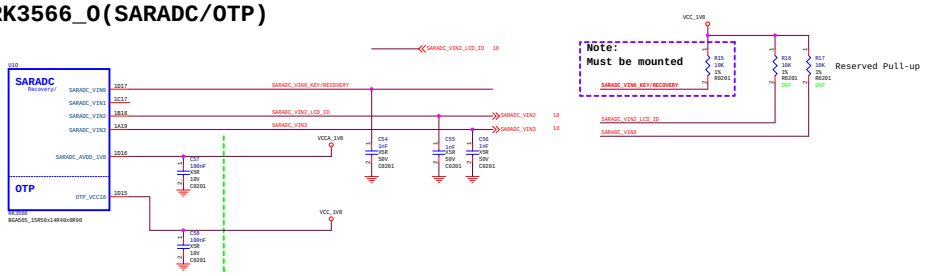
For BT

RK3566_N(VCCIO7 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3566_O(SARADC/OTP)

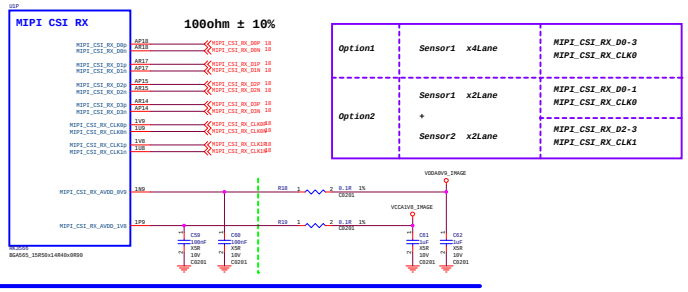


Note:
Must be mounted

Reserved Pull-up

PINE64	PINE64
Project:	SOQuartz SOM Schematic-20210816
File:	13.RK3566_SARADC&GPIO
Date:	Monday, August 09, 2021
Rev:	V1.1
Designed by:	David.J
Reviewed by:	Default
Sheet	13 of 36

RK3566_P(MIPI_CSI_RX)



CIFCLK_OUT

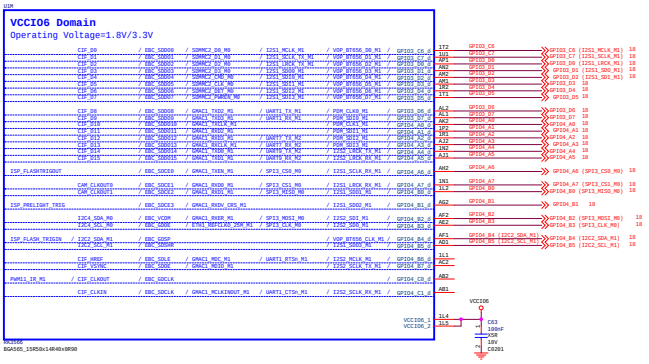
Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

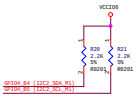
3.3V

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

Note:
Caps of between dashed green lines and U1000
Should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

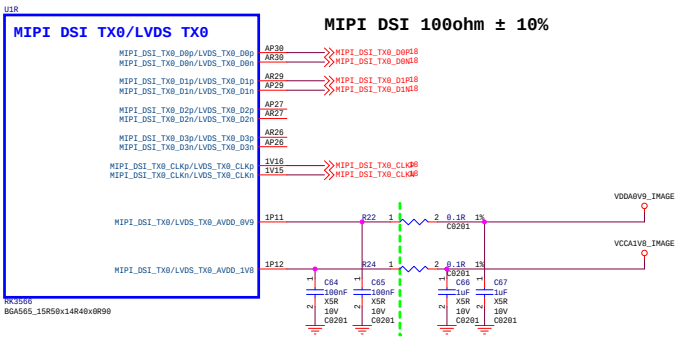
RK3566_M(VCCIO6 Domain)



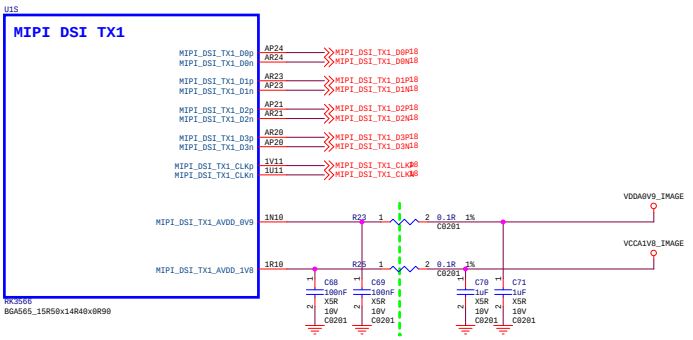


Project:	SOQuartz SOM Schematic-20210816
File:	14.RK3566_VI Interface
Date:	Monday, August 16, 2021
Rev:	V1.1
Designed by:	David.J
Reviewed by:	Default
Sheet	14 of 36

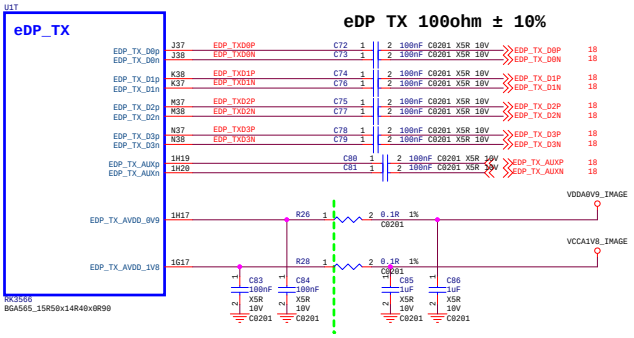
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



RK3566_S(MIPI_DSI_TX1)

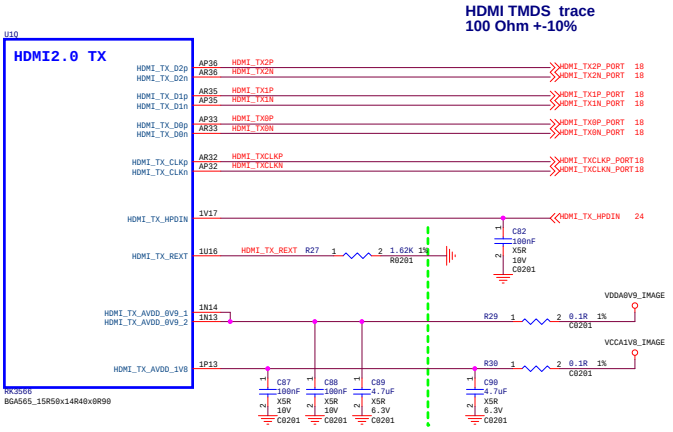


RK3566_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3566_Q(HDMI2.0 TX)



PINE64	PINE64		
Project:	SOQuartz SOM Schematic-20210816		
File:	**15.RK3566_VO Interface_1**		
Date:	Monday, August 16, 2021	**Rev:**	V1.1
Designed by:	Daniel.J	**Reviewed by:**	Default
Sheet:	15 of 26		

U1L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

	VOP_BT1120_D0 / SPI1_CS0_M1			/ SDMMC2_D0_M1 /	GPIO3_A1_d
	VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1 /	GPIO3_A2_d
	VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1 /	GPIO3_A3_d
	VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1 /	GPIO3_A4_d
	VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1 /	GPIO3_A5_d
	VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1 /	GPIO3_A6_d
	VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1 /	GPIO3_A7_d
	VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1 /	GPIO3_B0_d
PWM8_M0	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/	GPIO3_B1_d
PWM9_M0	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/	GPIO3_B2_d
	VOP_BT1120_D9 / I2C5_SCL_M0	/ GMAC1_RXDV_CRS_M0		/ PDM_SDI0_M2 /	GPIO3_B3_d
	VOP_BT1120_D10 / I2C5_SDA_M0	/ GMAC1_RXER_M0		/ PDM_SDI1_M2 /	GPIO3_B4_d
PWM10_M0	/ VOP_BT1120_D11 / I2C3_SCL_M1	/ GMAC1_TXD0_M0		/	GPIO3_B5_d
PWM11_IR_M0	/ VOP_BT1120_D12 / I2C3_SDA_M1	/ GMAC1_TXD1_M0		/	GPIO3_B6_d
PWM12_M0		/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2 /	GPIO3_B7_d
PWM13_M0		/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2 /	GPIO3_C0_d
	VOP_BT1120_D13 / SPI1_MOSI_M1		/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2 /	GPIO3_C1_d
	VOP_BT1120_D14 / SPI1_MISO_M1		/ UART5_TX_M1	/ I2S1_SDO3_M2 /	GPIO3_C2_d
	VOP_BT1120_D15 / SPI1_CLK_M1		/ UART5_RX_M1	/ I2S1_SCLK_RX_M2 /	GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2 /	GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2 /	GPIO3_C5_d

RK3566
BGA565_15R50x14R40x0R90

1U5
AR10 — GMAC1_TXD2_M1 26
AP10 — GMAC1_TXD3_M1 26
AR9 — GMAC1_RXD2_M1 26
AP9 — GMAC1_RXD3_M1 26
1U4 — GMAC1_TXCLK_M1 26
1V3 — GMAC1_RXCLK_M1 26

AR7
AP7 — GMAC1_RXD0_M1 26
AR6 — GMAC1_RXD1_M1 26
AP6 — GMAC1_RXDV_CRS_M1 26
1U3 — GMAC1_INT 26
1T4 — GMAC1_TXD0_M1 26
1V2 — GMAC1_TXD1_M1 26
AP5 — GMAC1_TXEN_M1 26

AR4 — GMAC1_MCLKINOUT_M1 26
AP4
AP3
AR2

1P3 — GMAC1_MDC_M1 26
1P4 — GMAC1_MDIO_M1 26

VCCIO5_1 1N5
VCCIO5_2 1N6
C91 100nF X5R 10V C0201
VCC_3V3
3.3V

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PINE64	PINE64
Project:	SOQuartz SOM Schematic-20210816
File:	16.RK3566_VO Interface_2
Date:	Monday, August 16, 2021
Rev:	V1.1
Designed by:	Daniel.J
Reviewed by:	Default
Sheet:	16 of 26

RK3566_H(VCCIO1 Domain)

U1H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

	/ I2C3_SDA_M0	/ UART3_RX_M0		/ AUDIOPWM_LOUT_p	/ GPIO1_A0_u
	/ I2C3_SCL_M0	/ UART3_TX_M0		/ AUDIOPWM_LOUT_n	/ GPIO1_A1_u
SCR_CLK	/ I2S1_MCLK_M0	/ UART3_RTSn_M0			/ GPIO1_A2_d
SCR_IO	/ I2S1_SCLK_TX_M0	/ UART3_CTSn_M0			/ GPIO1_A3_d
	I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0	/ GPIO1_A4_d
SCR_RST	/ I2S1_LRCK_TX_M0	/ UART4_RTSn_M0			/ GPIO1_A5_d
	I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_p	/ GPIO1_A6_d
SCR_DET	/ I2S1_SDO0_M0	/ UART4_CTSn_M0		/ AUDIOPWM_ROUT_n	/ GPIO1_A7_d
	I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ GPIO1_B0_d
	I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ GPIO1_B1_d
	I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2	/ GPIO1_B2_d
		I2S1_SDI0_M0	/ PDM_SDI0_M0		/ GPIO1_B3_d
					VCCIO1

RK3566

BGA565_15R50x14R40x0R90

A22 I2C3_SDA_M0 → GPIO1_A0 (I2C3_SDA_M0) 18

B22 I2C3_SCL_M0 → GPIO1_A1 (I2C3_SCL_M0) 18

A23

B23

1A13

B24

1A14

B25

1B13 → PCIE20_CLKREQn_3V3_L 18

A26

B26 → PCIE20_PERSTn_3V3_L 18

1B14

1D13

VCC_3V3

R31 2.2K 5% R0201

R32 2.2K 5% R0201

I2C3_SDA_M0

I2C3_SCL_M0

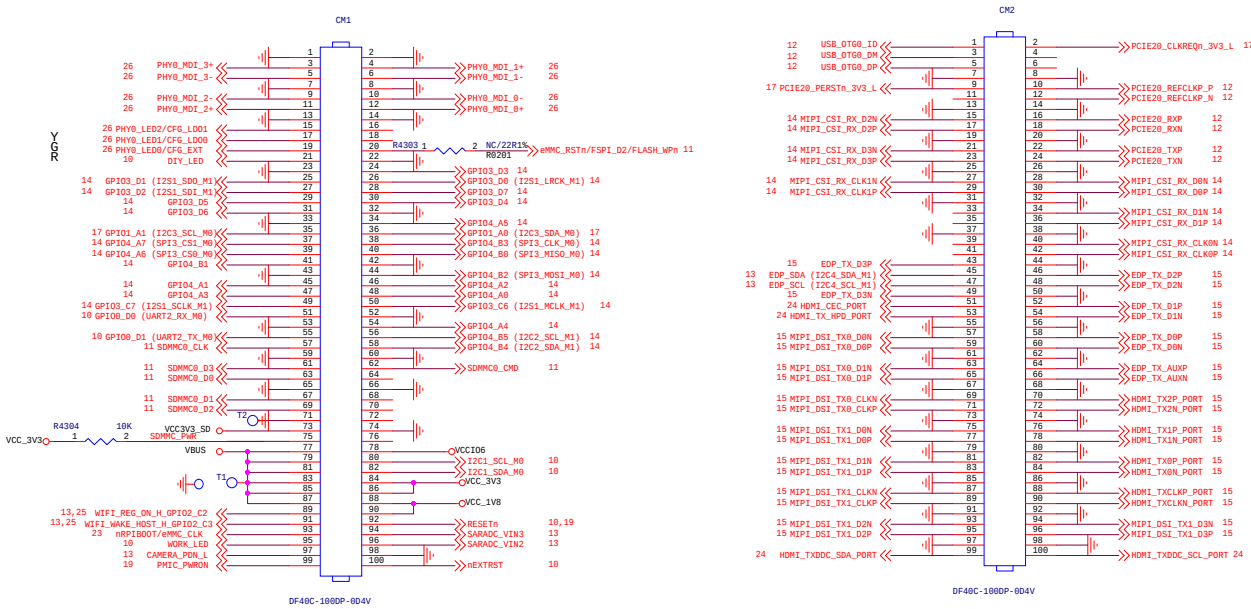
VCC_3V3

C92 100nF X5R 10V C0201

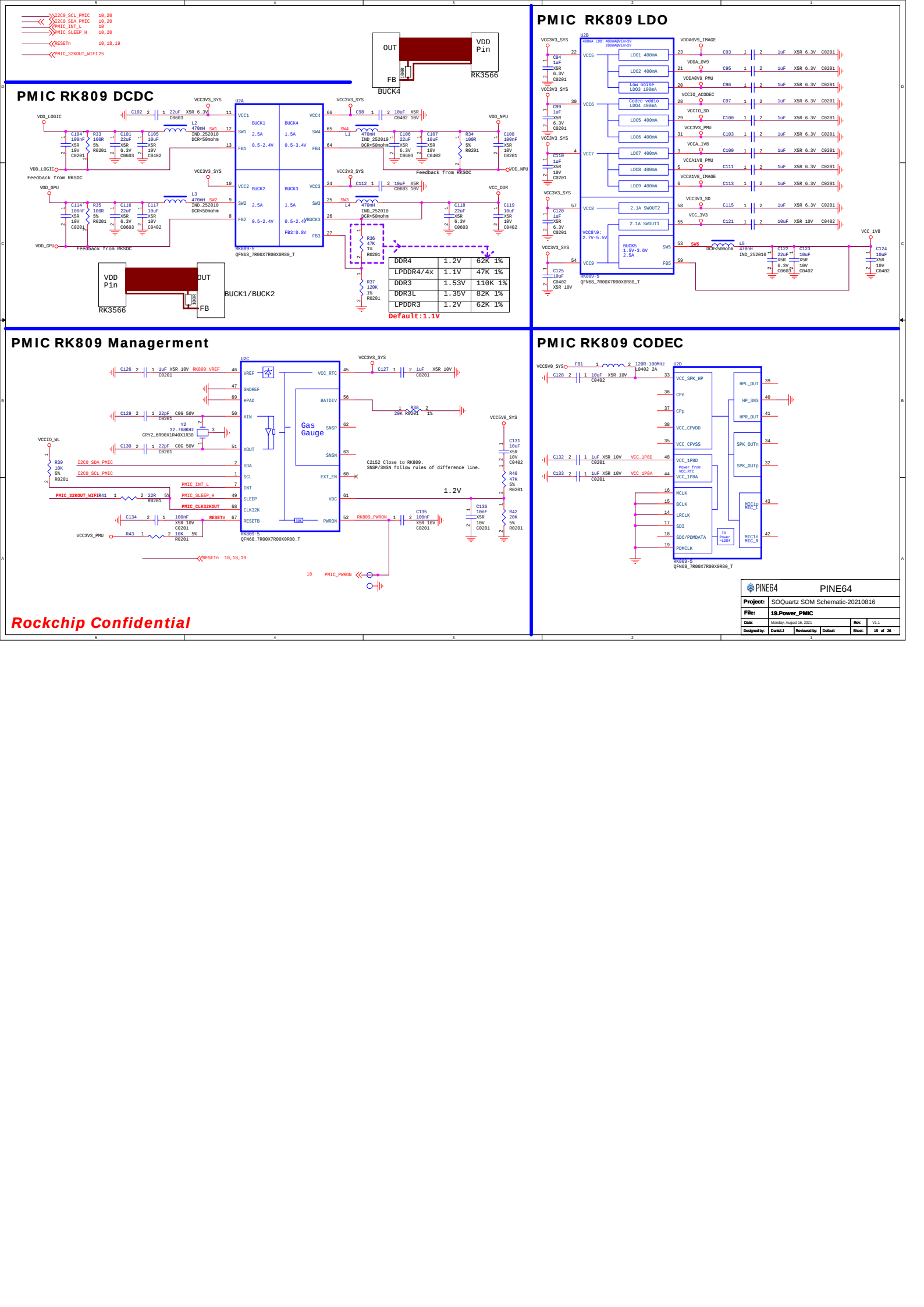
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	**17.RK3566_Audio Interface**				
Date:	Monday, August 16, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	17 of 26

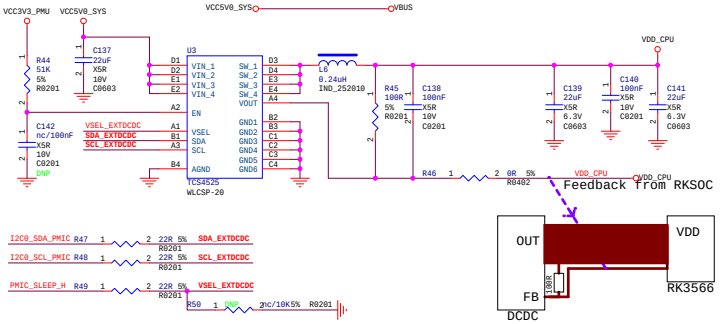


PINE64	PINE64		
Title	SOQuartz SOM Schematic-20210816		
Size: B	Document Number: Connectors		Rev: V1.1
Date: Monday, August 16, 2021	Sheet 18 of 26		

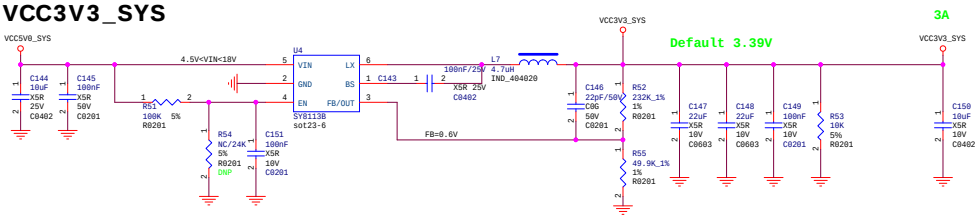

I2C0_SCL_PMIC 10,20
I2C0_SDA_PMIC 10,20
PMIC_INT_L 10
PMIC_SLEEP_H 10,20
RESETn 10,18,19
PMIC_32KOUT_WIFI 25
PMIC RK809 DCDC
VDD_LOGIC
VDD_GPU
VDD_NPU
VCC_DDR
VCC_1V8
VCCIO_WL
VCC3V3_SYS
VCC3V3_PMU
VCC5V0_SYS
U2A
U2B
U2C
U2D
BUCK1
BUCK2
BUCK3
BUCK4
2.5A
0.5-2.4V
1.5A
0.5-2.4V
0.5-2.4V
FB3=0.8V
RK809-5
QFN68_7R00X7R00X0R80_T
Feedback from RKSOC
BUCK1/BUCK2
VDD Pin
OUT
FB
RK3566
DDR4 1.2V 62K 1%
LPDDR4/4x 1.1V 47K 1%
DDR3 1.53V 110K 1%
DDR3L 1.35V 82K 1%
LPDDR3 1.2V 62K 1%
Default:1.1V
PMIC RK809 LDO
LDO1 400mA
LDO2 400mA
Low noise LDO3 100mA
Codec vddio LDO4 400mA
LDO5 400mA
LDO6 400mA
LDO7 400mA
LDO8 400mA
LDO9 400mA
2.1A SWOUT2
2.1A SWOUT1
BUCK5 1.5V-3.6V 2.5A
VDDA0V9_IMAGE
VDDA_0V9
VDDA0V9_PMU
VCCIO_ACODEC
VCCIO_SD
VCC3V3_PMU
VCCA_1V8
VCCA1V8_PMU
VCCA1V8_IMAGE
VCC3V3_SD
VCC_3V3
PMIC RK809 Managerment
Gas Gauge
Y2 32.768KHz CRY2_6R90X1R40X1R30
C2152 Close to RK809.
SNSP/SNSN follow rules of difference line.
1.2V
PMIC_PWRON
Rockchip Confidential
PMIC RK809 CODEC
VCC_SPK_HP
CPn
CPp
VCC_CPVDD
VCC_CPVSS
VCC_1P8D
VCC_1P8A
HPL_OUT
HP_SNS
HPR_OUT
SPK_OUTn
SPK_OUTp
MIC1p MIC_L
MIC1n MIC_R
MCLK
BCLK
LRCLK
SDI
SDO/PDMDATA
PDMCLK
PINE64
Project: SOQuartz SOM Schematic-20210816
File: 19.Power_PMIC
Date: Monday, August 16, 2021
Rev: V1.1
Designed by: DanielJ
Reviewed by: Default
Sheet: 19 of 26

I2C0_SCL_PMIC 10,19
I2C0_SDA_PMIC 10,19
PMIC_SLEEP_H 10,19

VDD_CPU_EXT



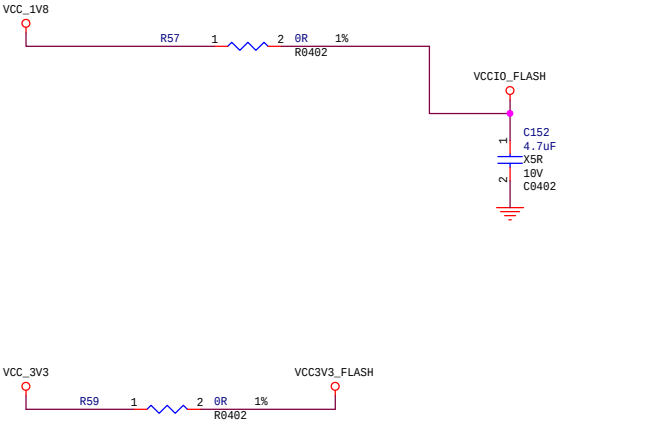
VCC3V3_SYS

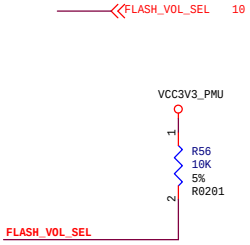


PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	**20.Power_other**				
Date:	Monday, August 16, 2021			**Rev:**	V1.1
Designed by:	DanielJ	**Reviewed by:**	Default	**Sheet:**	20 of 26

Flash Power Manage

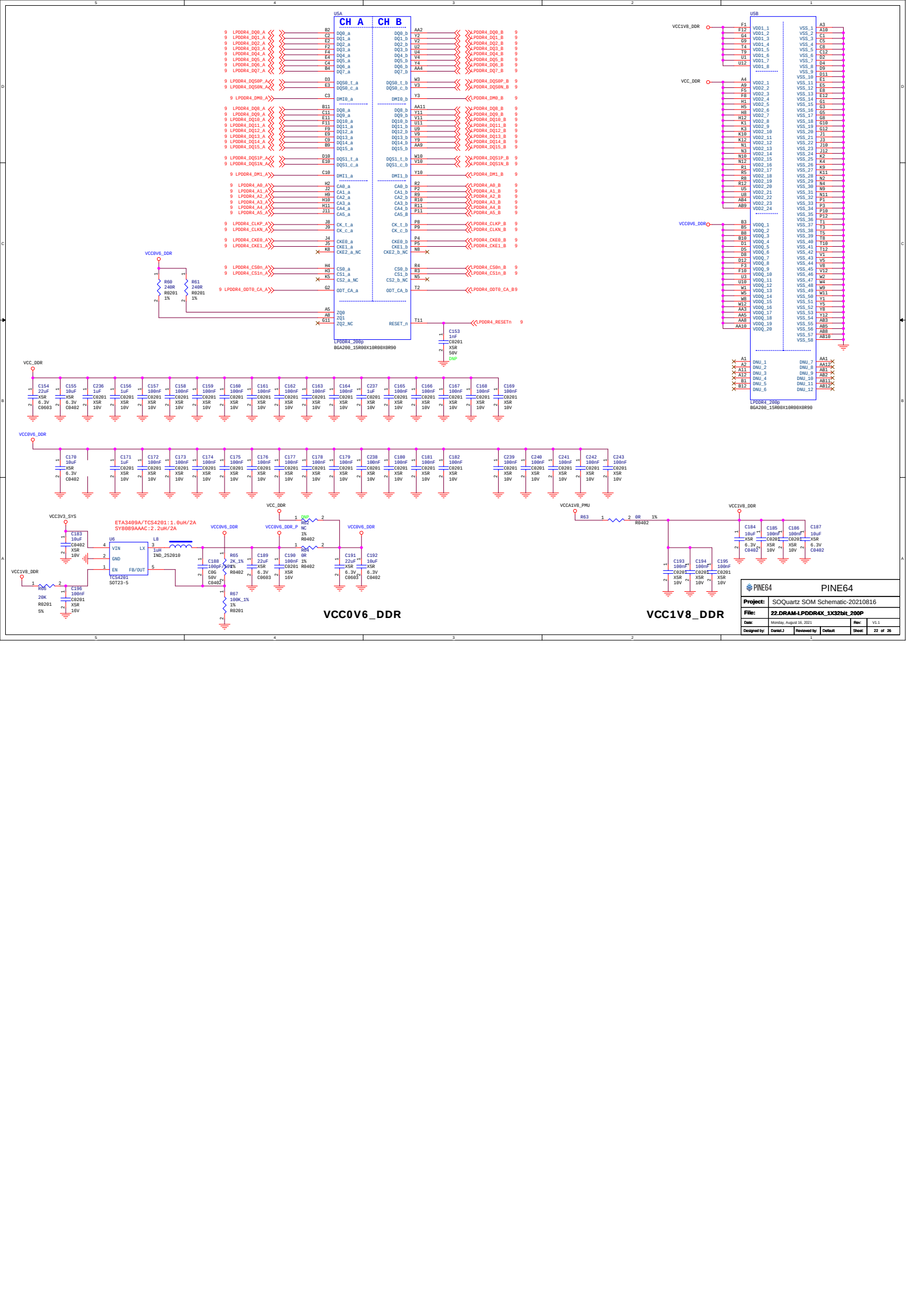
	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)

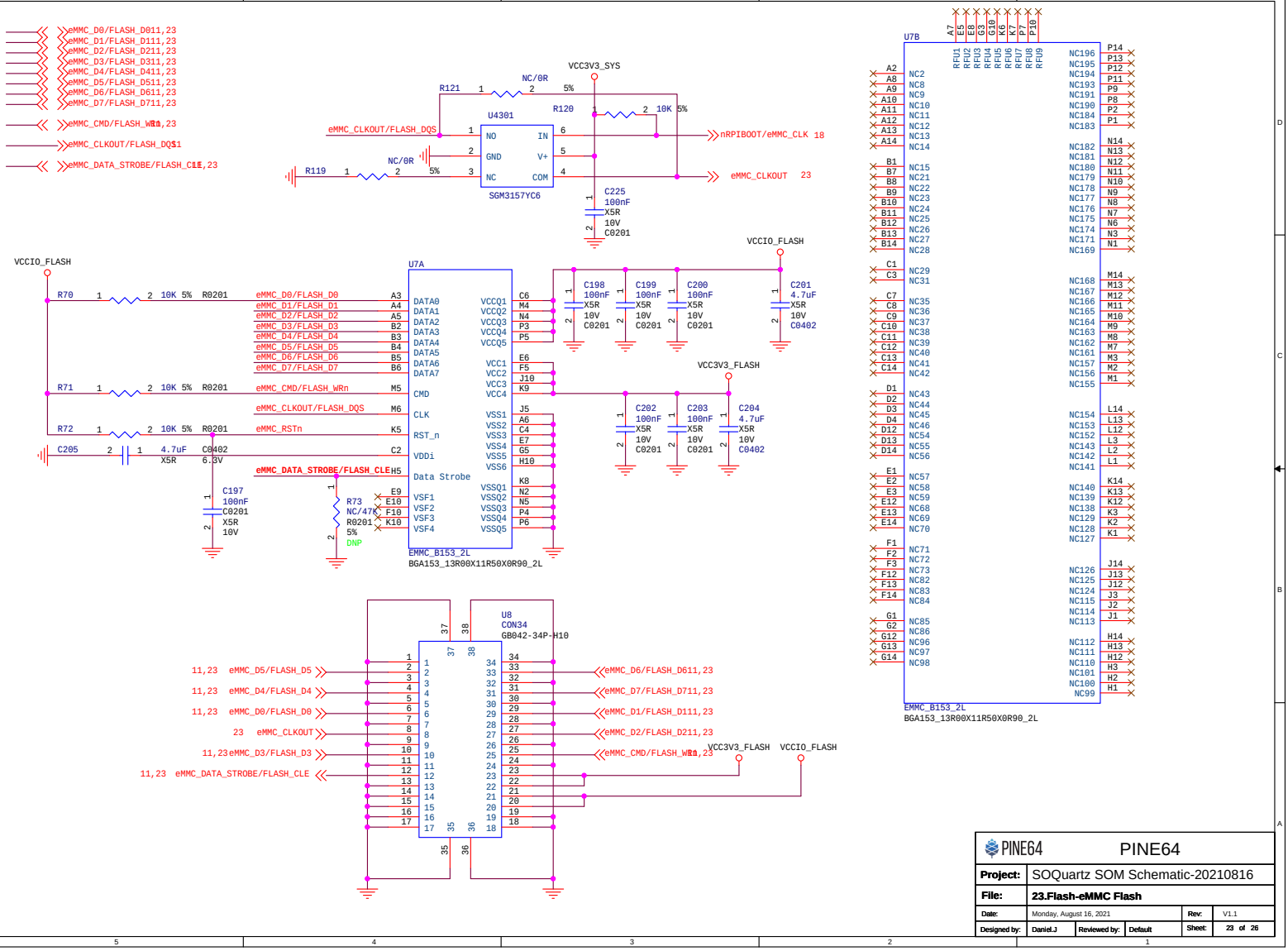




Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	21.Power_Flash Power Manage				
Date:	Monday, August 16, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	21 of 26


USA
CH A
CH B
LPDDR4_200p
BGA200_15R00X10R00X0R90
USB
LPDDR4_200p
BGA200_15R00X10R00X0R90
VCC0V6_DDR
VCC1V8_DDR
VCC_DDR
VCC3V3_SYS
VCCA1V8_PMU
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
TCS4201
SOT23-5
IND_252010
PINE64
Project: SOQuartz SOM Schematic-20210816
File: 22.DRAM-LPDDR4X_1X32bit_200P
Date: Monday, August 16, 2021
Rev: V1.1
Designed by: Daniel.J
Reviewed by: Default
Sheet: 22 of 26



PINE64	PINE64		
Project:	SOQuartz SOM Schematic-20210816		
File:	**23.Flash-eMMC Flash**		
Date:	Monday, August 16, 2021	**Rev:**	V1.1
Designed by:	Daniel.J	**Reviewed by:** Default	**Sheet:** 23 of 26

HDMI_TX2P_PORT 15,18
HDMI_TX2N_PORT 15,18

HDMI_TX1P_PORT 15,18
HDMI_TX1N_PORT 15,18

HDMI_TX0P_PORT 15,18
HDMI_TX0N_PORT 15,18

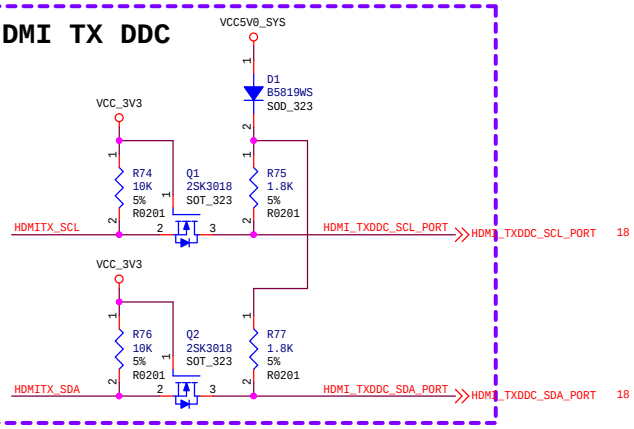
HDMI_TXCLKP_PORT 15,18
HDMI_TXCLKN_PORT 15,18

HDMITX_SCL 13
HDMITX_SDA 13

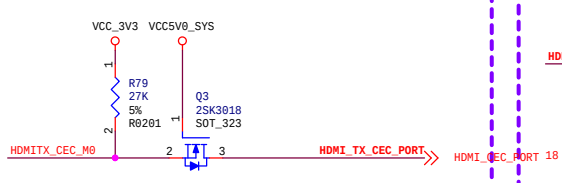
HDMITX_CEC_M0 13

HDMI_TX_HPDIN 15

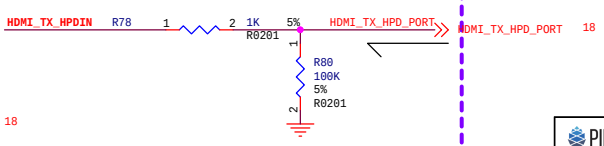
HDMI TX DDC



HDMI TX CEC

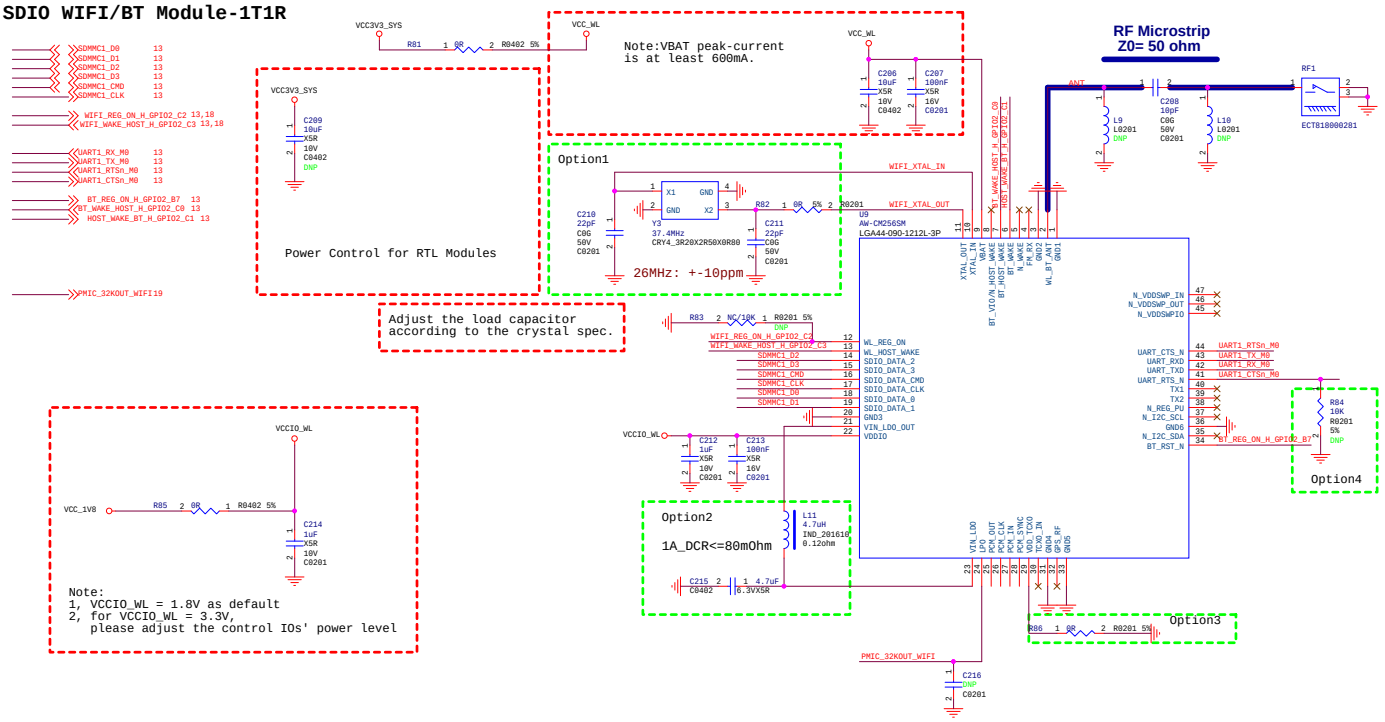


HDMI TX HPD



PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	**24.VO-HDMI2.0 TX**				
Date:	Monday, August 16, 2021			**Rev:**	V1.1
Designed by:	Zhangdz	**Reviewed by:**	Default	**Sheet:**	24 of 26

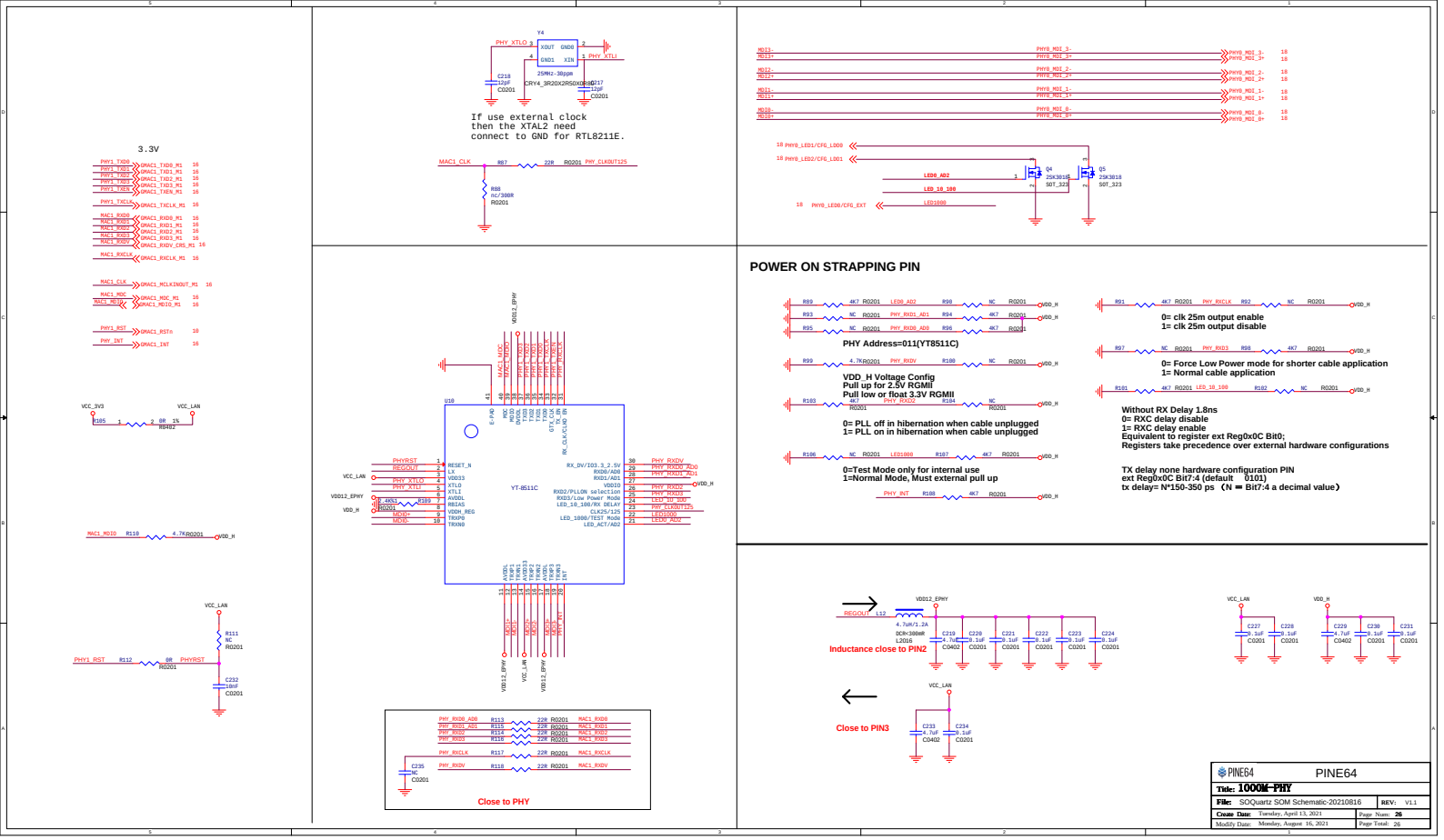
SDIO WIFI/BT Module-1T1R



Note:
1, VCCIO_WL = 1.8V as default
2, for VCCIO_WL = 3.3V,
please adjust the control IOs' power level

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

PINE64	PINE64				
Project:	SOQuartz SOM Schematic-20210816				
File:	25.WIFI/BT-SDIO_1T1R+UART				
Date:	Monday, August 16, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	25 of 26



PINE64	PINE64
Title:	1000M PHY
File:	SOQuartz SOM Schematic-20210816
REV:	V1.1
Create Date:	Tuesday, April 13, 2021
Page Num:	28
Modify Date:	Monday, August 16, 2021
Page Total:	28