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</table>

### Notes

**NOTE 1:**

Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

**NOTE 2:**

Please use our recommended components to avoid too many changes.
For more informations about the second source, please refer to our AVL.
## Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>By</th>
<th>Description</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0a</td>
<td>2020/12/15</td>
<td>skyth-tech</td>
<td>Model A SBC Released</td>
<td></td>
</tr>
<tr>
<td>2.0</td>
<td>2021/04/27</td>
<td>skyth-tech</td>
<td>Production board version</td>
<td></td>
</tr>
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</table>
Power Sequence
& Power Path assignment

**Power Sequence**

- **VDDA0V9_PMU**
- **VDDA_0V9**
- **VDD_LOGIC**
- **VCC3V2_PMU**
- **VCCA1V8_PMU**
- **VDD_CPU**
- **VCCV8_DDR**
- **VCCV32_DDR**
- **VCCIO_SD**
- **VCCIO_ACODEC**
- **VCC1V8_DVP**
- **VCC5V_MIDU**
- **VCC_SYS**
- **VCC_BAT**

**Power Path assignment**

- **VDDA0V9_PMU**
- **VDDA_0V9**
- **VDD_LOGIC**
- **VCC3V2_PMU**
- **VCCA1V8_PMU**
- **VDD_CPU**
- **VCCV8_DDR**
- **VCCV32_DDR**
- **VCCIO_SD**
- **VCCIO_ACODEC**
- **VCC1V8_DVP**
- **VCC5V_MIDU**
- **VCC_SYS**
- **VCC_BAT**

**IO Power Domain Map**

<table>
<thead>
<tr>
<th>IO Domain</th>
<th>Pin Num</th>
<th>Support IO Voltage</th>
<th>Assignment IO Domain Voltage</th>
<th>Supply Power Net Name</th>
<th>Power Source</th>
<th>Voltage</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU01</td>
<td>1P16</td>
<td>YES</td>
<td>NO</td>
<td>VCC3V3_PMU</td>
<td>VCC3V3_PMU</td>
<td>3.3V</td>
<td></td>
</tr>
<tr>
<td>PMU02</td>
<td>1N15</td>
<td>YES</td>
<td>YES</td>
<td>VCC3V3_PMU</td>
<td>VCC3V3_PMU</td>
<td>3.3V</td>
<td></td>
</tr>
<tr>
<td>PMU01</td>
<td>1D13</td>
<td>YES</td>
<td>YES</td>
<td>VCCIO_ACODEC</td>
<td>VCCIO_ACODEC</td>
<td>3.3V</td>
<td></td>
</tr>
<tr>
<td>VCC02</td>
<td>1C13</td>
<td>YES</td>
<td>YES</td>
<td>VCCIO_FLASH</td>
<td>VCC1V8</td>
<td>1.8V</td>
<td>FLASH_VOL_SEL = 1 --&gt; VCCIO_FLASH = 1.8V</td>
</tr>
<tr>
<td>VCC03</td>
<td>1F17</td>
<td>YES</td>
<td>YES</td>
<td>VCCIO_SD</td>
<td>VCCIO_SD</td>
<td>3.3V</td>
<td></td>
</tr>
<tr>
<td>VCC04</td>
<td>1E16</td>
<td>YES</td>
<td>YES</td>
<td>VCC1V8_PMU</td>
<td>VCC1V8_PMU</td>
<td>1.8V</td>
<td></td>
</tr>
<tr>
<td>VCC05</td>
<td>1N5 1N6</td>
<td>YES</td>
<td>YES</td>
<td>VCCIO5</td>
<td>VCC1V8</td>
<td>1.8V</td>
<td></td>
</tr>
<tr>
<td>VCC06</td>
<td>1L4 1L5</td>
<td>YES</td>
<td>YES</td>
<td>VCCIO6</td>
<td>VCCIO_DVP</td>
<td>1.8V</td>
<td></td>
</tr>
<tr>
<td>VCC07</td>
<td>1N8</td>
<td>YES</td>
<td>YES</td>
<td>VCCIO7</td>
<td>VCC3V3</td>
<td>3.3V</td>
<td></td>
</tr>
</tbody>
</table>
UART MAP

RK3566

UART0

UART1 M0
VCC_1V8

UART1_M0

BT

UART2 M0
VCC3V3_PMU

UART2_M0

default Debug Port

Debug

UART3

UART4 M1

UART5 M0

UART6 M1

UART7

UART8 M0

UART9 M1

Unselected IOMUX path
IOMUX path in use

VCC3V3_PMU

Default Debug Port

Wednesday, November 25, 2020
Daniel.J 89 9Default

Project: Quartz64 Model A Schematic 20210427
File: UART Map

Design by: [Name]
Revision: [Revision Number]
Sheet: 1 of 10
Caps should be placed close to the U1000 package

Caps should be placed under the U1000 package

RK3566_ABCDE
(Power&GND)
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package.
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
**Note:**
- Capacitors of between dashed green lines and U1000 should be placed under the U1000 package.
- Other caps should be placed close to the U1000 package.
**RK3566_R (MIPI_DSI_TX0/LVDS_TX0)**

**RK3566_S (MIPI_DSI_TX1)**

**RK3566_T (eDP/DP TX)**

**RK3566_Q (HDMI2.0 TX)**

Redoed capacitors should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

**Note:**
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.
VCCIO5 Domain
Operating Voltage=1.8V/3.3V

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
RK3566_H (VCCIO1 Domain)

VCCIO1 Domain
Operating Voltage=1.8V/3.3V

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
## Flash Power Manage

<table>
<thead>
<tr>
<th>Component</th>
<th>Voltage Requirement</th>
<th>Default Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>eMMC</td>
<td>1.8V</td>
<td><code>FLASH_VOL_SEL --&gt; Logic=H</code></td>
</tr>
<tr>
<td>Nand flash</td>
<td>Default 3.3V, Adjust according to demand 1.8V</td>
<td><code>FLASH_VOL_SEL --&gt; Logic=L (Default)</code></td>
</tr>
<tr>
<td>SPI flash</td>
<td>Default 3.3V, Adjust according to demand 1.8V</td>
<td><code>FLASH_VOL_SEL --&gt; Logic=L (Default)</code></td>
</tr>
</tbody>
</table>

Note: `FLASH_VOL_SEL` state decided to VCCIO2 domain IO driven by default

Logic = L: 3.3V IO driven
Logic = H: 1.8V IO driven

---

### Schematic

- **VCCIO2 domain voltage**: Recommend voltage value (VCCIO_FLASH)
- **FLASH_VOL_SEL**
  - Logic = L (Default)
  - Logic = H

---

**Diagram Elements**

- **C2300**: 1uF, 6.3V, C0402
- **C2301**: 4.7uF, 10V, C0603
- **C2302**: DNP, C0402
- **R2301**: 10K, R0402
- **R2302**: 0Ω, NC/4.7K
- **R2303**: 0Ω, NC/4.7K
- **U2300**: NC/RT9193-18GB, SOT_23_5
- **GND**, **IN1**, **EN3**, **BP 4**, **OUT 5**

---

**Note:**

FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default

Logic = L: 3.3V IO driven
Logic = H: 1.8V IO driven
**Project:** Quartz64 Model-A Schematic 20210427

**File:** E-Ink Interface

**Date:** Wednesday, November 25, 2020

**Rev:** V2.0

**Designed by:** ZHM

**Reviewed by:** <Checker>

**Sheet:** 24 of 33
主要 SATA 串口硬盘接口。

<table>
<thead>
<tr>
<th>PIN</th>
<th>SIGNAL</th>
<th>PIN</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>2</td>
<td>TXP</td>
</tr>
<tr>
<td>3</td>
<td>TXN</td>
<td>4</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>RXN</td>
<td>6</td>
<td>RXP</td>
</tr>
</tbody>
</table>

Note: USB3.0信号的ESD不能随便换掉
如需换那么必须选择相同的规格。

Cj<=0.4pF
default VCC = 1.8V
Quartz64 Model-A Schematic 20210427
Touch Panel connector

- VCC_3V3
- R5304
- VCC_TP
- OR
- R0402
- 5%
- TP_INT_L
- TP_RST_L
- I2C2_SDA_M0 38
- I2C2_SCL_M0 38

Components:
- C453: 4.7uF
- C454: 0.1uF
- C0603
- C0402
- R5304
- 0R
- 0.1uF
- 0.1uF

Quartz64 Model-A Schematic 20210427

PINE64

Title: Quartz64 Model-A Schematic 20210427

Size: A

Document Number: TP PORT

Rev: V2.0

Date: Sheet 34 of
If use external clock, then the XTAL2 need connect to GND for RTL8211E.

VCC_LAN

PHYS0_MDI_0+

If use external clock, then the XTAL2 need connect to GND for RTL8211E.

VCC_LAN

PHYS0_MDI_0+

If use external clock, then the XTAL2 need connect to GND for RTL8211E.

VCC_LAN

PHYS0_MDI_0+

If use external clock, then the XTAL2 need connect to GND for RTL8211E.

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If use external clock, then the XTAL2 need connect to GND for RTL8211E.

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If use external clock, then the XTAL2 need connect to GND for RTL8211E.

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VCC_LAN

PHYS0_MDI_0+

If use external clock, then the XTAL2 need connect to GND for RTL8211E.

VCC_LAN

PHYS0_MDI_0+
Note:
Reserve PAD for Update.
MicroSD Card

Close to MicroSD Card
Cj<=0.4pF
SDIO WIFI/BT Module-1T1R

Note:
- VBAT voltage range: 3.0V~4.8V
- Supply current at least 400mA
Heatsink

When use socket, NO Heatsink holes is reserved.