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Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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Revision History

Version	Date	By	Description	Remark
1.0a	2020/12/15	skyth-tech	Model A SBC Released	
2.0	2021/04/27	skyth-tech	Production board version	

PINE64	PINE64				
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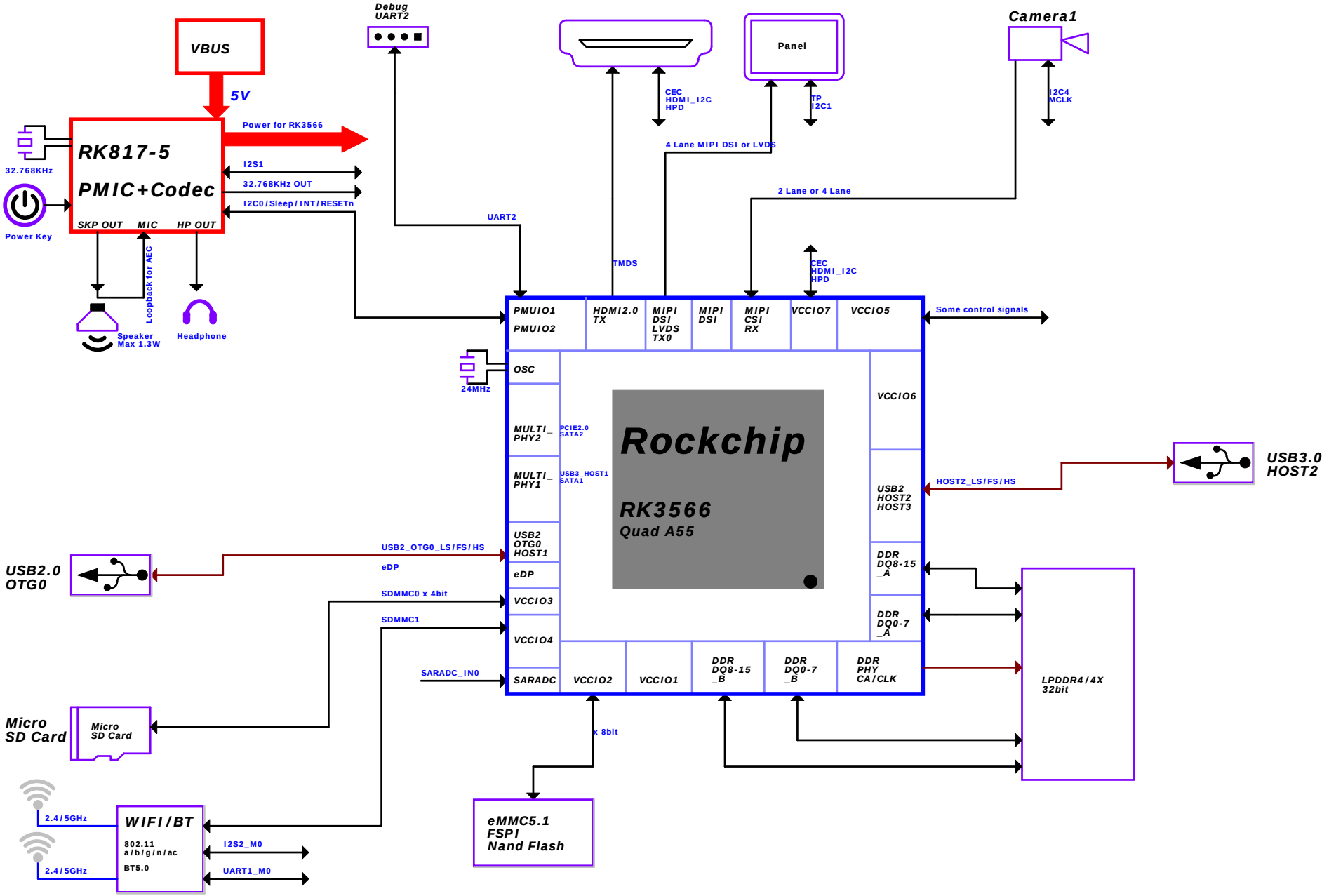
RK3566 Ref Block Diagram



PINE64	PINE64
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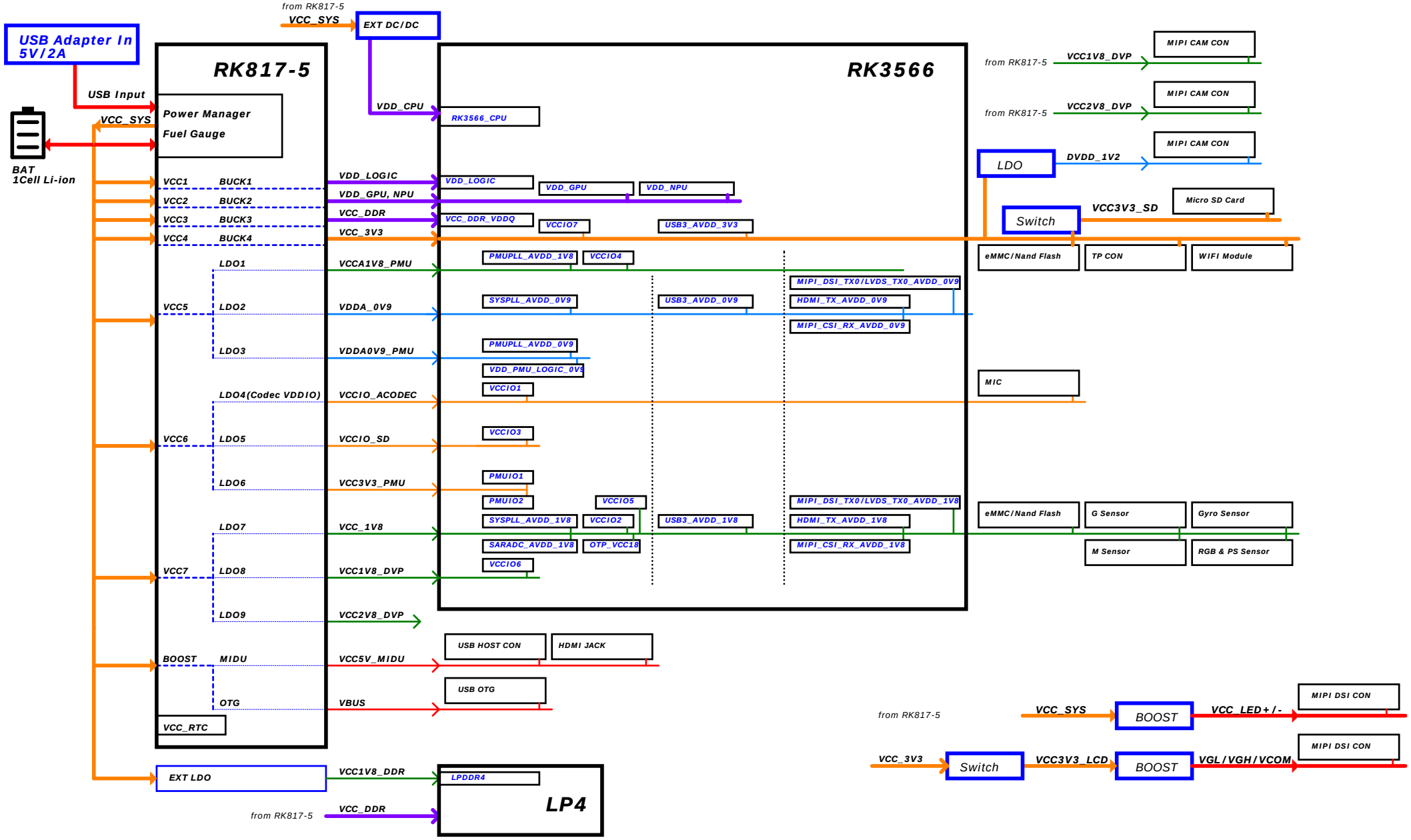
Power Diagram



PINE64	PINE64
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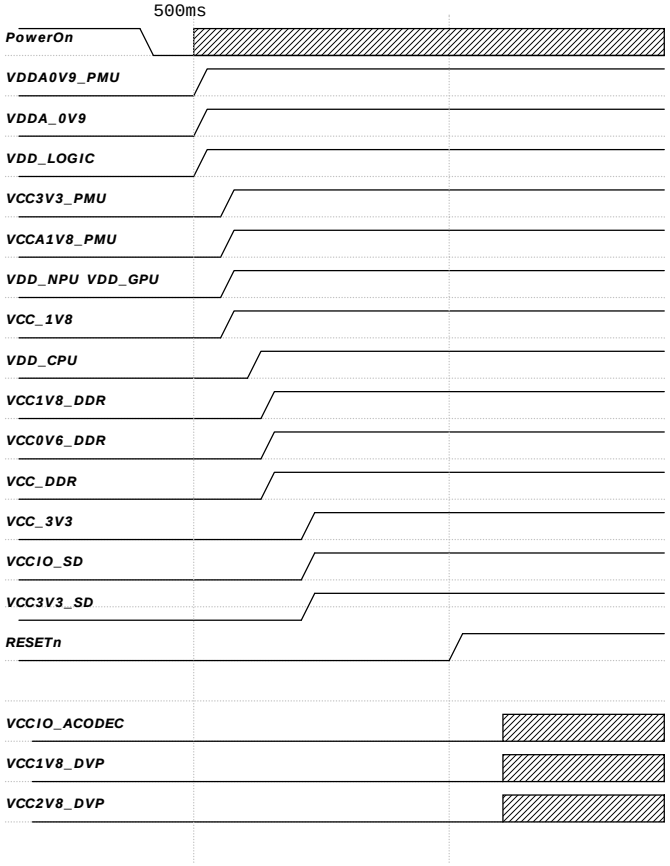
Power Sequence &Power Path assignment



Power Source	PMIC Channel	Supply Limit	Power Supply Name	Time Slot	Default Voltage	Work Status	Sleep Status
VCC_SYS	RK817-5_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_BUCK2	2.5A	VDD_NPU,VDD_GPU	Slot:2	0.9V	ON	OFF
VCC_SYS	RK817-5_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON
VCC_SYS	RK817-5_BUCK4	1.5A	VCC_3V3	Slot:4	3.3V	ON	OFF
VCC_SYS	RK817-5_LDO1	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON
	RK817-5_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF
	RK817-5_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_LDO4	0.4A	VCCIO_ACODEC	N/A	1.8V	ON	OFF
	RK817-5_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF
	RK817-5_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON
VCC_SYS	RK817-5_LDO7	0.4A	VCC_1V8	Slot:2	1.8V	ON	OFF
	RK817-5_LDO8	0.4A	VCC1V8_DVP	N/A	1.8V	ON	OFF
	RK817-5_LDO9	0.4A	VCC2V8_DVP	N/A	2.8V	ON	OFF
VCC_BAT	RK817-5_RESETn			Slot:4+5			
VCC_BAT	RK817-5_BOOST RK817-5_OTG	1.5A	VCC5V_MIDU VBUS	N/A	5.0V	ON	OFF
VCC_3V3	Switch		VCC3V3_SD	Slot:4	3.3V	ON	OFF
VCC_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO4	VCC1V8_PMU	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_1V8	1.8V	
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC1V8_DVP	1.8V	
VCCIO7	1N8	YES	YES	VCCIO7	VCC_3V3	3.3V	

PINE64

Project:	Quartz64 Model-A Schematic 20210427				
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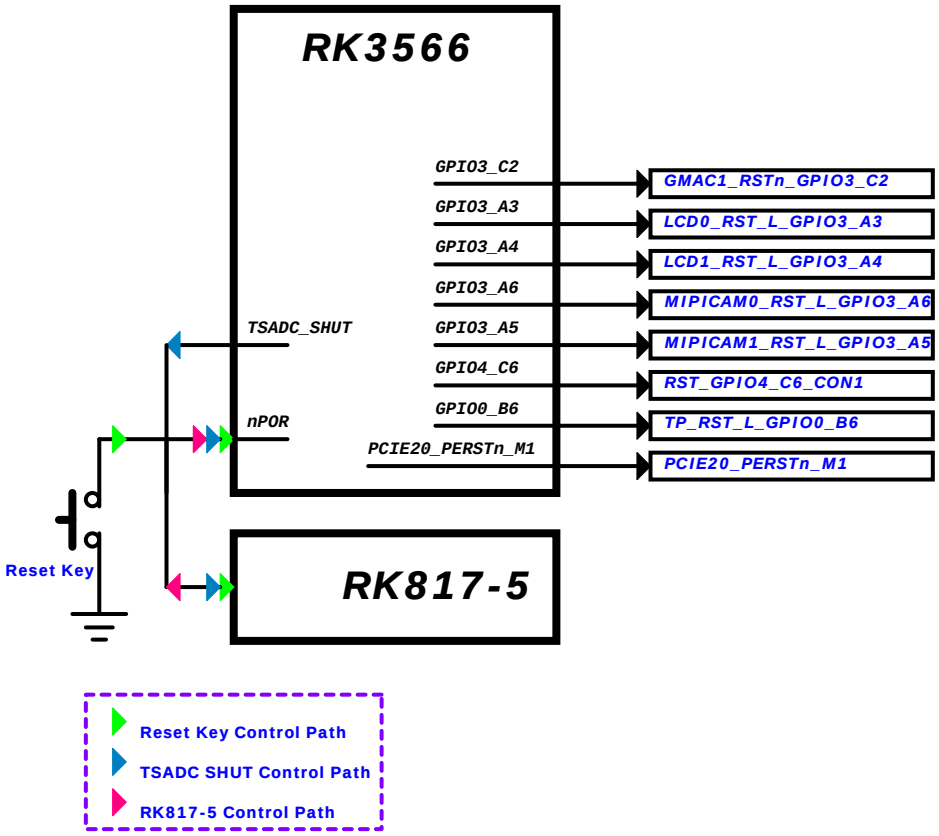
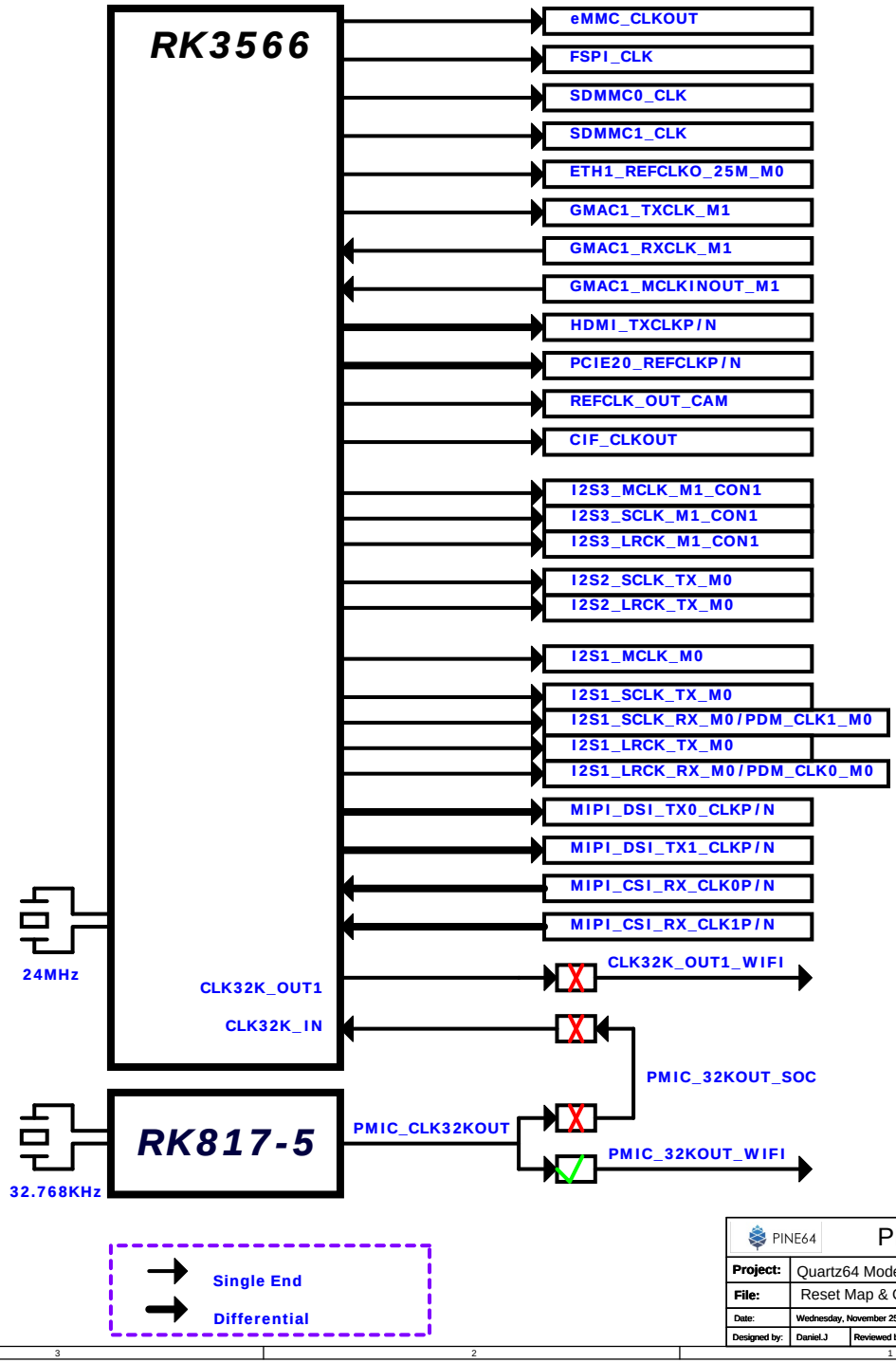
RESET Signal MAP



Clock Map



PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	Reset Map & Clock Map				
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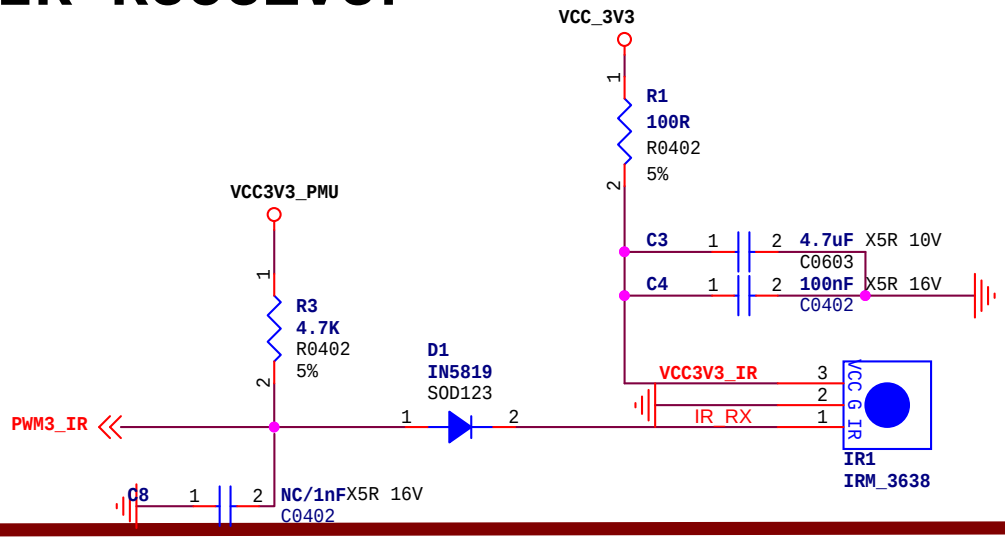
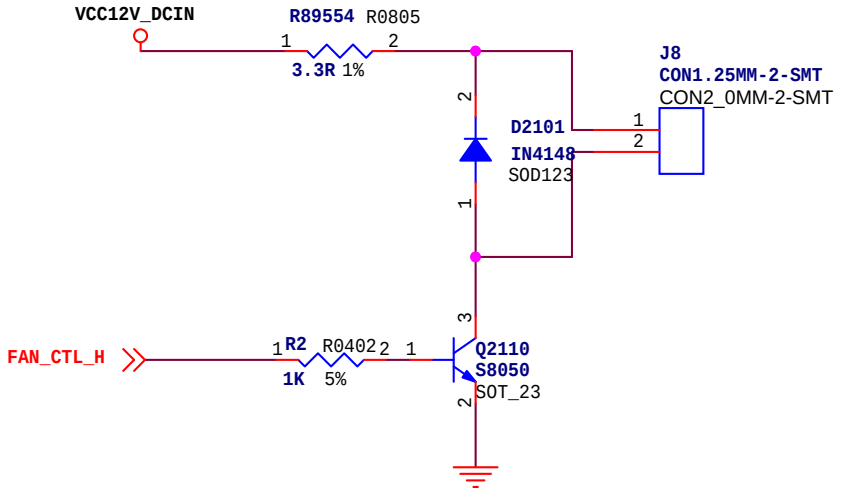
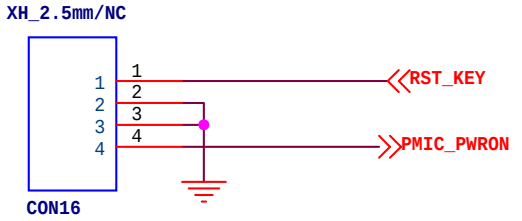
IR Receiver

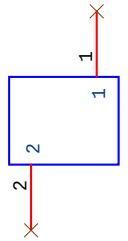


HEATSINK/FAN



Reset/PowerOn Connector





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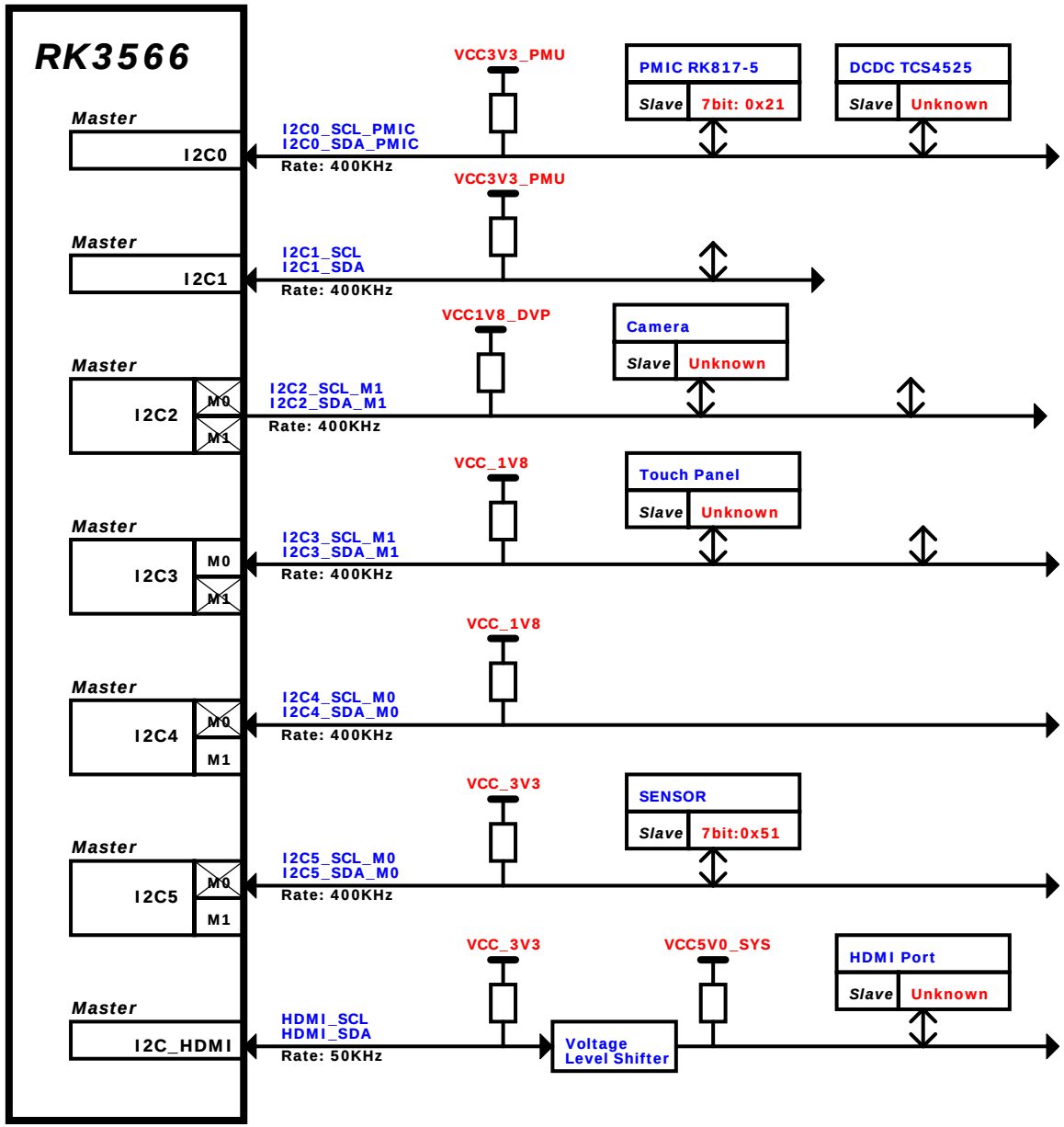
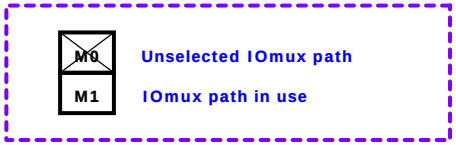
I2C MAP





PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	I2C Bus Map				
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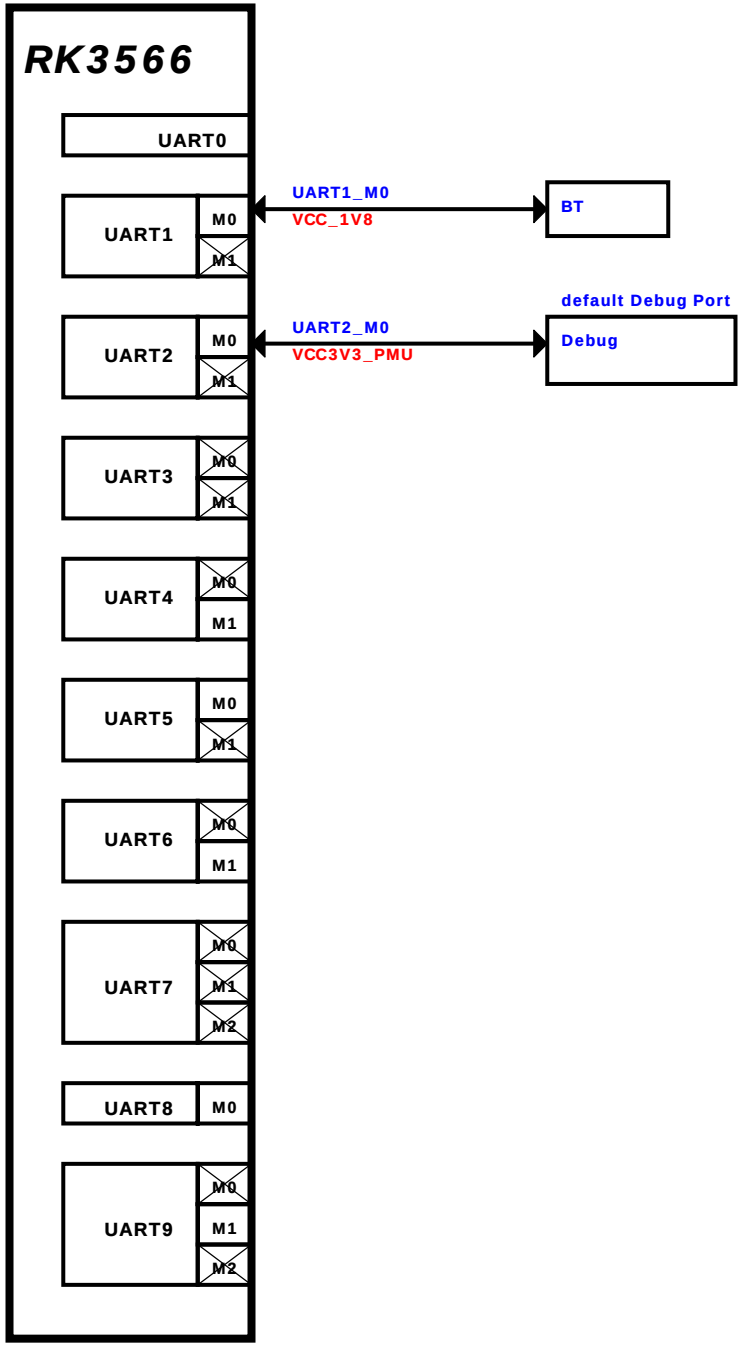
UART MAP



UART1_M0
VCC_1V8
BT

default Debug Port
UART2_M0
VCC3V3_PMU
Debug

M0 Unselected IOmux path
M1 IOmux path in use

PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
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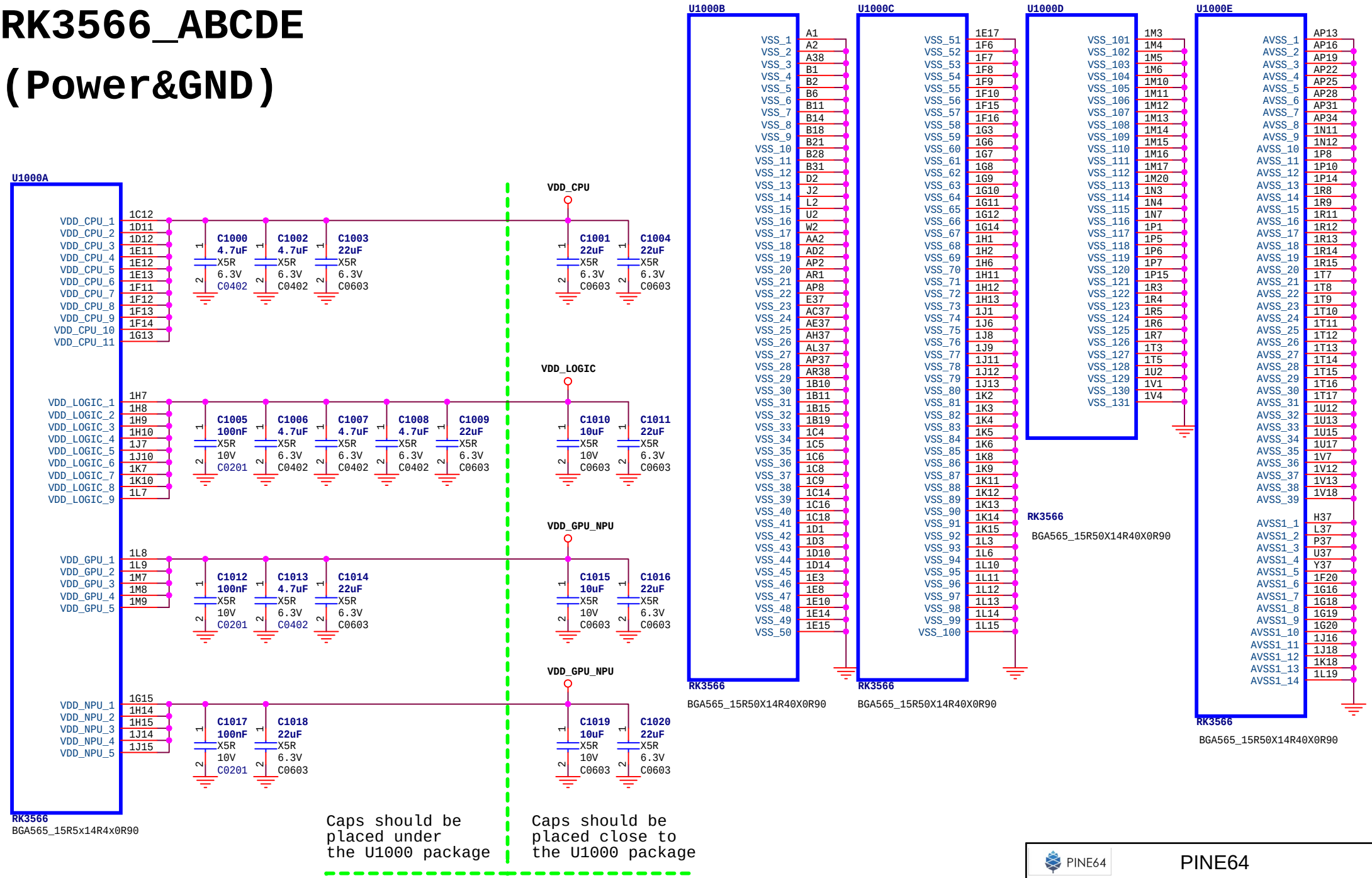
RK3566_ABCDE (Power&GND)



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Project:	Quartz64 Model-A Schematic 20210427				
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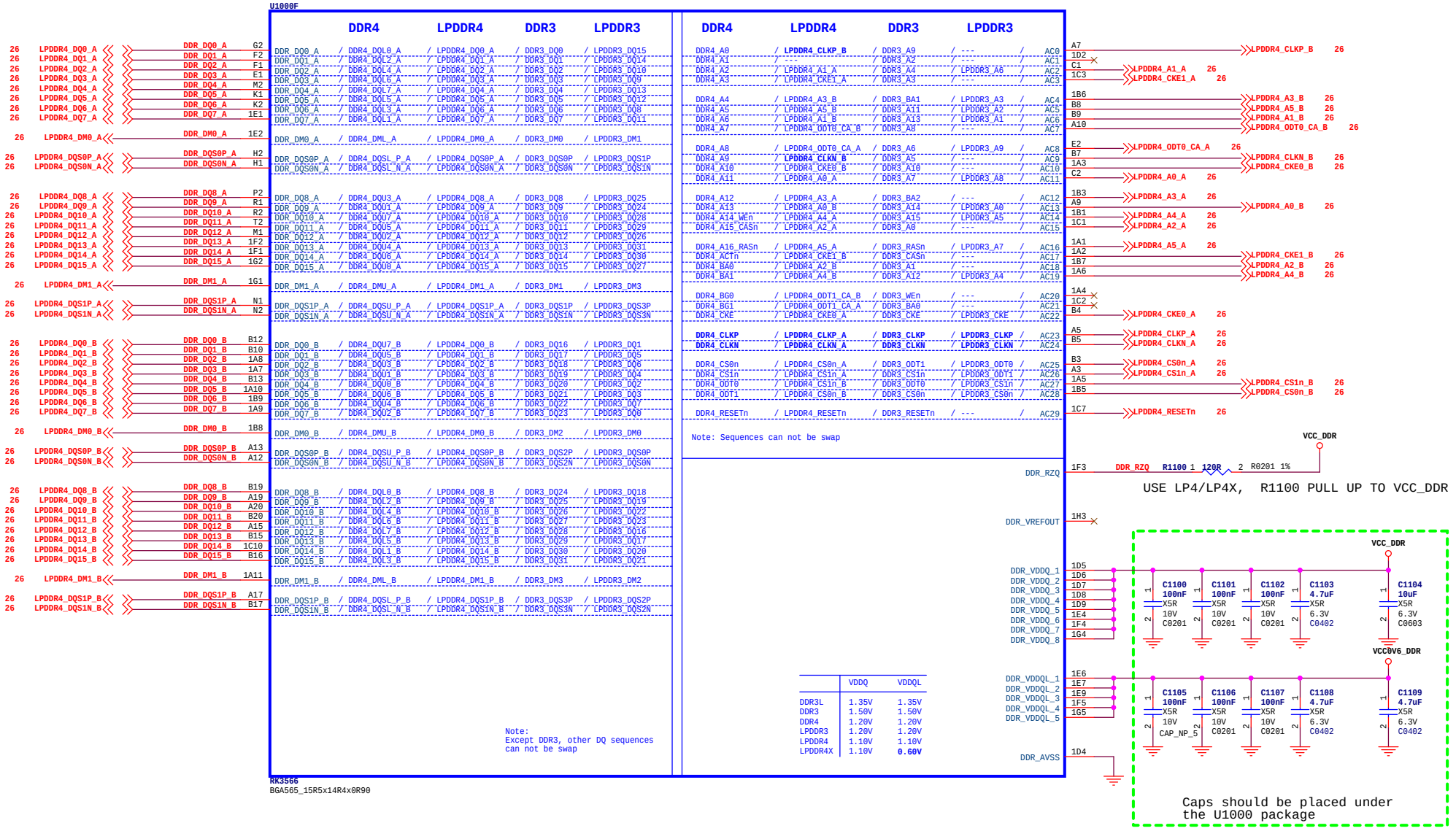
RK3566_F (DDR PHY)



PINE64	PINE64
Project:	Quartz64 Model-A Schematic 20210427
File:	RK3566 DDR Phy
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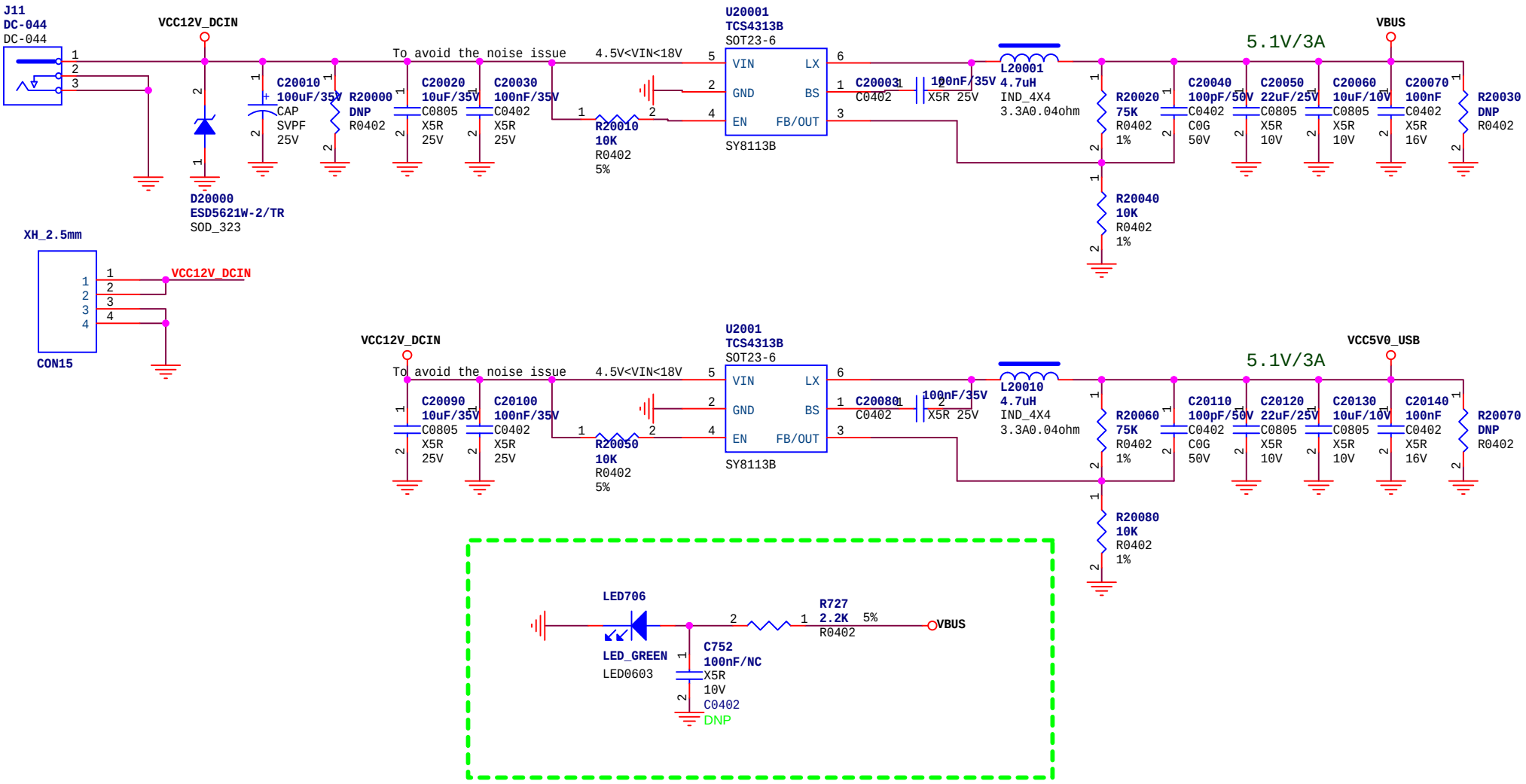
DC IN&SYSTEM Power



PINE64	PINE64	
Title	Quartz64 Model-A Schematic 20210427	
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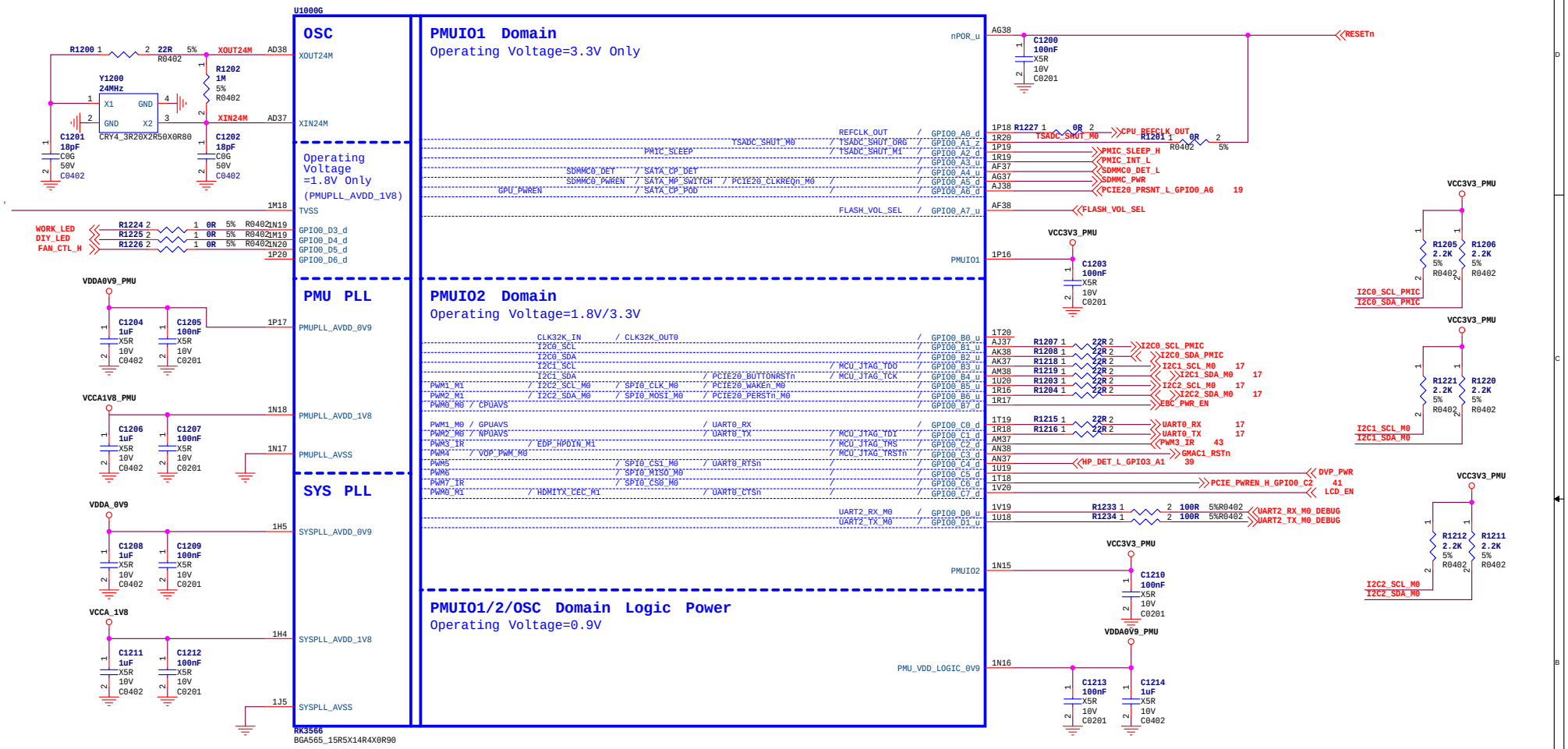
RK3566_G(OSC/PLL/PMUIO1/2)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	RK3566 OSC/PLL/PMUIO				
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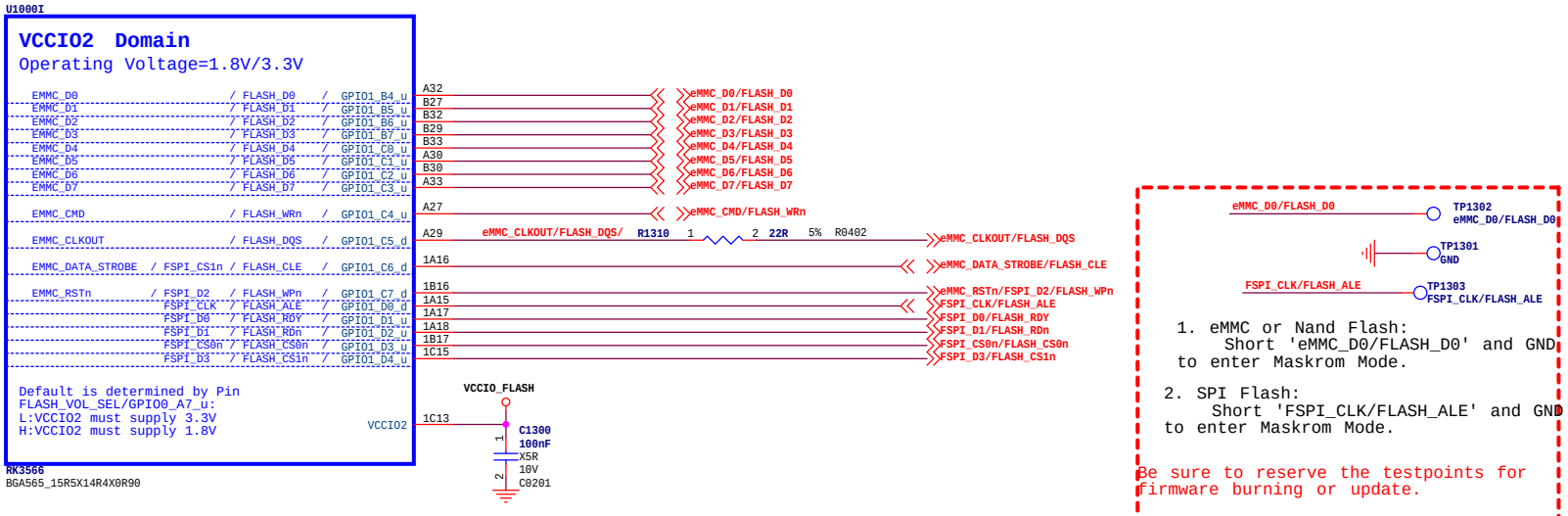
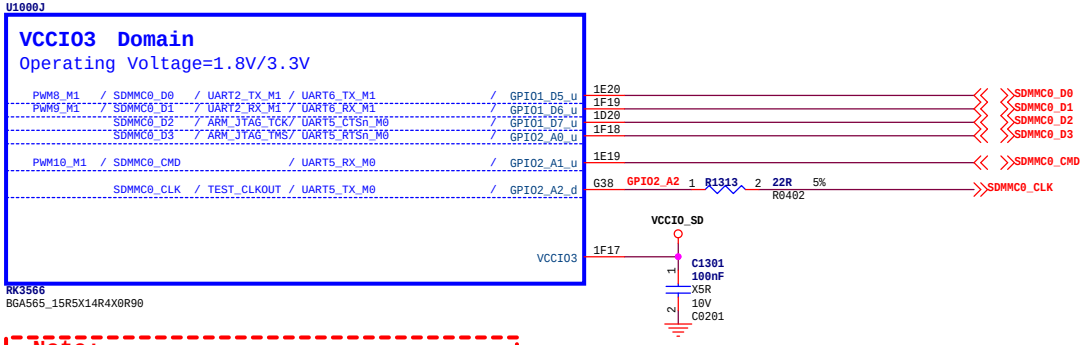
RK3566_I(VCCIO2 Domain)



RK3566_J(VCCIO3 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
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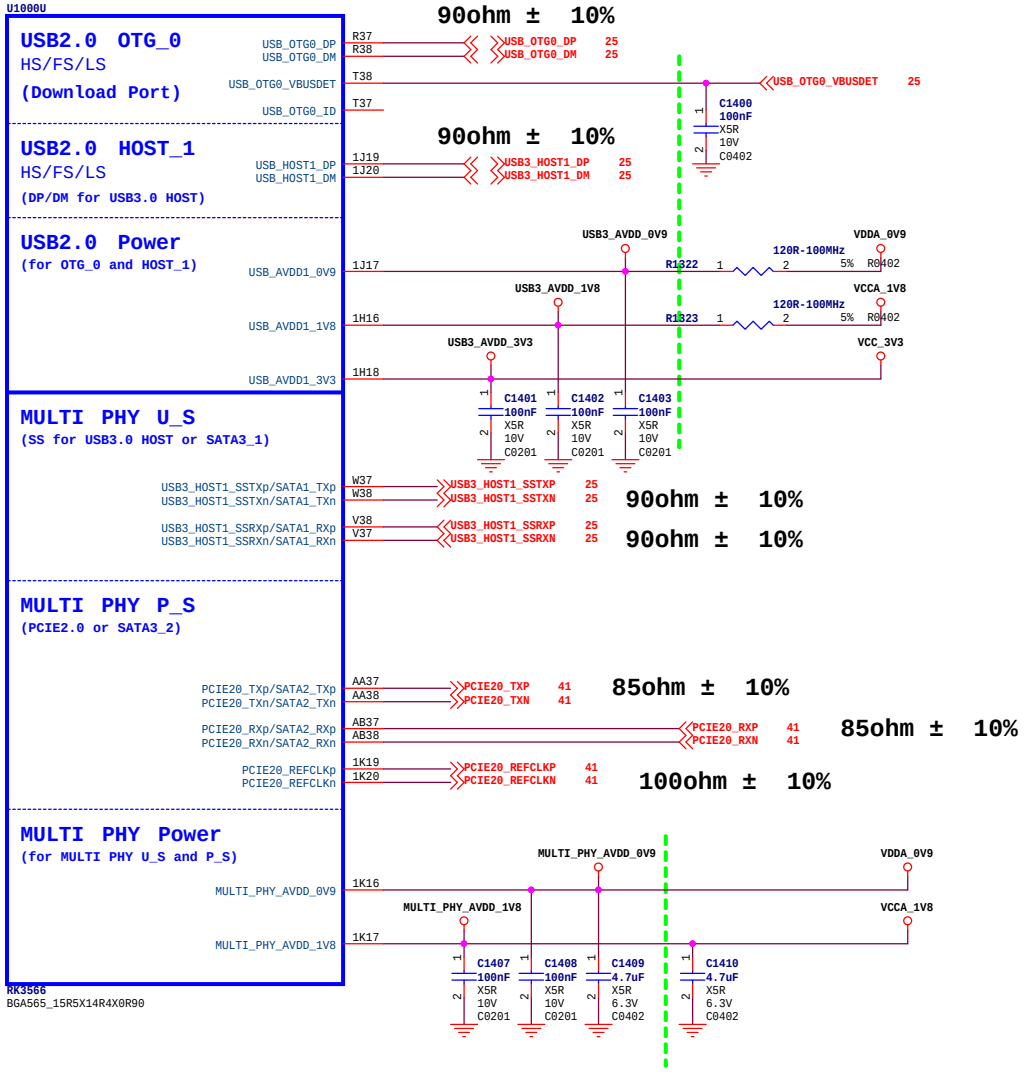
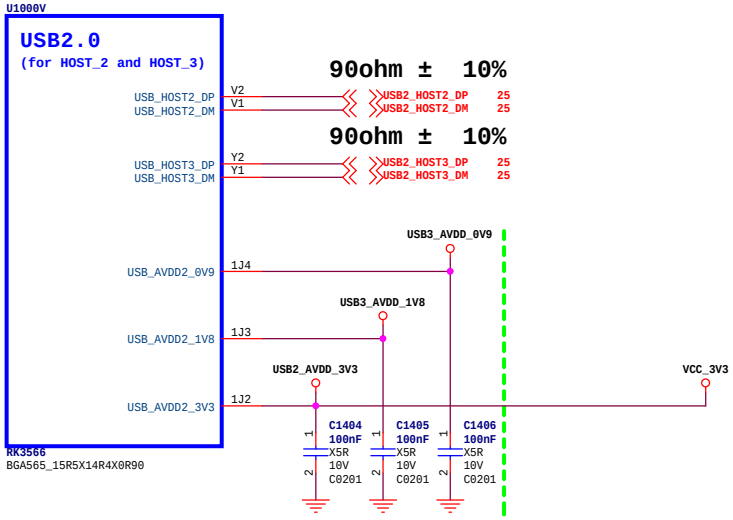
RK3566_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3566_V(USB2.0 HOST)



PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	RK3566 USB/PCIe/SATA PHY				
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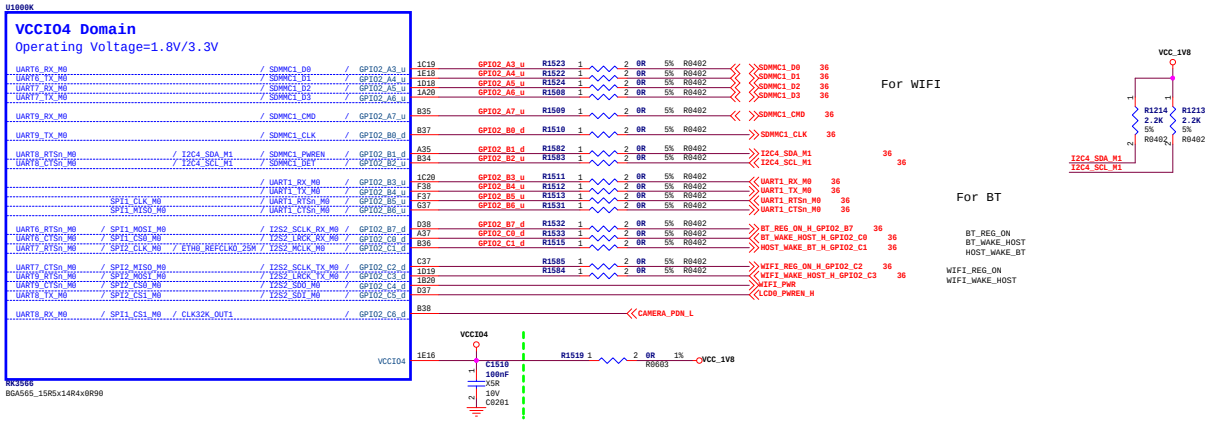
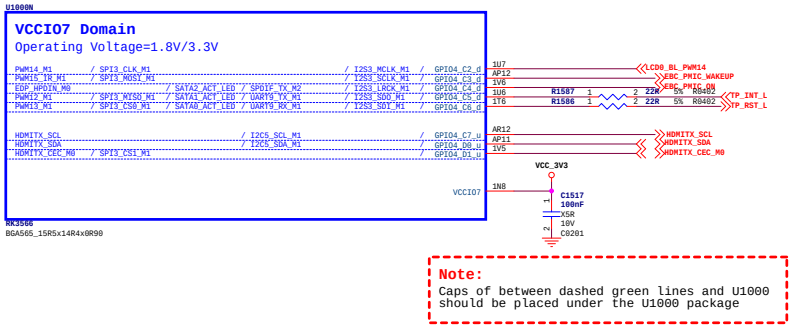
RK3566_K(VCCIO4 Domain)

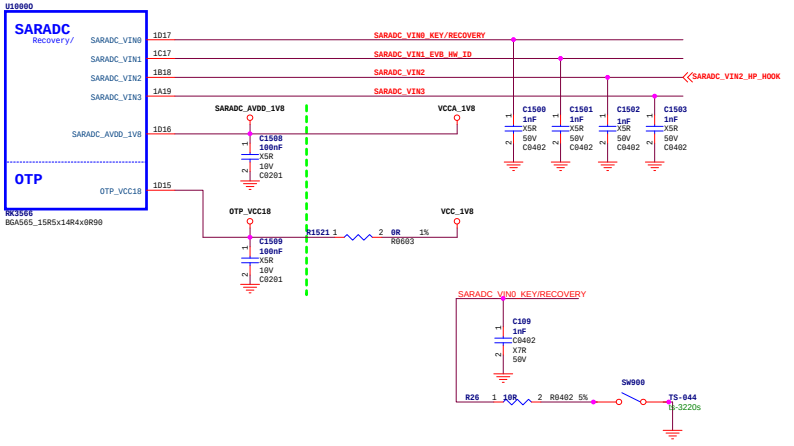


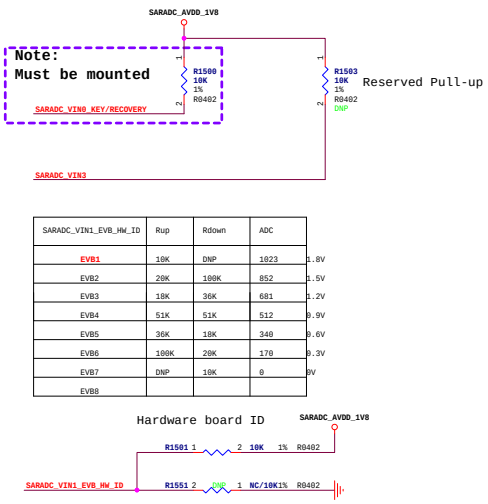
RK3566_N(VCCIO7 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3566_O(SARADC/OTP)





SARADC_VIN1_EVB_HW_ID	Rup	Rdown	ADC	
EVB1	10K	DNP	1023	1.8V
EVB2	20K	100K	852	1.5V
EVB3	18K	36K	681	1.2V
EVB4	51K	51K	512	0.9V
EVB5	36K	18K	340	0.6V
EVB6	100K	20K	170	0.3V
EVB7	DNP	10K	0	0V
EVB8				

Project:	Quartz64 Model-A Schematic 20210427
File:	RK3566 SARADC/GPIO
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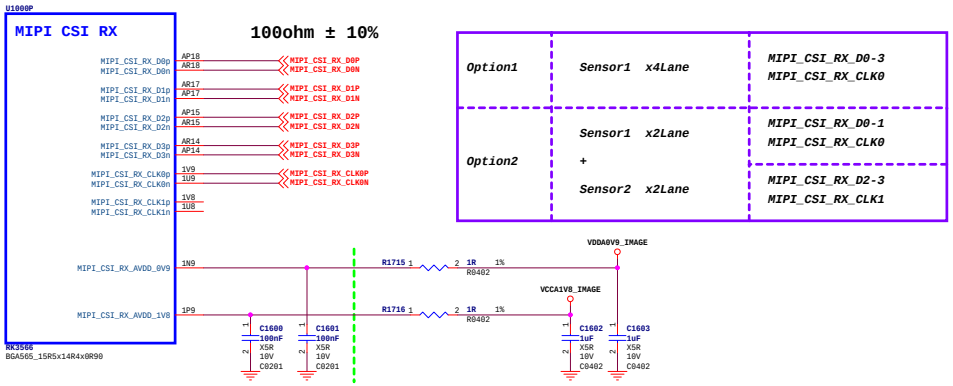
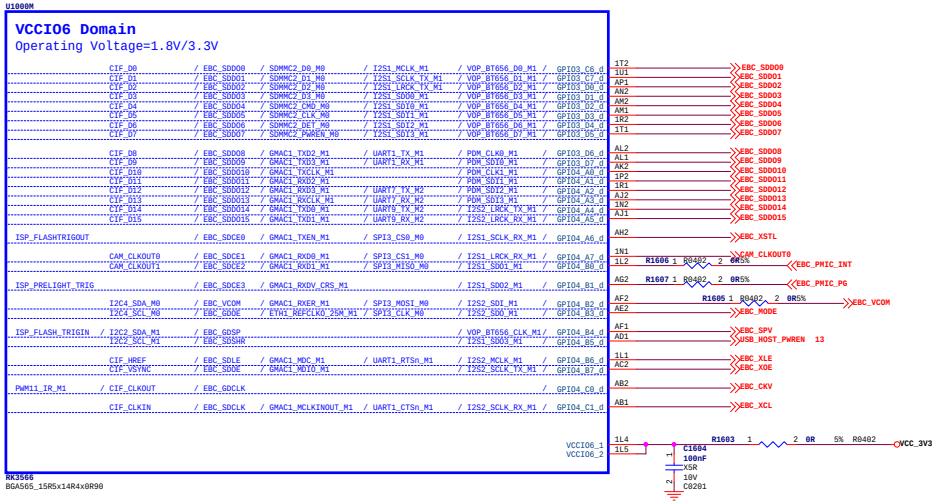
RK3566_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
		MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3566_M(VCCIO6 Domain)



Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

PINE64	PINE64
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File:	RK3566 VI Interface
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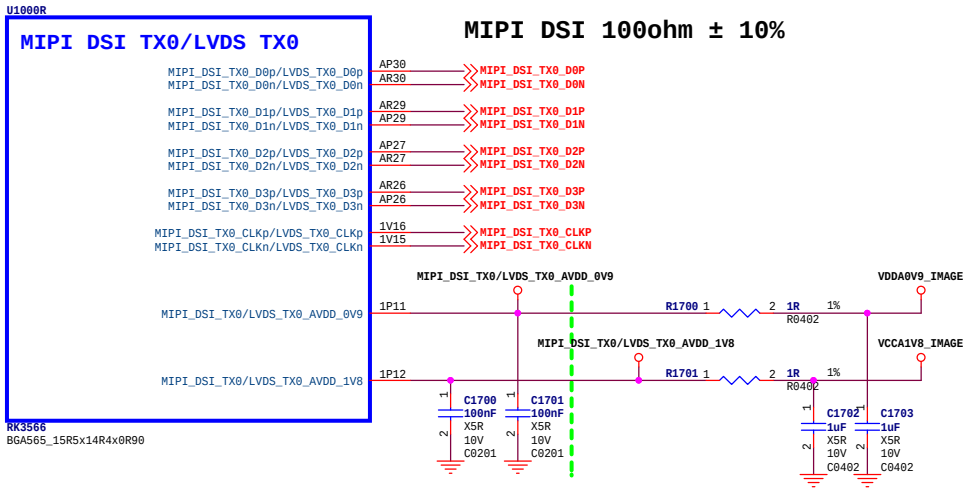
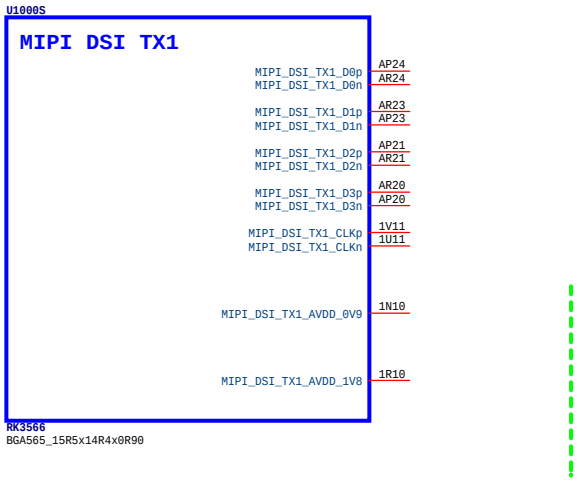
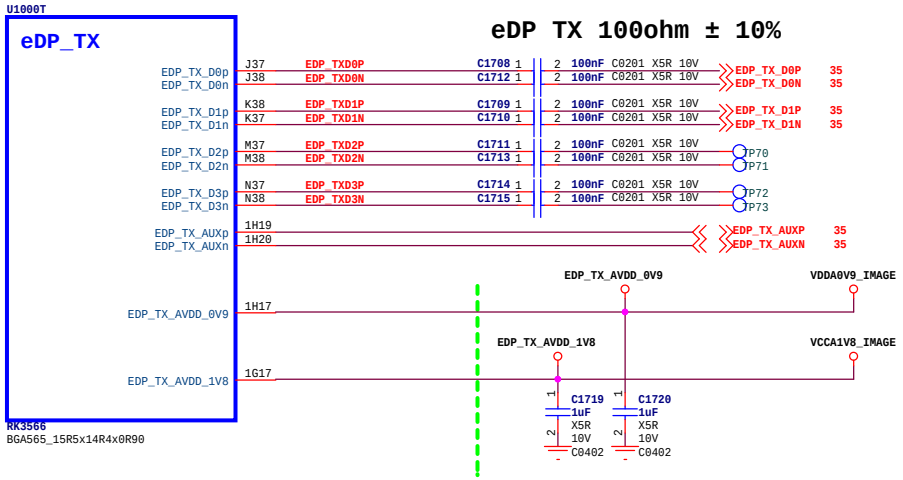
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



RK3566_S(MIPI_DSI_TX1)



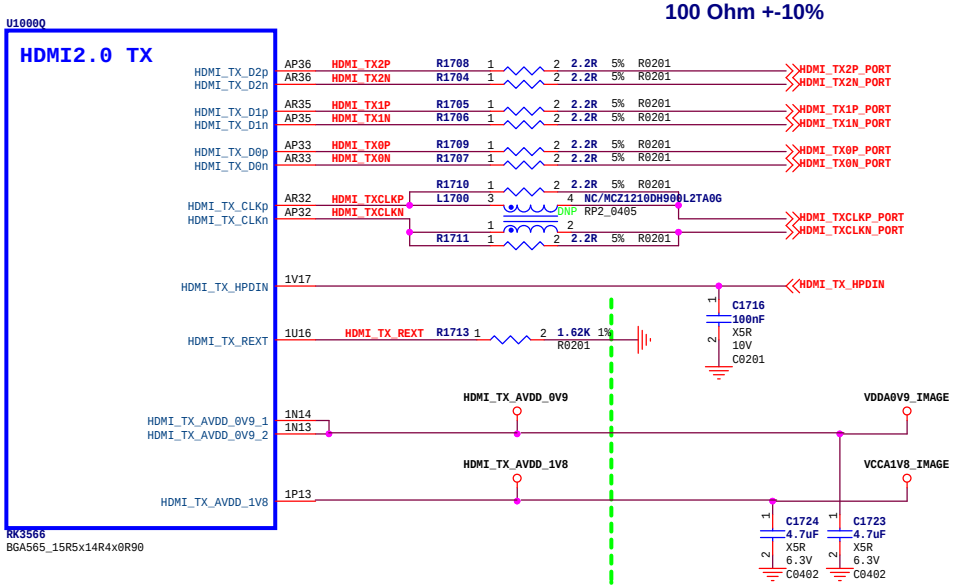
RK3566_T(eDP/DP TX)



Boxed capacitors should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3566_Q(HDMI2.0 TX)



PINE64

Project:	Quartz64 Model-A Schematic 20210427				
File:	RK3566 VO Interface 1				
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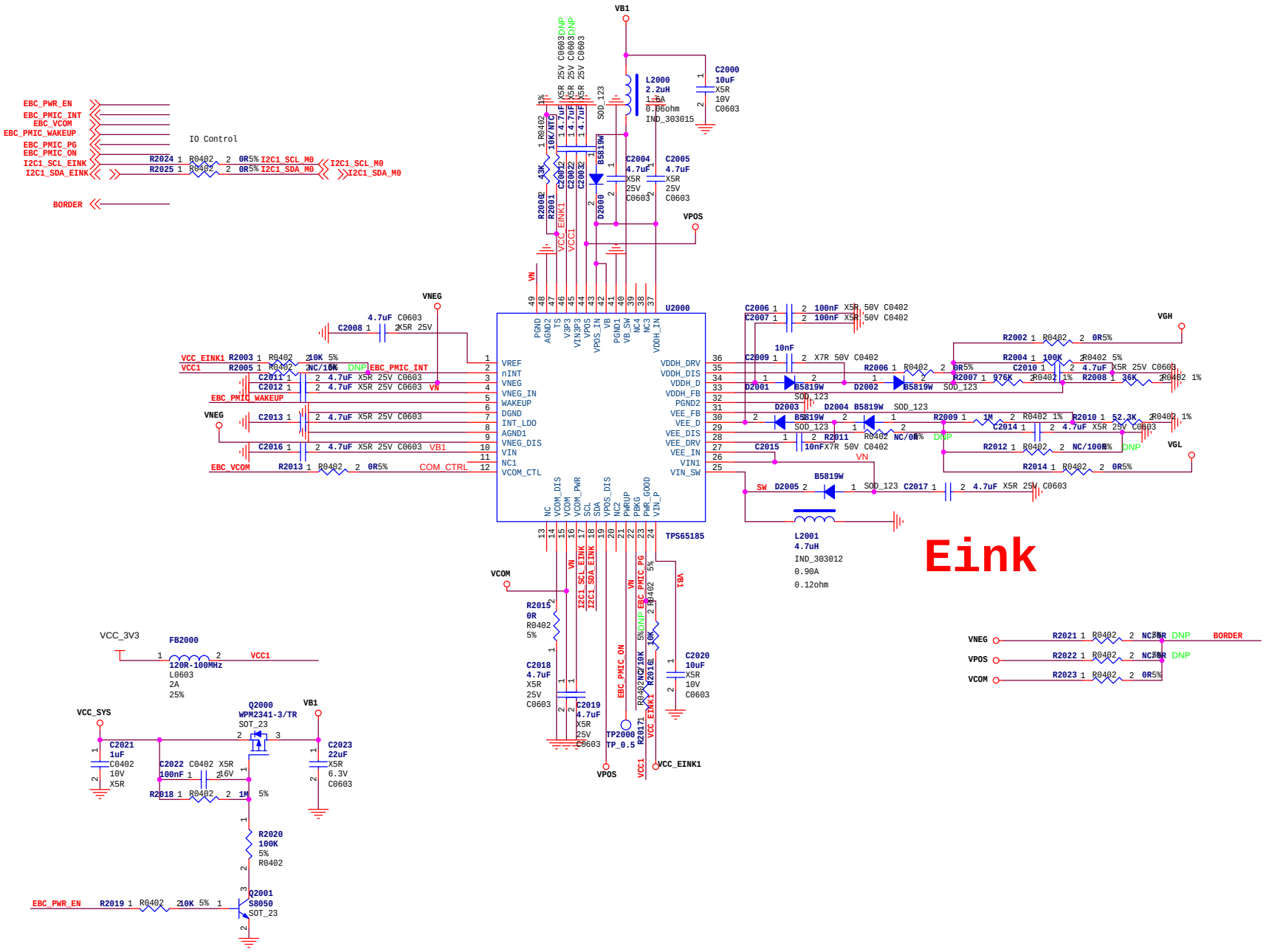

PINE64	PINE64		
Project:	Quartz64 Model-A Schematic 20210427		
File:	E-ink Interface		
Date:	Wednesday, November 25, 2020	Rev:	V2.0
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RK3566_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

	VOP_BT1120_D0	/ SPI1_CS0_M1		/ SDMMC2_D0_M1	/ GPIO3_A1_d
	VOP_BT1120_D1		/ GMAC1_TXD2_M0 / I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
	VOP_BT1120_D2		/ GMAC1_TXD3_M0 / I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
	VOP_BT1120_D3		/ GMAC1_RXD2_M0 / I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
	VOP_BT1120_D4		/ GMAC1_RXD3_M0 / I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
	VOP_BT1120_CLK		/ GMAC1_TXCLK_M0 / I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
	VOP_BT1120_D5		/ GMAC1_RXCLK_M0	/ SDMMC2_DET_M1	/ GPIO3_A7_d
	VOP_BT1120_D6		/ ETH1_REFCLKO_25M_M0	/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
PWM8_M0	/ VOP_BT1120_D7		/ GMAC1_RXD0_M0 / UART4_RX_M1		/ GPIO3_B1_d
PWM9_M0	/ VOP_BT1120_D8		/ GMAC1_RXD1_M0 / UART4_TX_M1		/ GPIO3_B2_d
	VOP_BT1120_D9	/ I2C5_SCL_M0	/ GMAC1_RXDV_CRS_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
	VOP_BT1120_D10	/ I2C5_SDA_M0	/ GMAC1_RXER_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
PWM10_M0	/ VOP_BT1120_D11	/ I2C3_SCL_M1	/ GMAC1_TXD0_M0		/ GPIO3_B5_d
PWM11_IR_M0	/ VOP_BT1120_D12	/ I2C3_SDA_M1	/ GMAC1_TXD1_M0		/ GPIO3_B6_d
PWM12_M0			/ GMAC1_TXEN_M0 / UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
PWM13_M0			/ GMAC1_MCLKINOUT_M0 / UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
	VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
	VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
	VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0		/ VOP_PWM_M1	/ GMAC1_MDC_M0 / UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0		/ SPDIF_TX_M1	/ GMAC1_MDIO_M0 / UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

RK3566
BGA565_15R5x14R4x0R90

1U5	R1809 1	2 22R 5% R0402	SPI1_CS0_M1		
AR10	R1802 1	2 22R 5% R0402	GMAC1_TXD2_M1		
AP10	R1801 1	2 22R 5% R0402	GMAC1_TXD3_M1		
AR9			GMAC1_RXD2_M1		
AP9			GMAC1_RXD3_M1		
1U4	R1803 1	2 22R 5% R0402	GMAC1_TXCLK_M1		
1V3			GMAC1_RXCLK_M1		
AR7	R1805 1	2 22R 5% R0402	GSENSOR_INT_L_GPIO3_B0	43	
AP7			GMAC1_RXD0_M1		
AR6			GMAC1_RXD1_M1		
AP6			GMAC1_RXDV_CRS_M1		
1U3			GMAC1_INT		
1T4	R1804 1	2 22R 5% R0402	GMAC1_TXD0_M1		
1V2	R1807 1	2 22R 5% R0402	GMAC1_TXD1_M1		
AP5	R1808 1	2 22R 5% R0402	GMAC1_TXEN_M1		
AR4					
AP4	R1810 1	2 22R 5% R0402	GMAC1_MCLKINOUT_M1		
AP3	R1811 1	2 22R 5% R0402	SPI1_MOSI_M1		
AR2	R1812 1	2 22R 5% R0402	SPI1_MISO_M1		
			SPI1_CLK_M1		
1P3			GMAC1_MDC_M1		
1P4			GMAC1_MDIO_M1		

VCCIO5

VCCIO5_1 1N5
VCCIO5_2 1N6

C1800 100nF X5R 10V C0201

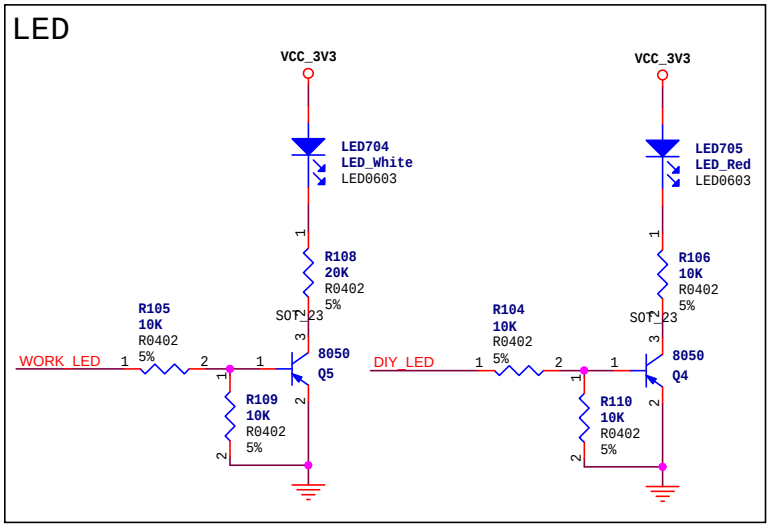
R1800 1 — 2 0R 1% R0603 — VCC_3V3

3.3V

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

WORK_LED
DIY_LED

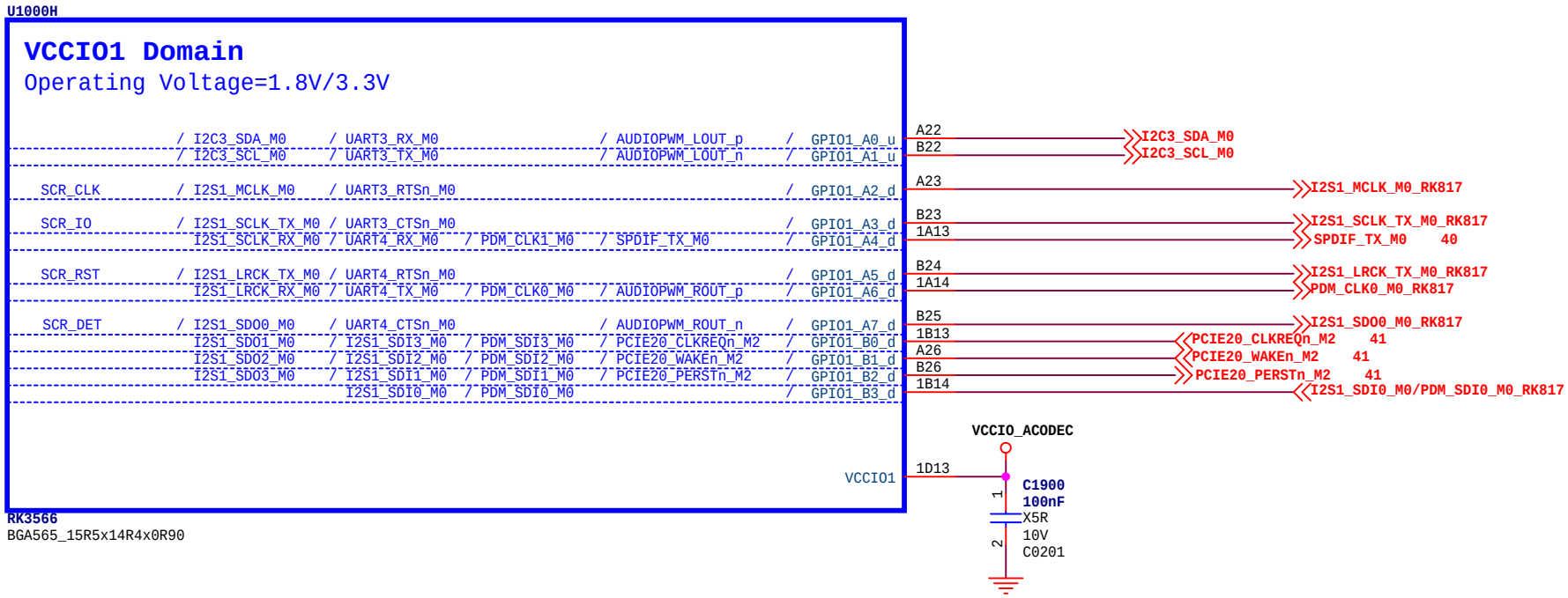
LED



VCC_3V3
R1825 10K 5% R0402
GMAC1_INT

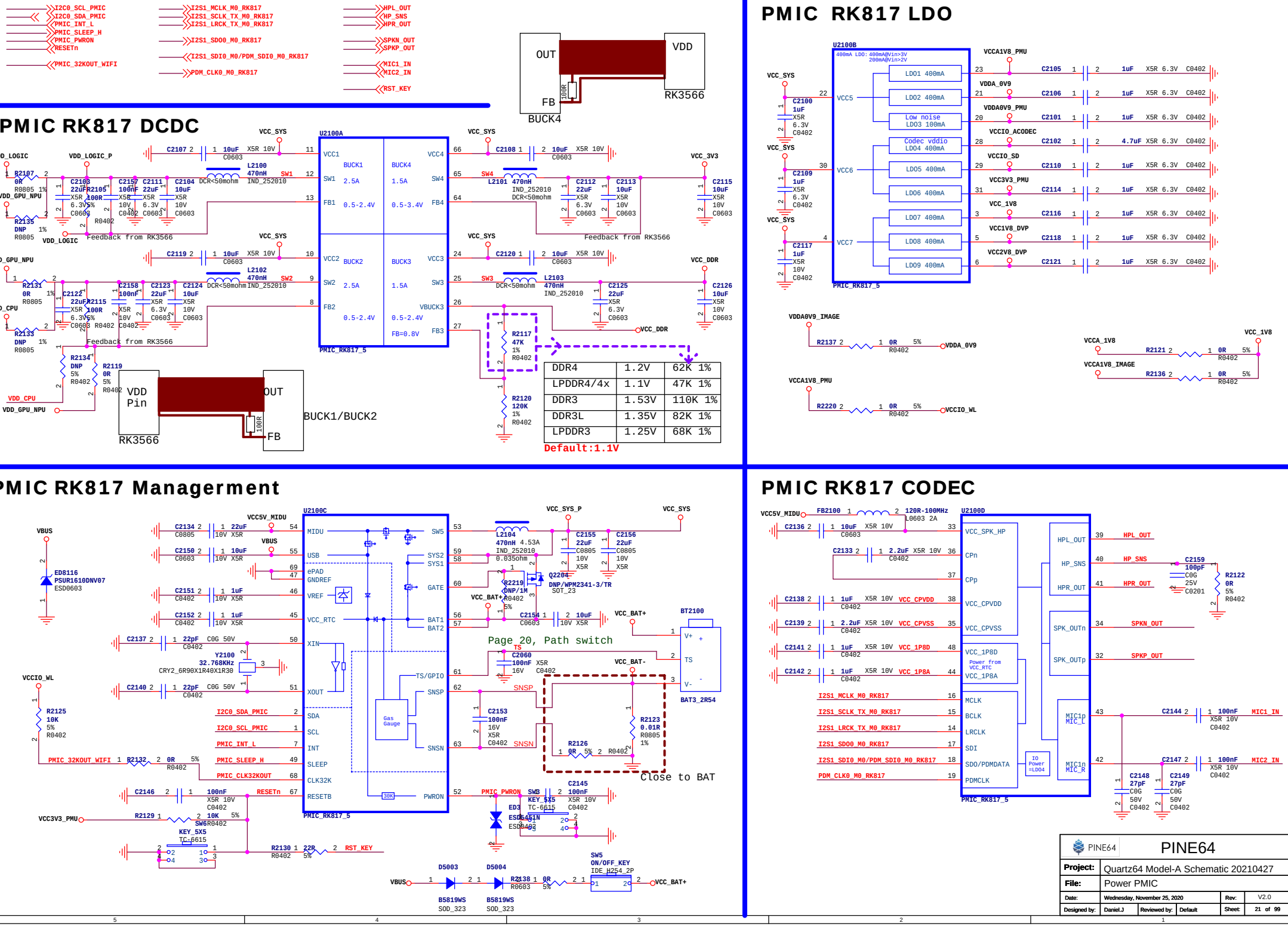
PINE64	PINE64		
Project:	Quartz64 Model-A Schematic 20210427		
File:	RK3566 RGMII Interface		
Date:	Wednesday, November 25, 2020	Rev:	V2.0
Designed by:	Daniel.J / Reviewed by: Default	Sheet:	18 of 99

RK3566_H(VCCIO1 Domain)



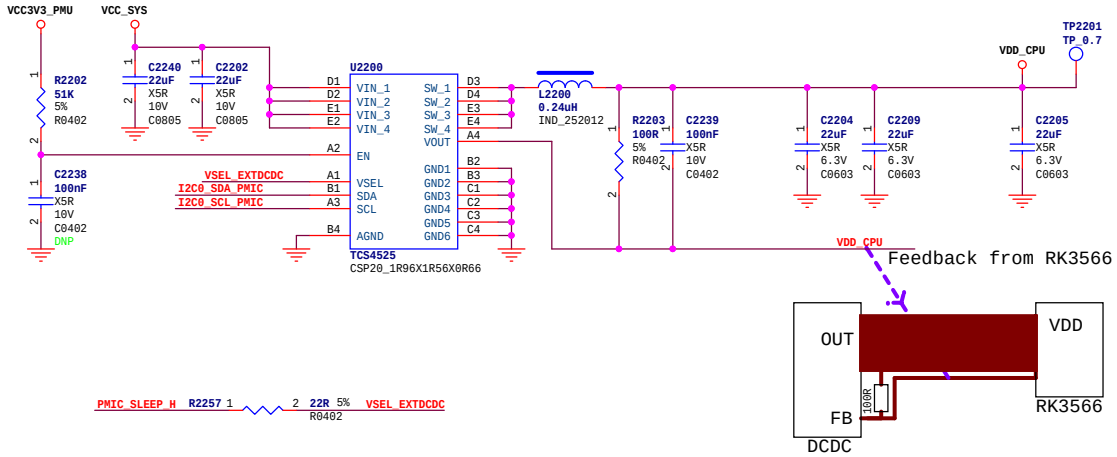
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	RK3566 Audio Interface				
Date:	Wednesday, November 25, 2020			Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	19 of 99


I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_INT_L
PMIC_SLEEP_H
PMIC_PWRON
RESETn
PMIC_32KOUT_WIFI
I2S1_MCLK_M0_RK817
I2S1_SCLK_TX_M0_RK817
I2S1_LRCK_TX_M0_RK817
I2S1_SDO0_M0_RK817
I2S1_SDI0_M0/PDM_SDI0_M0_RK817
PDM_CLK0_M0_RK817
HPL_OUT
HP_SNS
HPR_OUT
SPKN_OUT
SPKP_OUT
MIC1_IN
MIC2_IN
RST_KEY
OUT
VDD
FB
100R
RK3566
BUCK4
PMIC RK817 DCDC
VCC_SYS
U2100A
VDD_LOGIC
VDD_LOGIC_P
VDD_GPU_NPU
VDD_CPU
VCC_3V3
VCC_DDR
VCC1
VCC2
VCC3
VCC4
VBUCK3
BUCK1
BUCK2
BUCK3
BUCK4
SW1
SW2
SW3
SW4
FB1
FB2
FB3
FB4
2.5A
1.5A
0.5-2.4V
0.5-3.4V
0.5-2.4V
FB=0.8V
L2100 470nH IND_252010 DCR<50mohm
L2101 470nH IND_252010 DCR<50mohm
L2102 470nH DCR<50mohm IND_252010
L2103 470nH IND_252010
Feedback from RK3566
PMIC_RK817_5
R2117 47K 1% R0402
R2120 120K 1% R0402
BUCK1/BUCK2
VDD Pin
DDR4 1.2V 62K 1%
LPDDR4/4x 1.1V 47K 1%
DDR3 1.53V 110K 1%
DDR3L 1.35V 82K 1%
LPDDR3 1.25V 68K 1%
Default:1.1V
PMIC RK817 LDO
U2100B
400mA LDO: 400mA@Vin>3V 200mA@Vin>2V
VCC5
VCC6
VCC7
LDO1 400mA
LDO2 400mA
Low noise LDO3 100mA
Codec vddio LDO4 400mA
LDO5 400mA
LDO6 400mA
LDO7 400mA
LDO8 400mA
LDO9 400mA
VCCA1V8_PMU
VDDA_0V9
VDDA0V9_PMU
VCCIO_ACODEC
VCCIO_SD
VCC3V3_PMU
VCC_1V8
VCC1V8_DVP
VCC2V8_DVP
VDDA0V9_IMAGE
VCCA1V8_IMAGE
VCCA_1V8
VCCIO_WL
PMIC RK817 Managerment
U2100C
VCC5V_MIDU
VBUS
ED8116 PSUR1610DNV07 ESD0603
MIDU
USB
ePAD
GNDREF
VREF
VCC_RTC
XIN
XOUT
SDA
SCL
INT
SLEEP
CLK32K
RESETB
PWRON
SW5
SYS2
SYS1
GATE
BAT1
BAT2
TS/GPIO
SNSP
SNSN
Y2100 32.768KHz CRY2_6R90X1R40X1R30
Gas Gauge
I2C0_SDA_PMIC
I2C0_SCL_PMIC
PMIC_INT_L
PMIC_SLEEP_H
PMIC_CLK32KOUT
RESETn
PMIC_32KOUT_WIFI
VCC3V3_PMU
KEY_5X5 TC-6615
SW6
VCC_SYS_P
L2104 470nH 4.53A IND_252010 0.035ohm
Q2204 DNP/WPM2341-3/TR SOT_23
VCC_BAT+
VCC_BAT-
BT2100
BAT3_2R54
Page 20, Path switch
Close to BAT
PMIC_PWRON
KEY_5X5 TC-6615
ED3 ESD9451N
D5003 B5819WS SOD_323
D5004 B5819WS SOD_323
SW5 ON/OFF_KEY IDE_H254_2P
PMIC RK817 CODEC
U2100D
VCC5V_MIDU
FB2100 120R-100MHz 0603 2A
VCC_SPK_HP
CPn
CPp
VCC_CPVDD
VCC_CPVSS
VCC_1P8D
VCC_1P8A
MCLK
BCLK
LRCLK
SDI
SDO/PDMDATA
PDMCLK
HPL_OUT
HP_SNS
HPR_OUT
SPK_OUTn
SPK_OUTp
MIC1p MIC_L
MIC1n MIC_R
I2S1_MCLK_M0_RK817
I2S1_SCLK_TX_M0_RK817
I2S1_LRCK_TX_M0_RK817
I2S1_SDO0_M0_RK817
I2S1_SDI0_M0/PDM_SDI0_M0_RK817
PDM_CLK0_M0_RK817
IO Power =LDO4
PMIC_RK817_5
PINE64
Project: Quartz64 Model-A Schematic 20210427
File: Power PMIC
Date: Wednesday, November 25, 2020
Rev: V2.0
Designed by: Daniel.J
Reviewed by: Default
Sheet: 21 of 99

I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_SLEEP_H

VDD_CPU_EXT

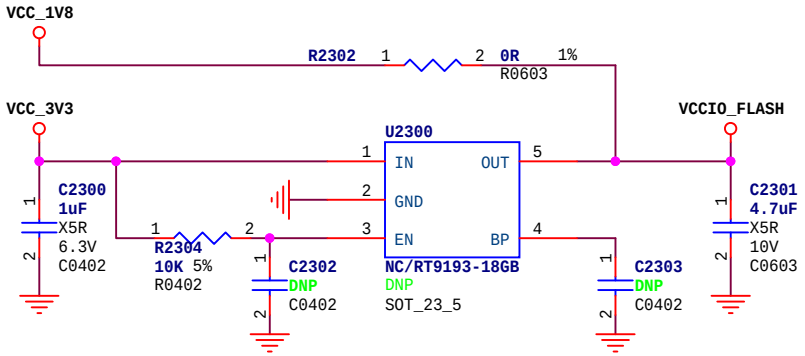


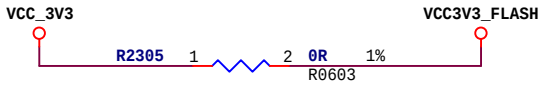
PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	Power DC IN				
Date:	Wednesday, November 25, 2020			**Rev:**	V2.0
Designed by:	DanielJ	**Reviewed by:**	Default	**Sheet:**	22 of 99

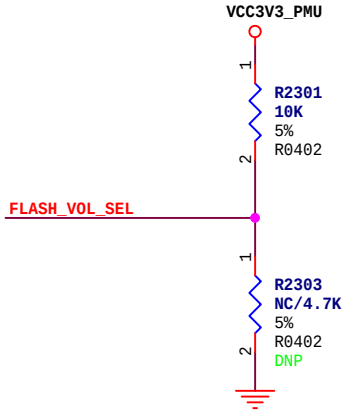
Flash Power Manage

FLASH_VOL_SEL

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)

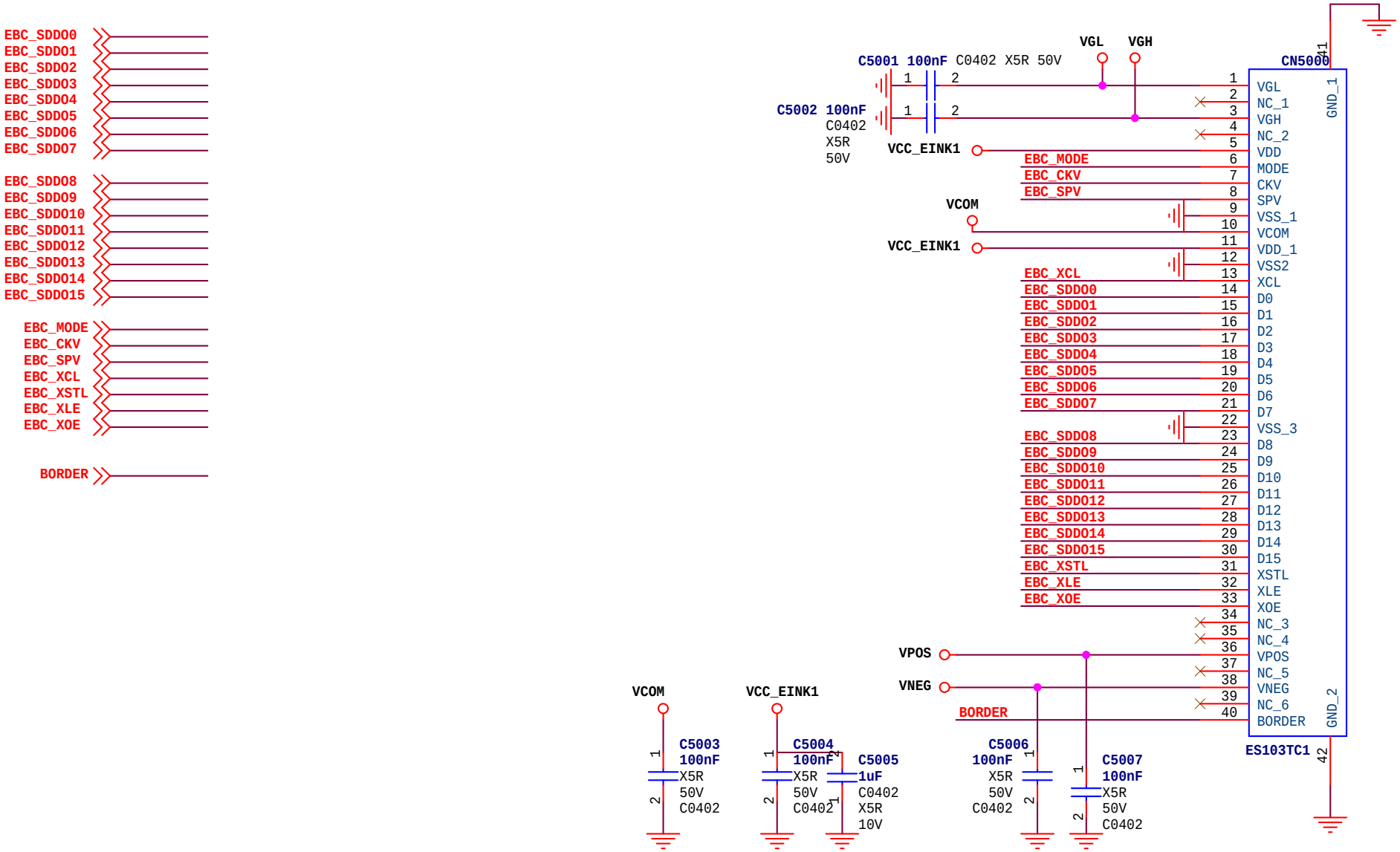






Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	Flash Power Manage				
Date:	Wednesday, November 25, 2020			Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	23 of 99



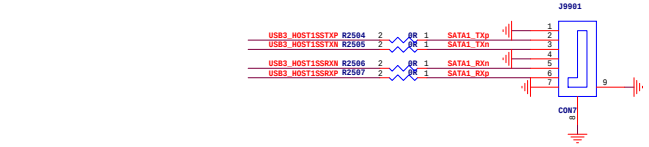
PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	E-Ink Interface				
Date:	Wednesday, November 25, 2020			Rev:	V2.0
Designed by:	ZHM	Reviewed by:	<Checker>	Sheet:	24 of 33

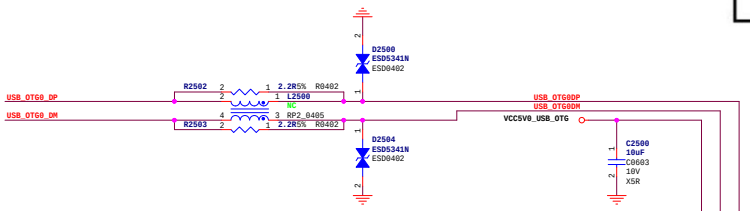
SATA

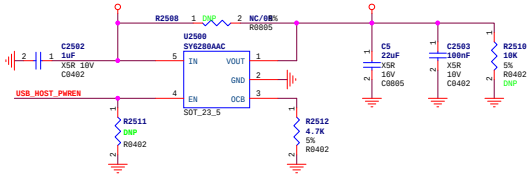
主板 SATA 串口硬盘接口。

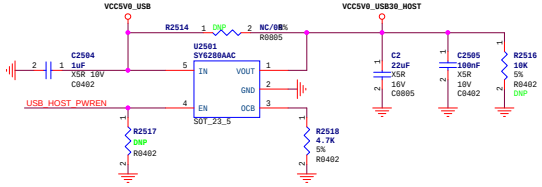
SATA1~SATA4针脚定义

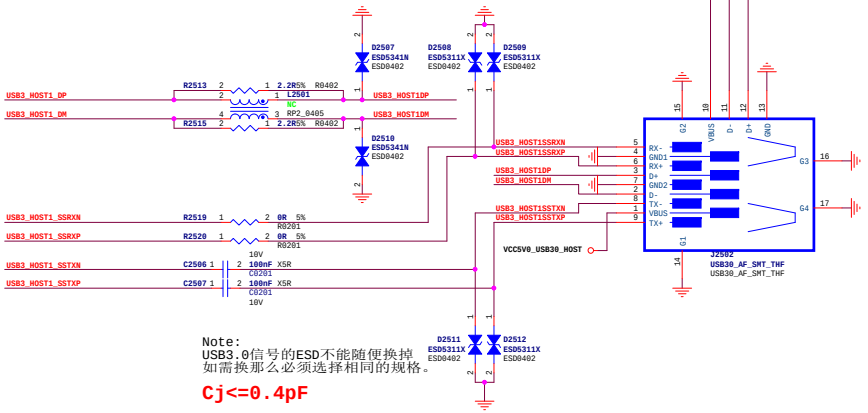
PIN	SIGNAL	PIN	SIGNAL
1	GND	2	TXP
3	TXN	4	GND
5	RXN	6	RXP
7	GND		









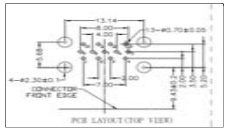


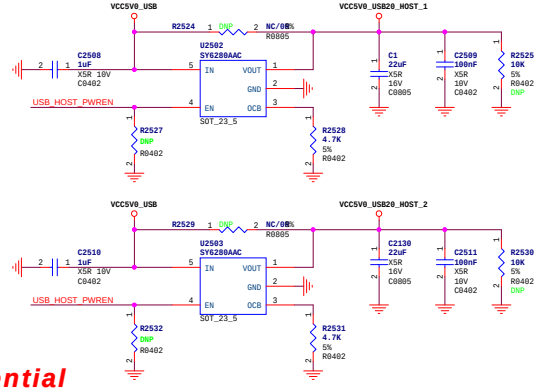
Note:
USB3.0信号的ESD不能随便换掉
如需换那么必须选择相同的规格。

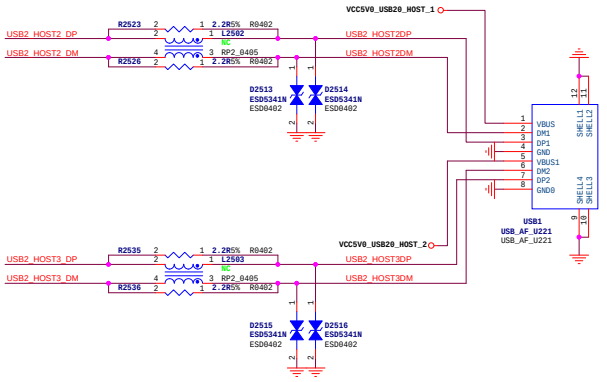
Cj<=0.4pF

USB2.0 HOST2

USB3.0 HOST1





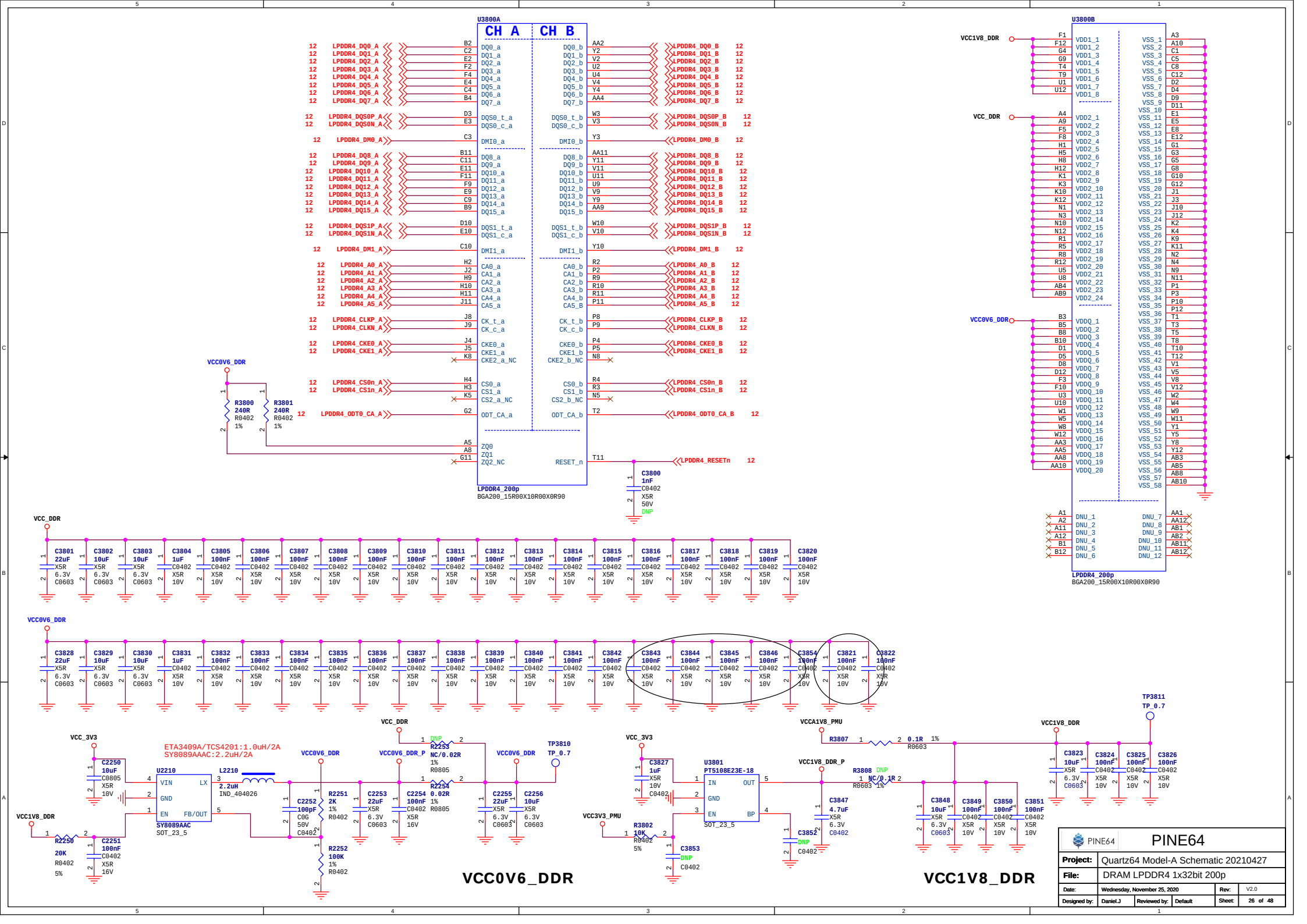


USB2.0 HOST2

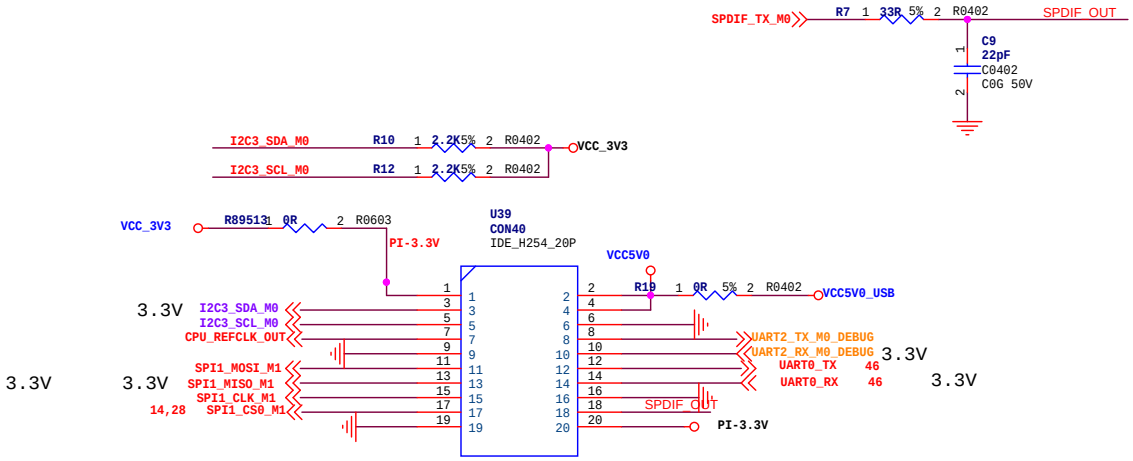
USB2.0 HOST3

Rockchip Confidential

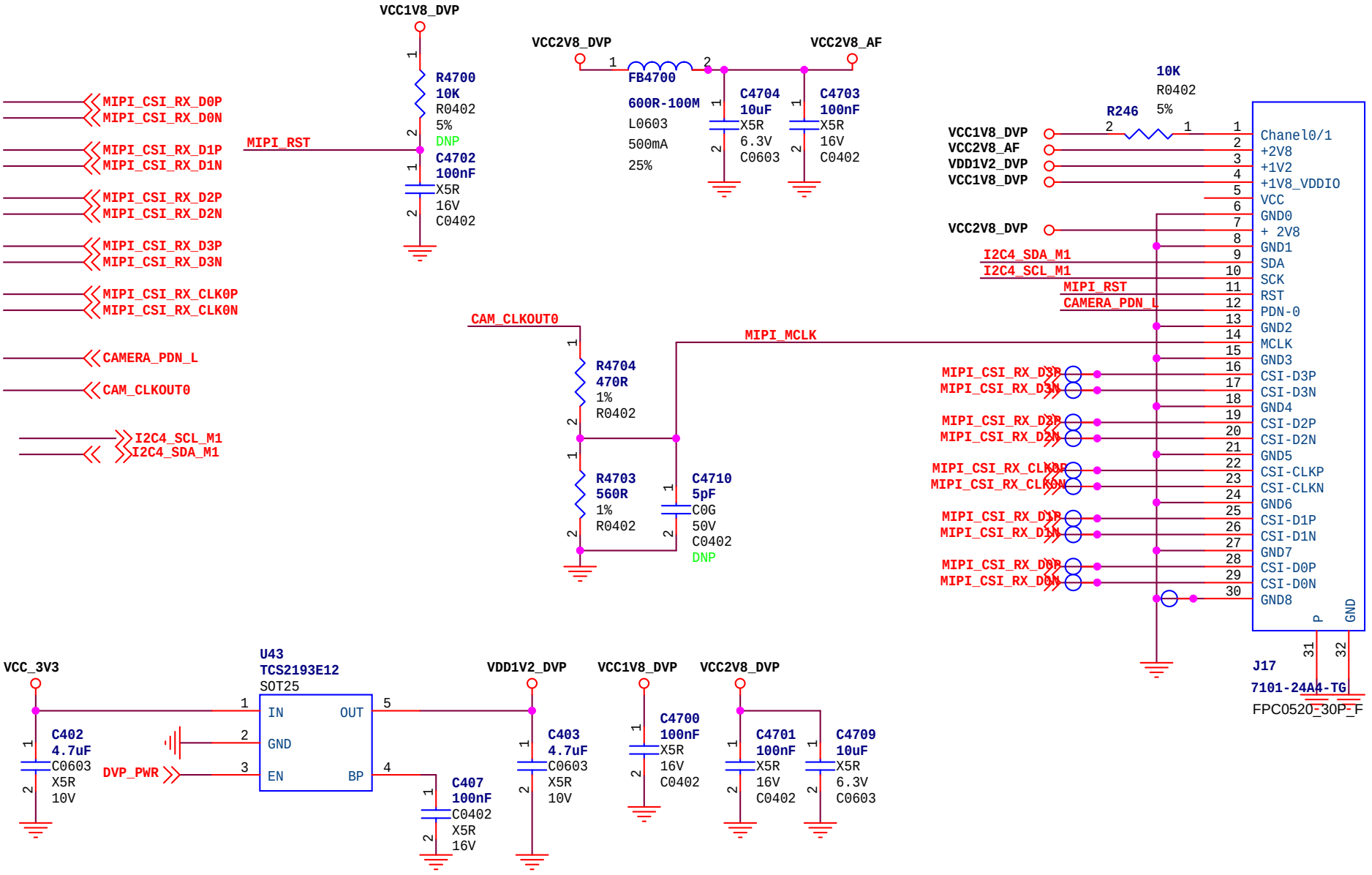
PINE64	PINE64
Project:	Quartz64 Model-A Schematic 20210427
File:	USB2/USB3 Port
Date:	Wednesday, November 25, 2020
Rev:	V2.0
Designed by:	Daniel.J
Reviewed by:	Default
Sheet:	25 of 48



Project:	Quartz64 Model-A Schematic 20210427
File:	DRAM LPDDR4 1x32bit 200p
Date:	Wednesday, November 25, 2020
Rev:	V2.0
Designed by:	DanielJ
Reviewed by:	Default
Sheet:	26 of 48



PINE64	PINE64	
Title	Quartz64 Model-A Schematic 20210427	
Size: B	Document Number: GPIO BUS	Rev: V2.0
Date:	Sheet 29 of 33	



PINE64

Title: Quartz64 Model-A Schematic 20210427

Size	Document Number	Rev
A	CAMERA	V2.0

Date:

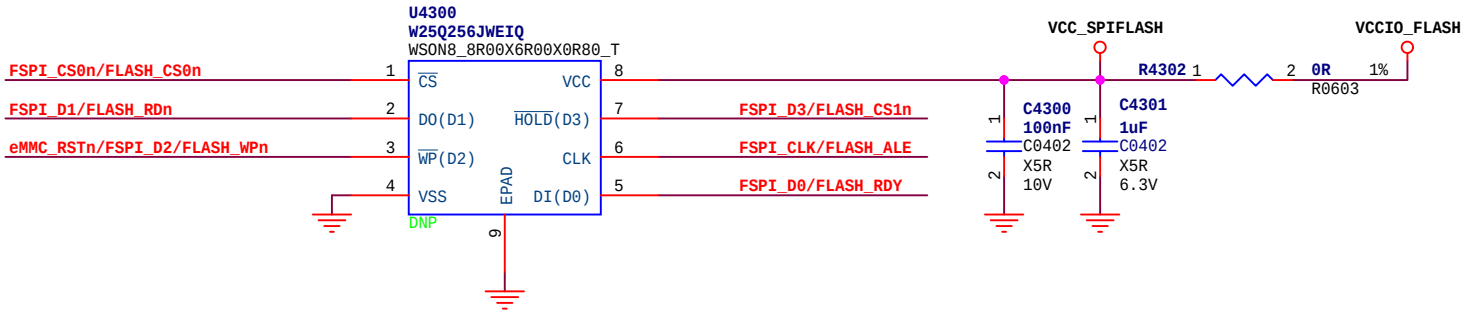
Sheet 30 of 33

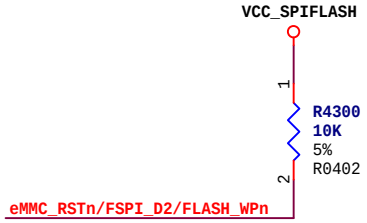
FSPI_CLK/FLASH_ALE 14,28

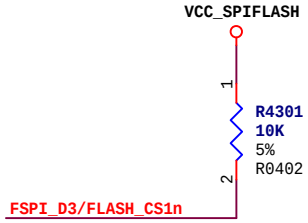
FSPI_D0/FLASH_RDY 14,28
FSPI_D1/FLASH_RDn 14,28
eMMC_RSTn/FSPI_D2/FLASH_WPn 14,27,28
FSPI_D3/FLASH_CS1n 14,28

FSPI_CS0n/FLASH_CS0n 14,28

default VCC = 1.8V

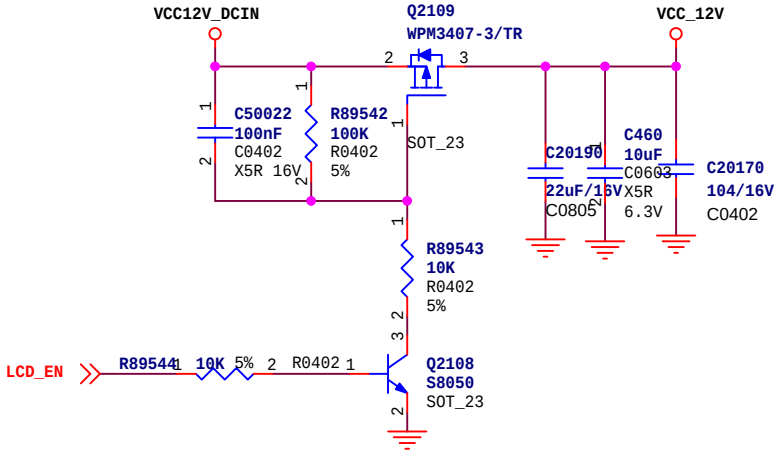


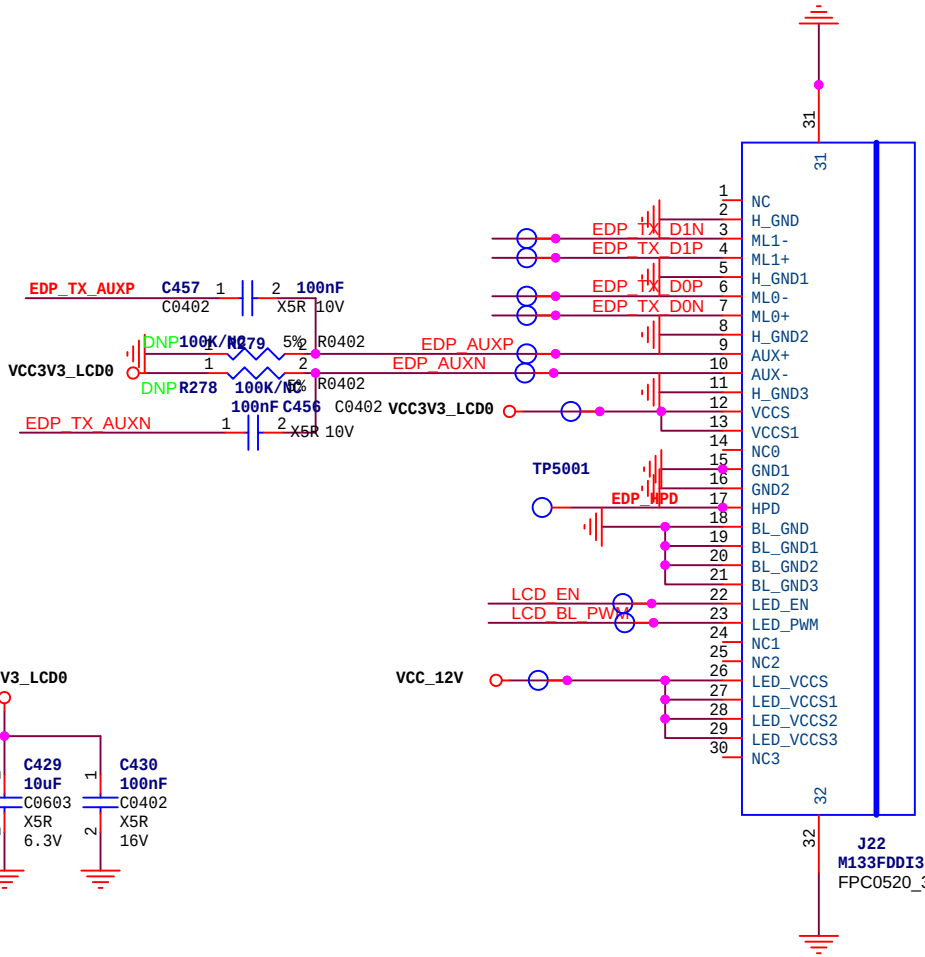




PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	Flash SPI NOR				
Date:	Wednesday, November 25, 2020			**Rev:**	V2.0
Designed by:	Daniel.J	**Reviewed by:**	Default	**Sheet:**	31 of

eDP Panel

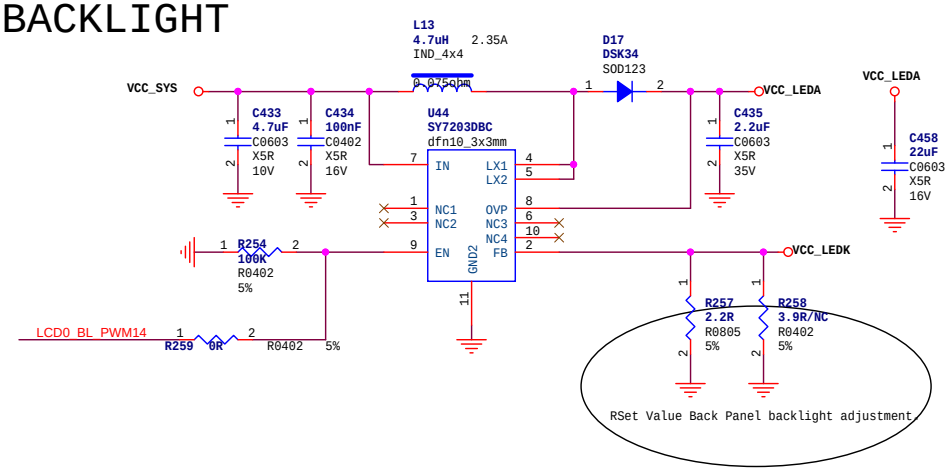




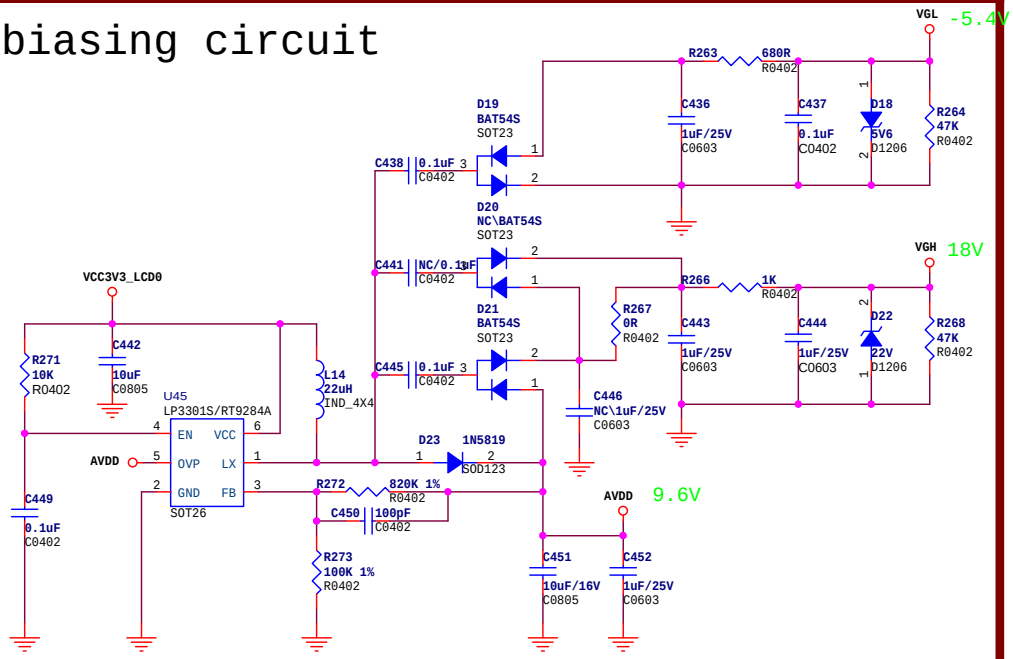
PINE64	PINE64	
Title: Quartz64 Model-A Schematic 20210427		
Size: A4	Document Number: LCD EDP	Rev: V2.0
Date: Tuesday, MAR 6, 2018	Sheet 32 of	

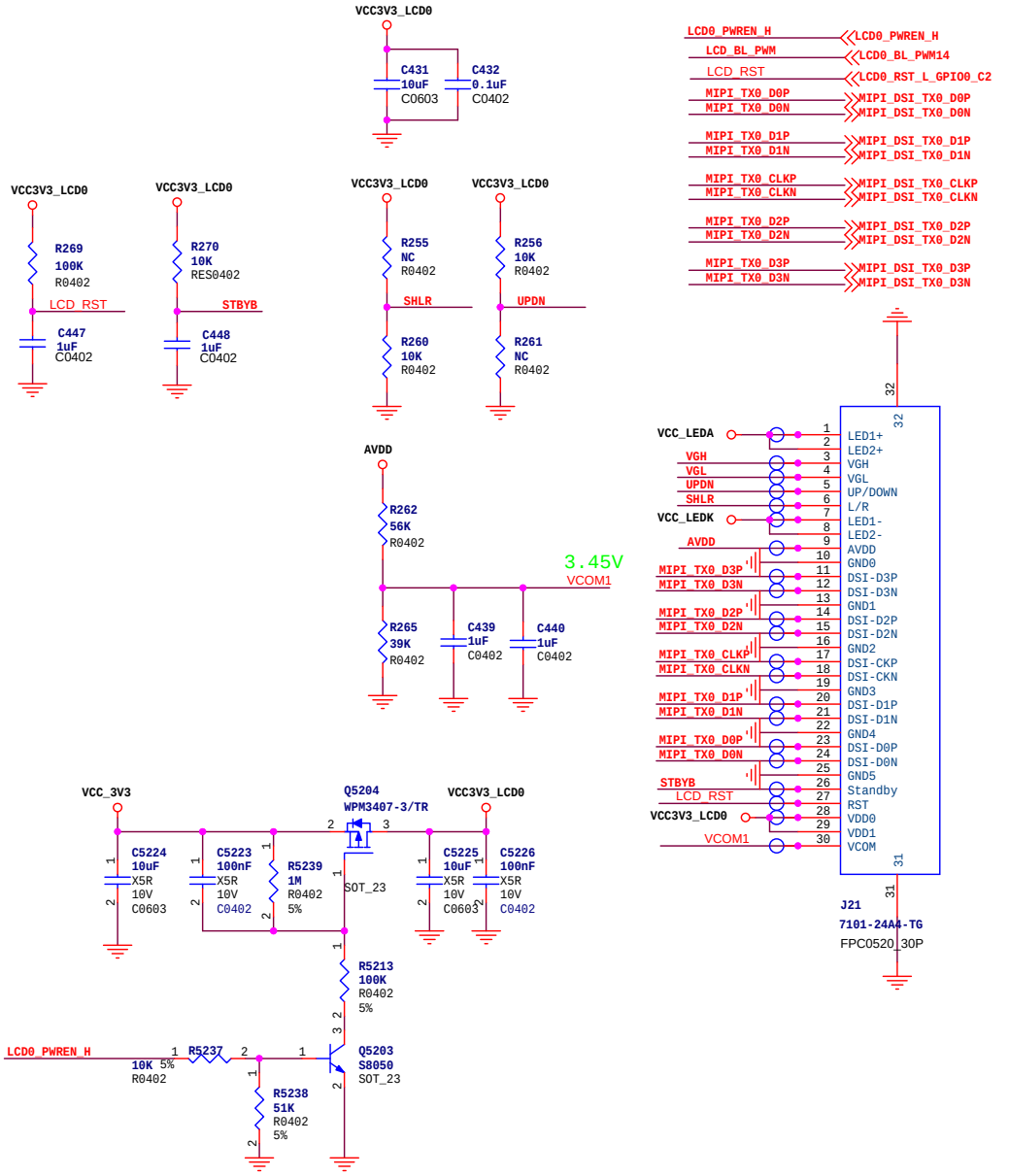
MIPI Panel

BACKLIGHT



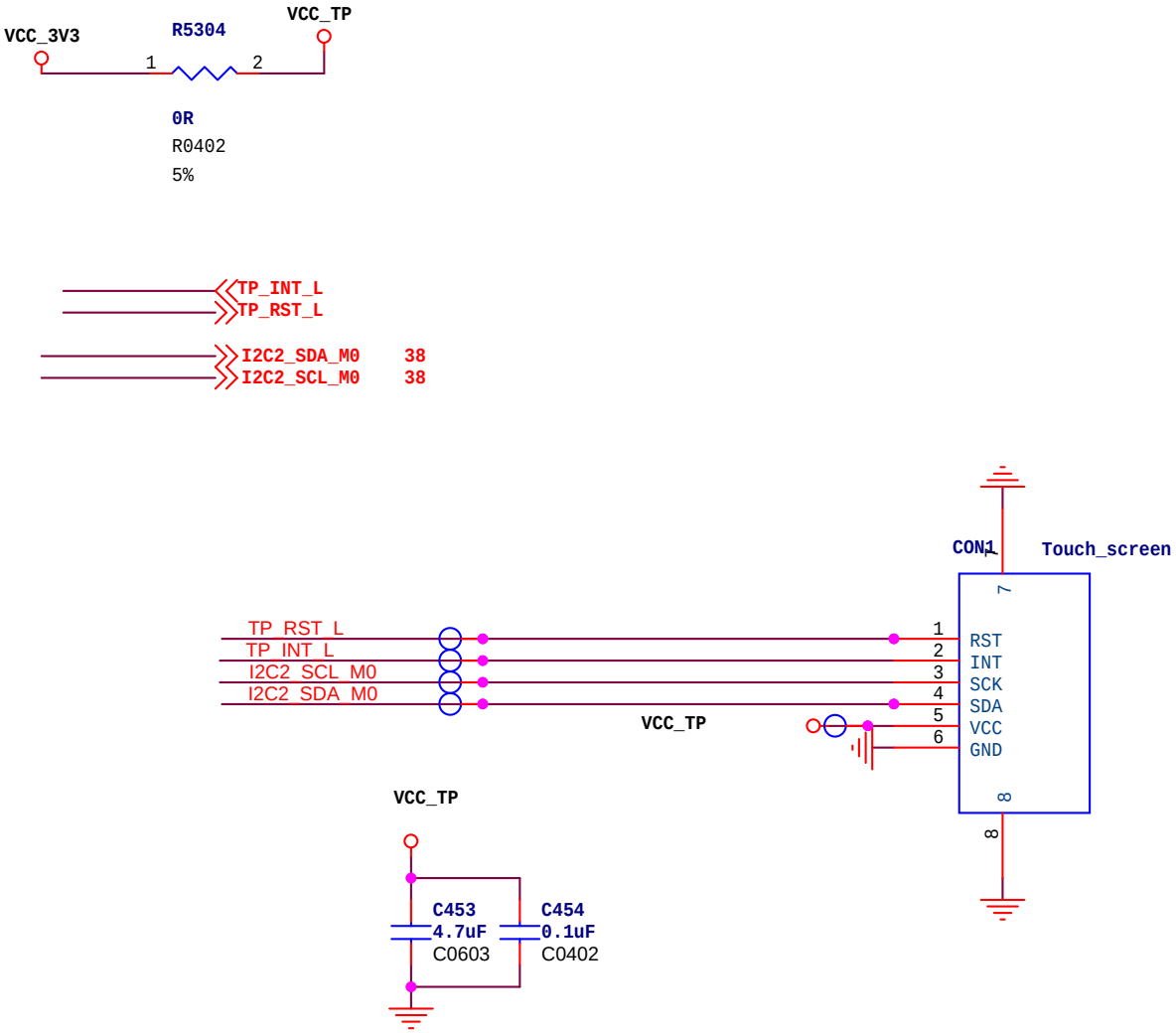
biasing circuit



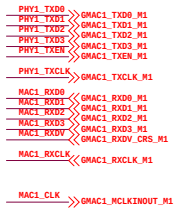


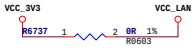
PINE64	PINE64	
Title	Quartz64 Model-A Schematic 20210427	
Size: B	Document Number: LCD MIPI	Rev: V2.0
Date:	Sheet 33 of	

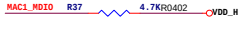
Touch Panel connector

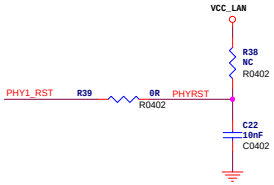


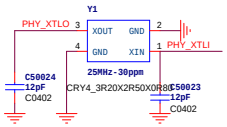
PINE64	PINE64	
Title	Quartz64 Model-A Schematic 20210427	
Size: A	Document Number: TP PORT	Rev: V2.0
Date:	Sheet 34 of	



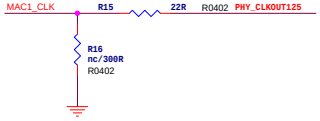


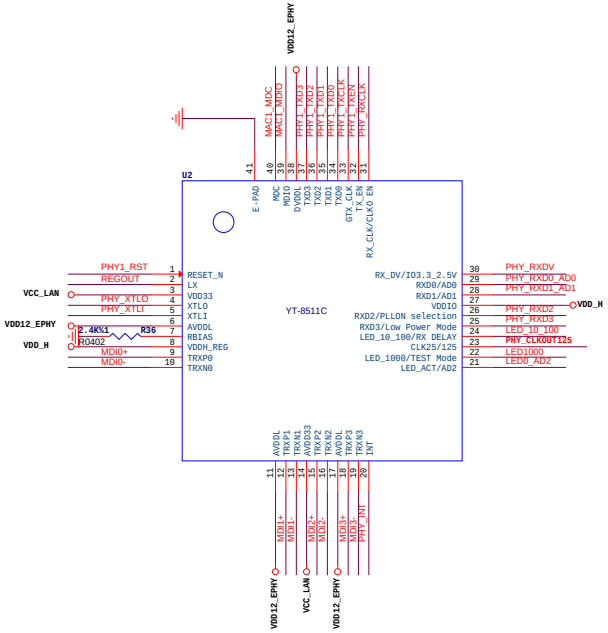


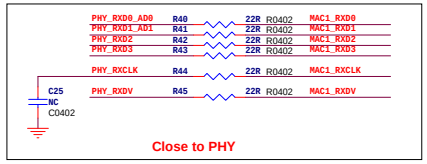




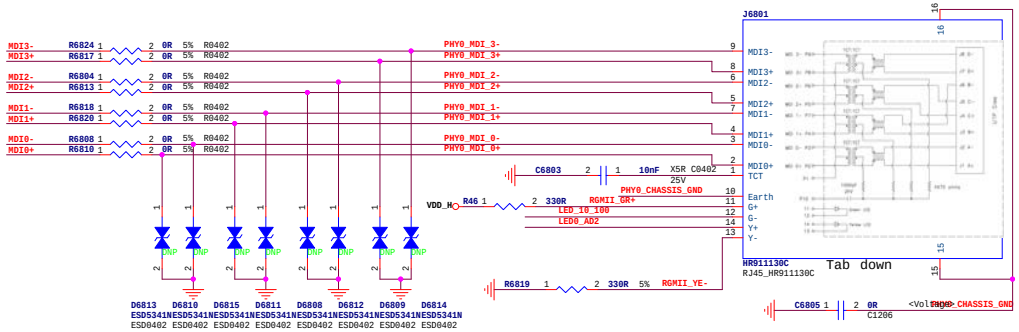
If use external clock
then the XTAL2 need
connect to GND for RTL8211E.





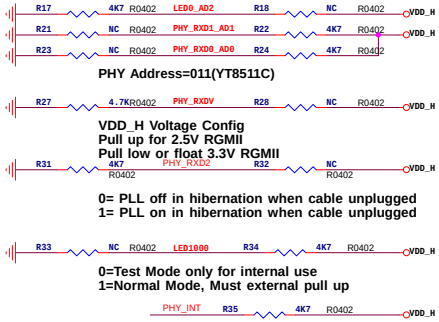


Close to PHY



HR915330CE: -40~85

POWER ON STRAPPING PIN



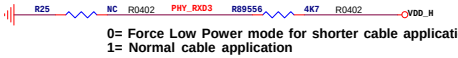
PHY Address=011(YT8511C)

VDD_H Voltage Config
Pull up for 2.5V RGMII
Pull low or float 3.3V RGMII

0= PLL off in hibernation when cable unplugged
1= PLL on in hibernation when cable unplugged

0=Test Mode only for internal use
1=Normal Mode, Must external pull up

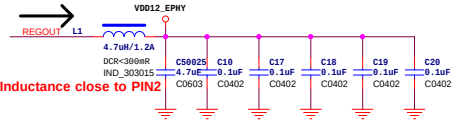
0= clk 25m output enable
1= clk 25m output disable



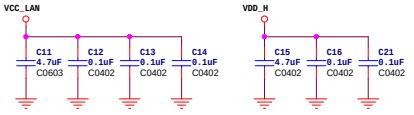
0= Force Low Power mode for shorter cable application
1= Normal cable application

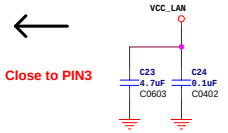
Without RX Delay 1.8ns
0= RXC delay disable
1= RXC delay enable
Equivalent to register ext Reg0x0C Bit0;
Registers take precedence over external hardware configurations

TX delay none hardware configuration PIN
ext Reg0x0C Bit7:4 (default 0101)
tx delay= N*150-350 ps (N= Bit7:4 a decimal value)



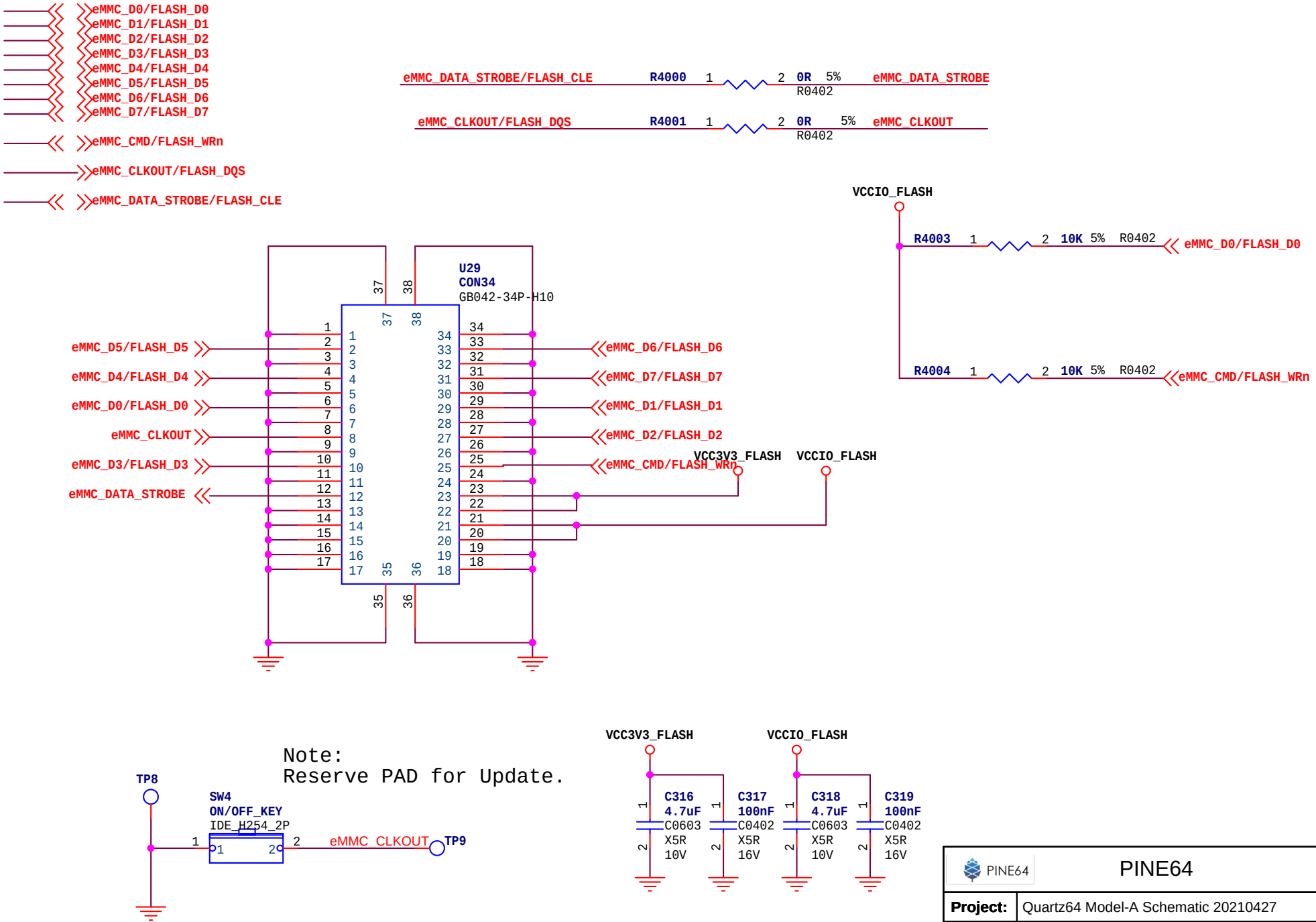
Inductance close to PIN2





Close to PIN3

PINE64	PINE64
Title: 1000M-PHY	
File:	REV: V2.0
Create Date: Monday, April 12, 2021	Page Num: 37
Modify Date: Friday, April 16, 2021	Page Total: 43



PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	Flash eMMC Flash				
Date:	Wednesday, November 25, 2020			Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	40 of 99

PCIe2.0 x 1 (x4 Slot)

PCIE20_TXP 15
PCIE20_TXN 15

PCIE20_RXP 15
PCIE20_RXN 15

PCIE20_REFCLKP 15
PCIE20_REFCLKN 15

PCIE20_CLKREQn_M2 20
PCIE20_WAKEn_M2 20
PCIE20_PERSTn_M2 20

Option

PCIE20_PRSNT_L_GPIO0_A6 19

PCIE_PWREN_H_GPIO0_C2 13

10W Slot: 12V 0.5Amax
25W Slot: 12V 2.1Amax
25W Slot: 12V 5.5Amax
3.3V 3Amax
3.3V 3Amax
3.3V 3Amax
3.3Vaux 0.375Amax

U8200
PCIe-SMT-64PIN
PCIE64_X4_SMT

VCC12V_PCIE	B1	+12V_1	PRSNT1#	A1	
	B2	+12V_2	+12V_4	A3	
	B3	+12V_3	+12V_5	A4	VCC12V_PCIE
	B4	GND_B4	GND_A4	A5	
	B5	SMCLK	JTAG_TCK	A6	
	B6	SMDAT	JTAG_TDI	A7	
	B7	GND_B7	JTAG_TDO	A8	
VCC3V3_PCIE	B8	+3.3V_1	JTAG_TMS	A9	
	B9	JTAG_TRST	+3.3V_2	A10	VCC3V3_PCIE
PCIE20_WAKEn_3V3_L	B10	3.3VAUX	+3.3V_3	A11	PCIE20_PERSTn_3V3_L
	B11	WAKE#	PERST#		
PCIE20_CLKREQn_3V3_L	B12	RSVD_B12	GND_A12	A12	
PCIE20_TXP C8204 100nF C0201 X5R 10V PCIE20_TXP_C	B13	GND_B13	REFCLK+	A13	PCIE20_REFCLKP_C
PCIE20_TXN C8206 100nF C0201 X5R 10V PCIE20_TXN_C	B14	PETp0	REFCLK-	A14	PCIE20_REFCLKN_C
	B15	PETn0	GND_A15	A15	
	B16	GND_B16	PERp0	A16	PCIE20_RXP
	B17	PRSNT2#_1	PERn0	A17	PCIE20_RXN
	B18	GND_B18	GND_A18	A18	
	B19	PETp1	RSVD_A19	A19	
	B20	PETn1	GND_A20	A20	
	B21	GND_B21	PERp1	A21	
	B22	GND_B22	PERn1	A22	
	B23	PETp2	GND_A23	A23	
	B24	PETn2	GND_A24	A24	
	B25	GND_B25	PERp2	A25	
	B26	GND_B26	PERn2	A26	
	B27	PETp3	GND_A27	A27	
	B28	PETn3	GND_A28	A28	
	B29	GND_B29	PERp3	A29	
	B30	RSVD_B30	PERn3	A30	
	B31	PRSNT2#_2	GND_A31	A31	
	B32	GND_B32	RSVD_A32	A32	

X1
X4
PCIE20_PRSNT_3V3_L
Hot-plug

VCC12V_PCIE
C8200 10uF X5R 25V C1206
C8201 100nF X5R 25V C0402

VCC3V3_PCIE
C8208 22uF X5R 6.3V C0805
C8209 100nF X5R 10V C0402

VCC3V3_PCIE
C8212 22uF X5R 6.3V C0805
C8213 100nF X5R 10V C0402

VCCIO_ACODEC 3.3V default PCIE20_CLKREQn_M2 R8200 0R 5% R0402 PCIE20_CLKREQn_3V3_L
VCCIO_ACODEC 3.3V default PCIE20_WAKEn_M2 R8201 0R 5% R0402 PCIE20_WAKEn_3V3_L
VCCIO_ACODEC 3.3V default PCIE20_PERSTn_M2 R8202 0R 5% R0402 PCIE20_PERSTn_3V3_L
3.3V
VCCIO_ACODEC 3.3V default PCIE20_PRSNT_L_GPIO0_A6 R8204 0R 5% R0402 PCIE20_PRSNT_3V3_L

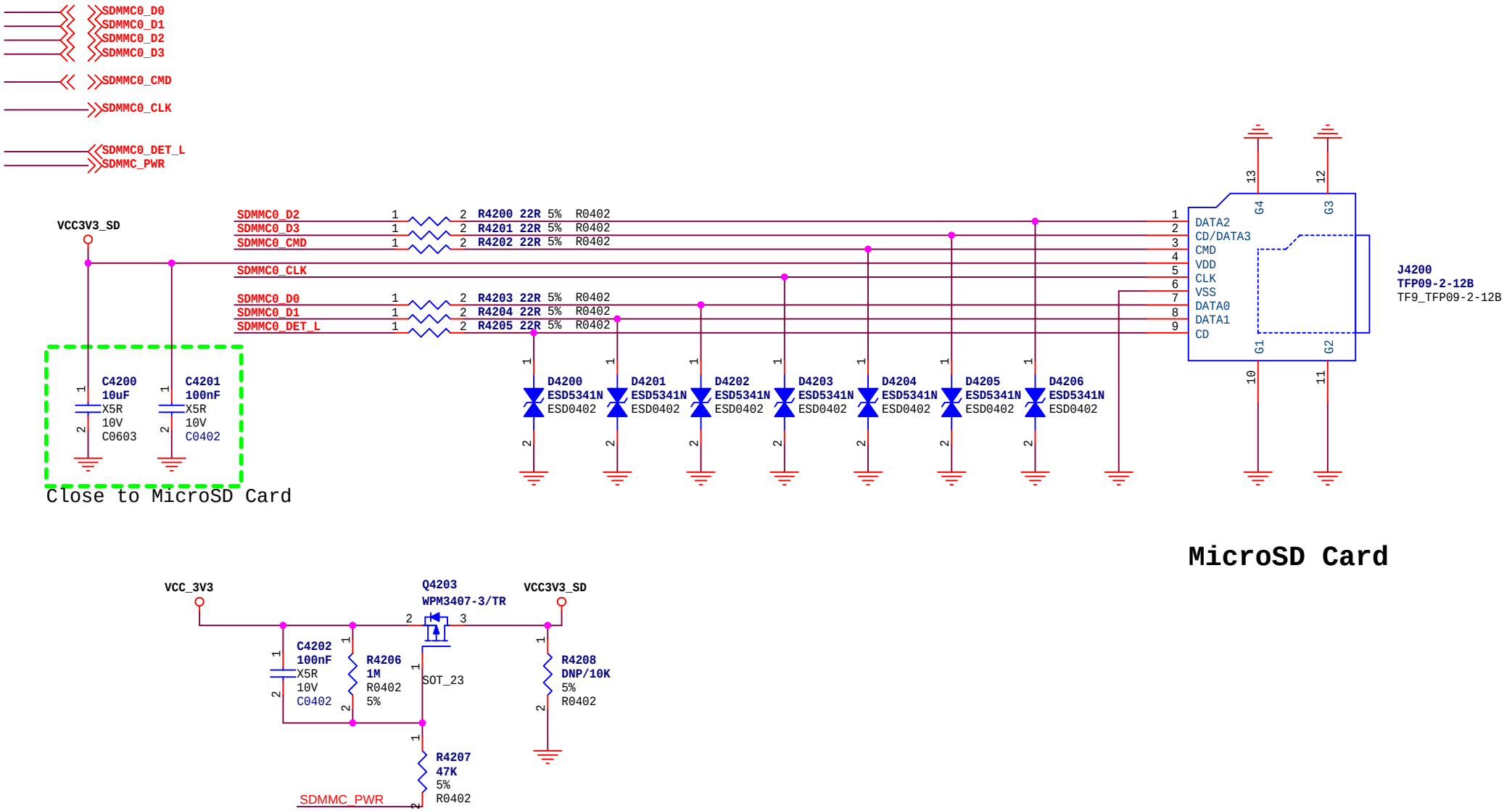
PCIE20_REFCLKP R8210 0R 5% R0201 PCIE20_REFCLKP_C
PCIE20_REFCLKN R8211 0R 5% R0201 PCIE20_REFCLKN_C

Clock --> PCIE2.0 CON

VCC12V_DCIN
Q8200 WPM3407-3/TR SOT_23
R8246 0.02R 1% R0805
VCC12V_PCIE
C8228 10uF X5R 25V C1206
C8229 100nF X5R 25V C0402
R8248 100K R0402 5%
C8230 10uF X5R 25V C1206
C8231 100nF X5R 25V C0402
R8252 10K R0402 5%
3.3V
PCIE_PWREN_H_GPIO0_C2
R8254 10K 5% R0402
Q8201 S8050 SOT_23
R8255 51K R0402 5%

VCC12V_DCIN
C8232 10uF X5R 25V C1206
C8233 100nF X5R 25V C0402
4.5V<VIN<18V
R8249 10K 5% R0402
C8235 100nF X5R 10V C0402
PCIE_PWREN_H_GPIO0_C2
R8256 DNP R0402
U8204 SY8113B SOT_23_6
VIN LX GND BS EN FB/OUT
C8227 100nF X5R 25V C0402
L8200 4.7uH IND_606045
FB=0.6V
VCC3V3_PCIE_P
C8234 22pF C0G 50V C0402
R8250 232K 1% R0402
R8253 49.9K 1% R0402
VCC3V3_PCIE_P
C8236 120uF SVPF 20V E_C6
C8237 10uF X5R 10V C0603
C8238 100nF X5R 10V C0402
R8247 0.02R 1% R0805
R8251 DNP R0402
VCC3V3_PCIE

PINE64	PINE64
Project:	Quartz64 Model-A Schematic 20210427
File:	PCIe Interface
Date:	Wednesday, November 25, 2020
Rev:	V2.0
Designed by:	Daniel.J
Reviewed by:	Default
Sheet:	41 of 48



PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	Flash MicroSD Card				
Date:	Wednesday, November 25, 2020			Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	42 of 99

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
HDMITX_SCL
HDMITX_SDA
HDMITX_CEC_M0
HDMI_TX_HPDIN

VCC5V_MIDU
R5011 1 DNP 2 NC/0R 5% R0603
VCC5V_HDMI
C5001 1uF X5R 10V C0402
U5002
IN VOUT GND EN OCB
SY6280AAC SOT_23_5
VCC_3V3
R5012 100K 5% R0402
C5002 1uF X5R 10V C0402
D5002 B5819W SOD_123
VCC5V_HDMI_TX
R5014 1 DNP 2 NC/0R 5% R0402
R5013 10K 5% R0402

Cj<=0.4pF

HDMI TX DDC

VCC5V_HDMI
D5000 B5819WS SOD_323
VCC_3V3
R5000 10K 5% R0402
Q5000 2SK3018 SOT_323
R5001 1.8K 5% R0402
HDMITX_SCL
HDMI_TXDDC_SCL_PORT
VCC_3V3
R5002 10K 5% R0402
Q5001 2SK3018 SOT_323
R5003 1.8K 5% R0402
HDMITX_SDA
HDMI_TXDDC_SDA_PORT

U5000 ESD5304D SON10_2R50X1R00X0R50
U5001 ESD5304D SON10_2R50X1R00X0R50
IO1 IO2 GND IO3 IO4 NC_10 NC_9 NC_7 NC_6
HDMI_TX2P_PORT HDMI_TX2N_PORT HDMI_TX1P_PORT HDMI_TX1N_PORT
HDMI_TX0P_PORT HDMI_TX0N_PORT HDMI_TXCLKP_PORT HDMI_TXCLKN_PORT
HDMI_TX_CEC_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TXDDC_SDA_PORT
HDMI_TX_HPD_PORT
ED5000 ESD5341N ESD0402
ED5001 ESD5341N ESD0402
ED5002 ESD5341N ESD0402
ED5003 ESD5341N ESD0402
VCC5V_HDMI_TX
C5000 1uF X5R 10V C0402

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TX_CEC_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TX_HPD_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
HDMI_TXDDC_SDA_PORT
VCC5V_HDMI_TX
C356 100nF C0402 X5R 16V
C357 1uF C0402 X5R 10V
J14
HDMI_A
HDMI-14_5X11_55-23P

HDMI TX CEC

VCC_3V3
BAT60BE6327
Cj=30pF max
D5001 B5819WS SOD_323
Cj=120pF max
R5006 27K 5% R0402
HDMITX_CEC_M0 R5008 1 2 22R 5% R0402 HDMI_TX_CEC_PORT

HDMI TX HPD

HDMI_TX_HPDIN R5004 1 2 1K 5% R0402 HDMI_TX_HPD_PORT
R5007 100K 5% R0402

PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	VO Digital Video Out				
Date:	Wednesday, November 25, 2020			Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	50 of 99

SDIO WIFI/BT Module-1T1R

SDMMC1_D0
SDMMC1_D1
SDMMC1_D2
SDMMC1_D3
SDMMC1_CMD
SDMMC1_CLK

WIFI_REG_ON_H_GPIO2_C2
WIFI_WAKE_HOST_H_GPIO2_C3

UART1_RX_M0
UART1_TX_M0
UART1_RTSn_M0
UART1_CTSn_M0

BT_REG_ON_H_GPIO2_B7
BT_WAKE_HOST_H_GPIO2_C0
HOST_WAKE_BT_H_GPIO2_C1

PMIC_32KOUT_WIFI

U30
CON34
DIP_2_0_2X7

SDMMC1_CLK	1	2	SDMMC1_D0
	3	4	SDMMC1_D1
SDMMC1_CMD	5	6	SDMMC1_D2
WIFI_REG_ON_H_GPIO2_C2	7	8	SDMMC1_D3
WIFI_WAKE_HOST_H_GPIO2_C3	9	10	PMIC_32KOUT_WIFI
	11	12	
VCCIO_WL	13	14	VCC_WL

U31
CON34
DIP_2_0_2X8

	1	2	UART1_RX_M0
	3	4	UART1_TX_M0
	5	6	UART1_CTSn_M0
	7	8	UART1_RTSn_M0
BT_WAKE_HOST_H_GPIO2_C0	9	10	
BT_REG_ON_H_GPIO2_B7	11	12	HOST_WAKE_BT_H_GPIO2_C1
	13	14	VCC_WL
	15	16	

Note:
VBAT voltage range:3.0V~4.8V,
Supply current at least 400mA

VCC_WL
VCC_SYS
R9128 0R R0603 5%
VCC_3V3
Q6102 DNP/WPM2026 SOT23
C6113 1uF X5R 6.3V C0402
C6114 100nF X5R 16V C0402
R6127 1M 5% R0402
C6111 10uF X5R 6.3V C0603
C6112 100nF X5R 16V C0402
R6126 100K 5% R0402
R6128 10K R0402 5%
WIFI_PWR
Q5205 S8050 SOT_23
R6129 47K R0402 5%

PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	Wifi/BT SDIO Module Connection				
Date:	Wednesday, November 25, 2020			Rev:	V2.0
Designed by:	Linus.Lin	Reviewed by:		Sheet:	61 of 99

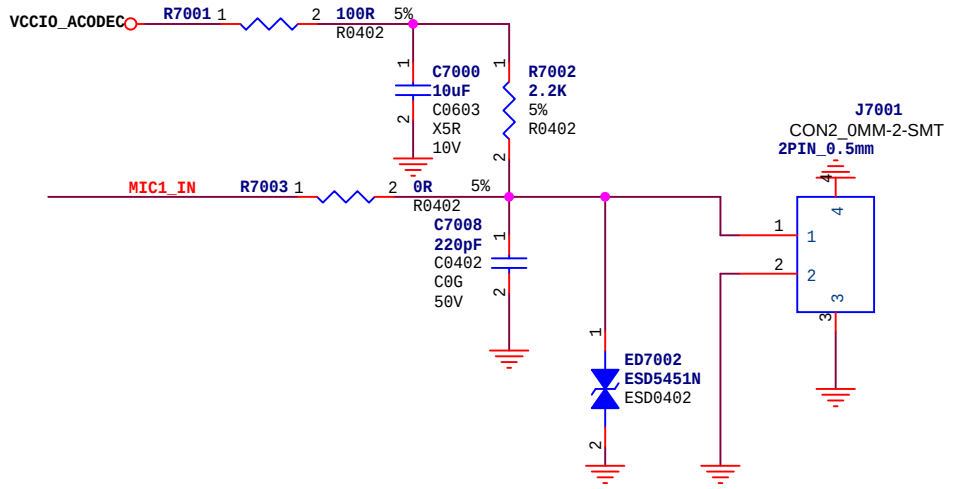
HPL_OUT
HP_SNS
HPR_OUT

SPKN_OUT
SPKP_OUT

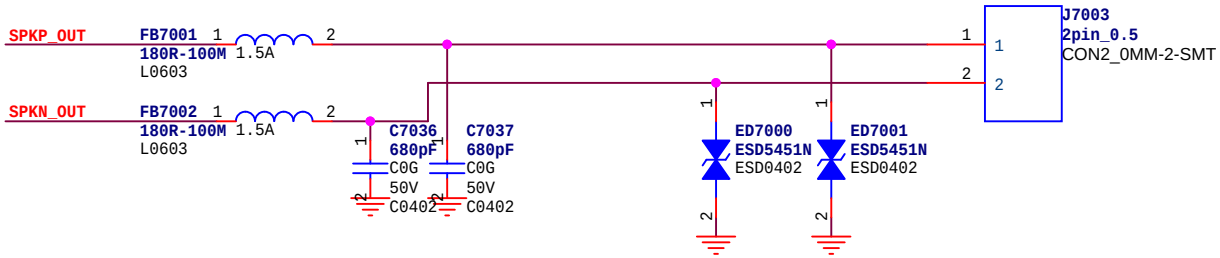
MIC1_IN
MIC2_IN

HP_DET_L_GPIO3_A1
SARADC_VIN2_HP_HOOK

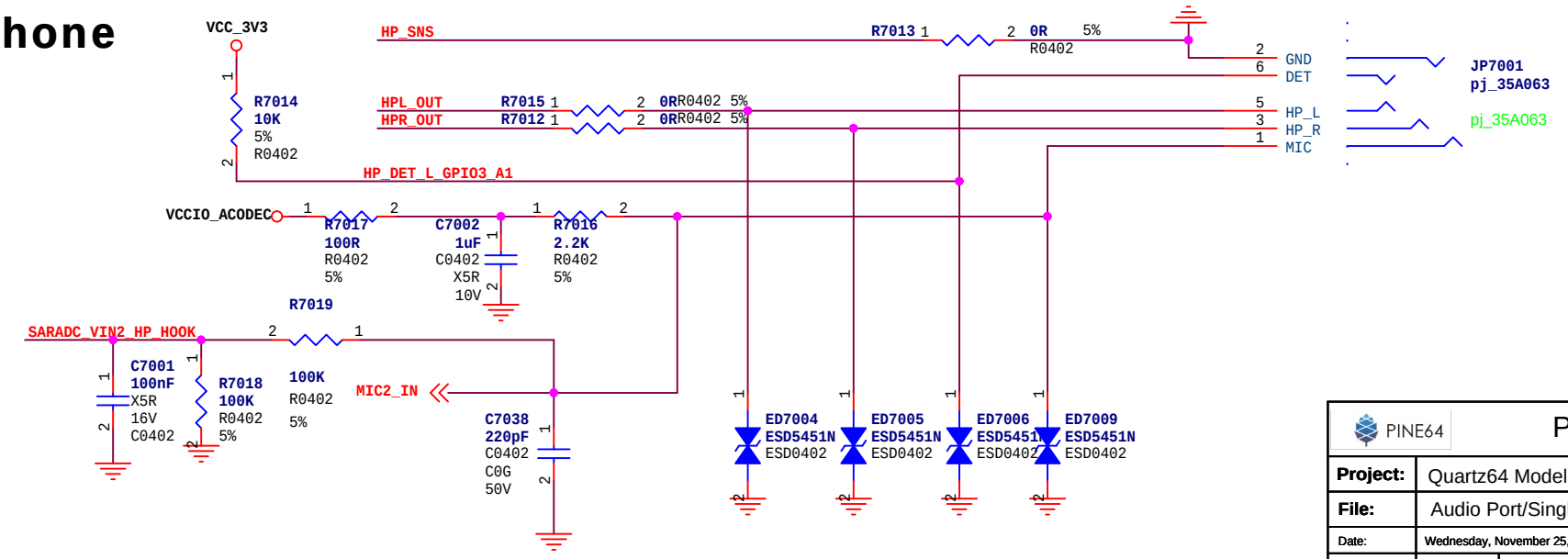
MIC



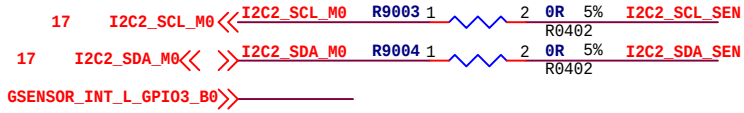
SPK



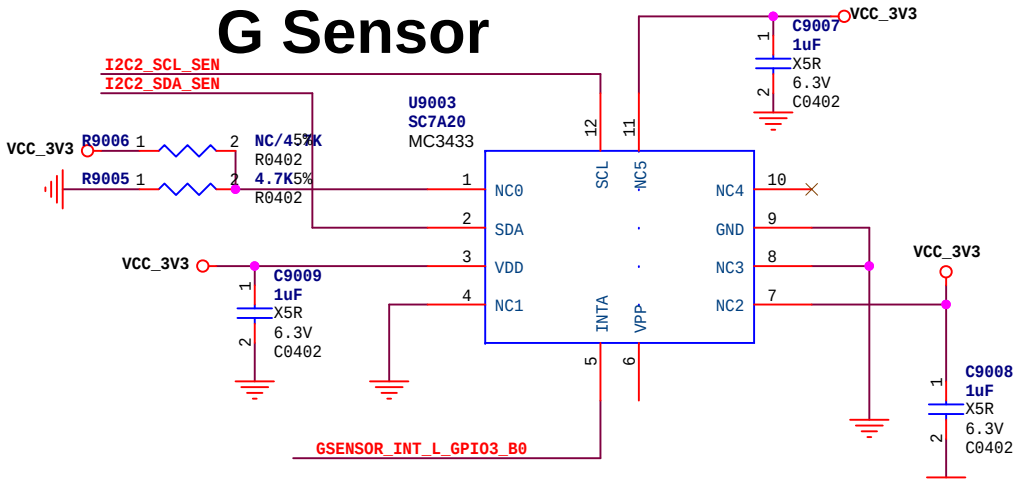
Headphone



PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	Audio Port/Single Speaker				
Date:	Wednesday, November 25, 2020			Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	70 of 99



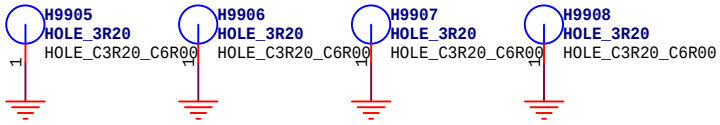
G Sensor



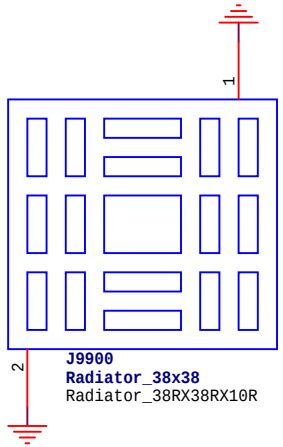
PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	Sensor				
Date:	Wednesday, November 25, 2020			Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	90 of 99

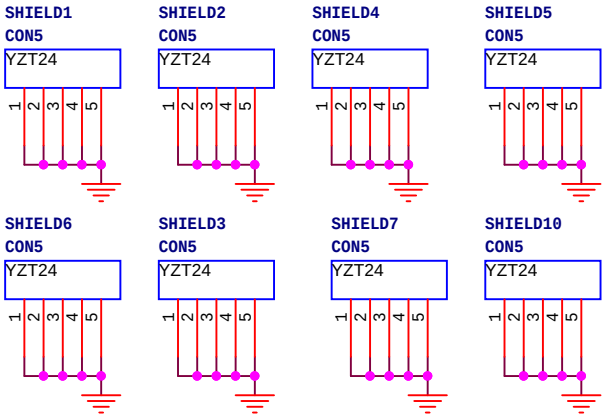
Page of Accessories

PCB Mark Point



Heatsink





Heatsink

When use socket,
NO Heatsink holes is reserved.

PINE64	PINE64				
Project:	Quartz64 Model-A Schematic 20210427				
File:	Mark/Hole/Heatsink				
Date:	Wednesday, November 25, 2020			Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	99 of 99