Version: 1.0

TECHNICAL SPECIFICATION

MODEL NO: ED103TC2

The content of this information is subject to be changed without notice.

Please contact E Ink or its agent for further information.

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐E Ink's Confirmation

Approved By 王昱翰 5/14 19'

Confirmed By 蔡毓琦 5/14 19'

Prepared By 胡亚揚 5/14

Revision History

Rev.	Issued Date	Revised Contents
1.0	2019-05-08	V1.0 Version

TECHNICAL SPECIFICATION

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1. General Description

ED103TC2 is a reflective electrophoretic E Ink® display module based on active matrix TFT substrate. It has 10.3" active area with 1404 x 1872 pixels, the display is capable to display images at 2-16 gray levels (1-4 bits) depending on the display controller and the associated waveform file it used.

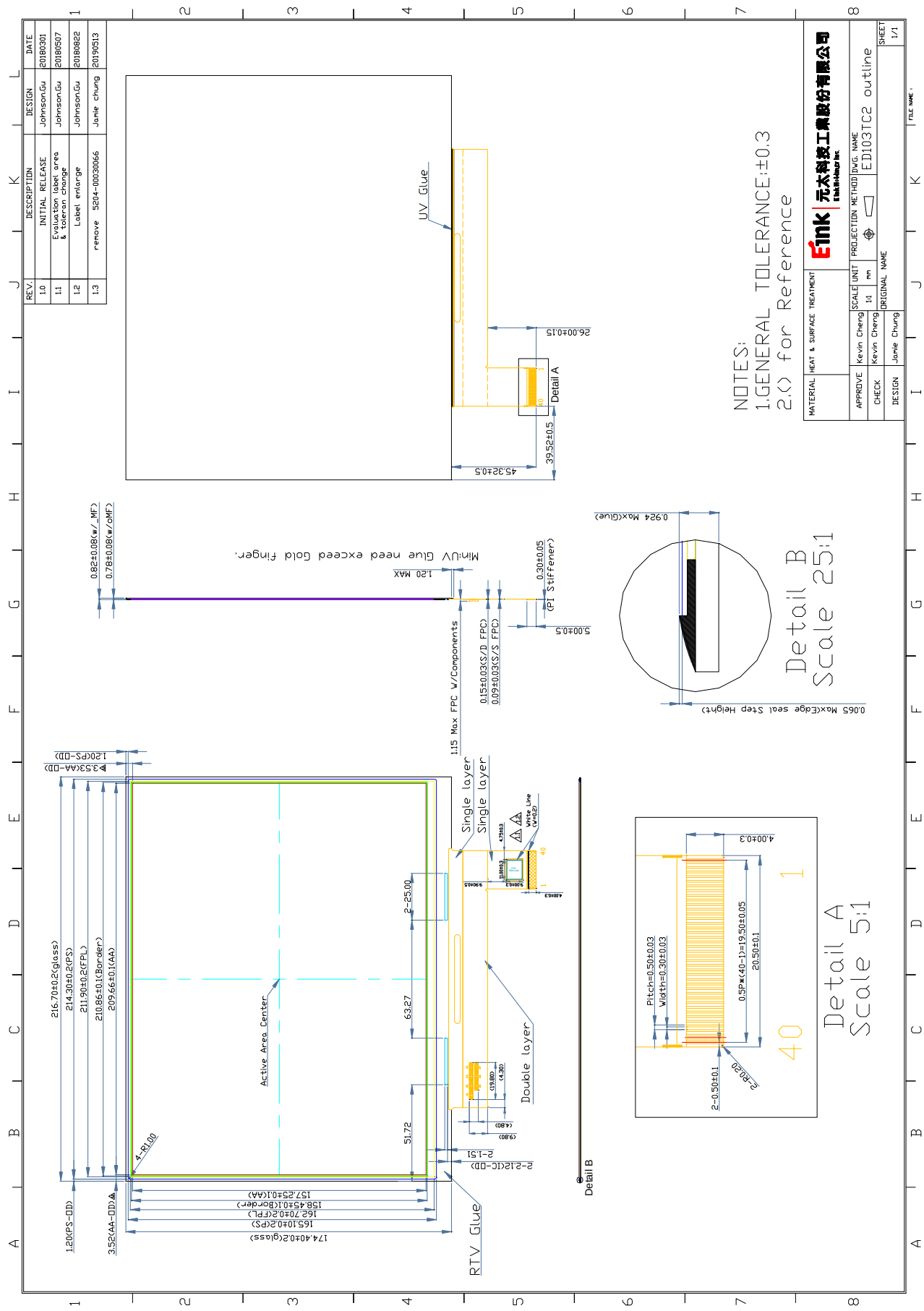
2. Features

- High contrast reflective/electrophoretic technology
- 1404 x 1872 EPD display
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape mode

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	10.3	inch	
Display Resolution	1404 (V)×1872 (H)	pixel	
Active Area	157.25(V)×209.66(H)	mm	
Pixel Pitch	112(V)×112(H)	μm	
Pixel Configuration	Rectangle		
Outline Dimension	174.4(V)×216.7(H)×0.78(D)	mm	
Module Weight	60±7	g	
Number of Gray	16 Grey Level (monochrome)		
Display operating mode	Reflective mode		
Surface treatment	Anti-glare treatment for projective sheet		

4. Mechanical Drawing of EPD Module



5. Input / Output Interface

5.1 Pin Assignment

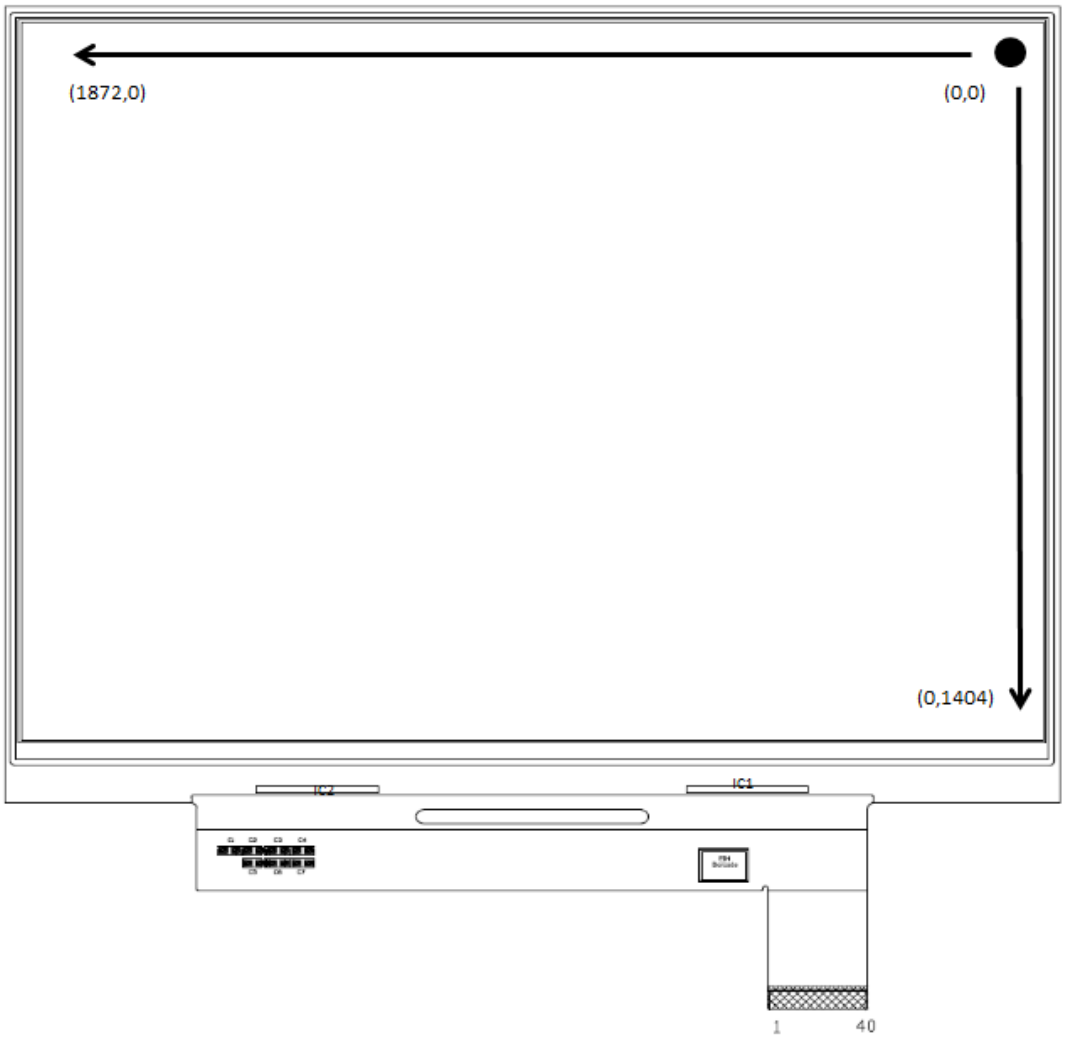
Connector type：196033-40041

Pin #	Signal	Description	Remark
1	VGL	Negative power supply gate driver	
2	NC	NO Connection	
3	VGH	Positive power supply gate driver	
4	NC	NO Connection	
5	VDD	Digital power supply drivers	
6	MODE	Output mode selection gate driver	
7	CKV	Clock gate driver	
8	SPV	Start pulse gate driver	
9	VSS	Ground	
10	VCOM	Common voltage	
11	VDD	Digital power supply drivers	
12	VSS	Ground	
13	XCL	Clock source driver	
14	D0	Data signal source driver	
15	D1	Data signal source driver	
16	D2	Data signal source driver	
17	D3	Data signal source driver	
18	D4	Data signal source driver	
19	D5	Data signal source driver	
20	D6	Data signal source driver	
21	D7	Data signal source driver	
22	VSS	Ground	
23	D8	Data signal source driver	
24	D9	Data signal source driver	
25	D10	Data signal source driver	
26	D11	Data signal source driver	
27	D12	Data signal source driver	
28	D13	Data signal source driver	
29	D14	Data signal source driver	
30	D15	Data signal source driver	
31	XSTL	Start pulse source driver	
32	XLE	Latch enable source driver	
33	XOE	Output enable source driver	
34	TEST	Eink internal test pin	Note1

35	NC	NO Connection	
36	VPOS	Positive power supply source driver	
37	NC	NO Connection	
38	VNEG	Negative power supply source driver	
39	NC	NO Connection	
40	Border	Border connection	

Note1: Please connect to VDD voltage.

5.2 Panel Scan Direction



6. Display Module Electrical Characteristics

6.1 Absolute Maximum Ratings

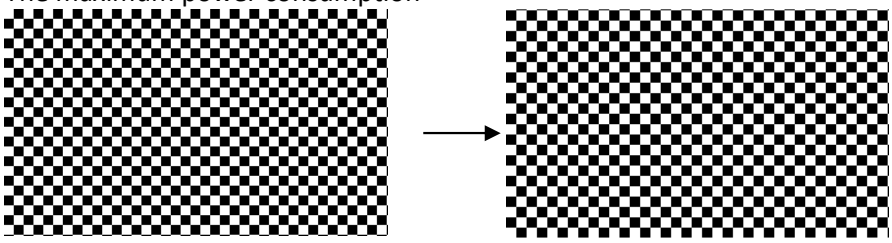
Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +5	V	--
Positive Supply Voltage	V_{POS}	-0.3 to +18	V	--
Negative Supply Voltage	V_{NEG}	+0.3 to -18	V	--
Max .Drive Voltage Range	V_{POS} - V_{NEG}	36	V	--
Supply Voltage	VGH	-0.3 to VGL+50	V	--
Supply Voltage	VGL	-25 to +0.3	V	--
Supply Range	VGH-VGL	+10 to +50	V	--
Operating Temp. Range	TOTR	0 to +50	℃	--
Storage Temperature	TSTG	-25 to +70	℃	--

6.2 Display Module DC Characteristics

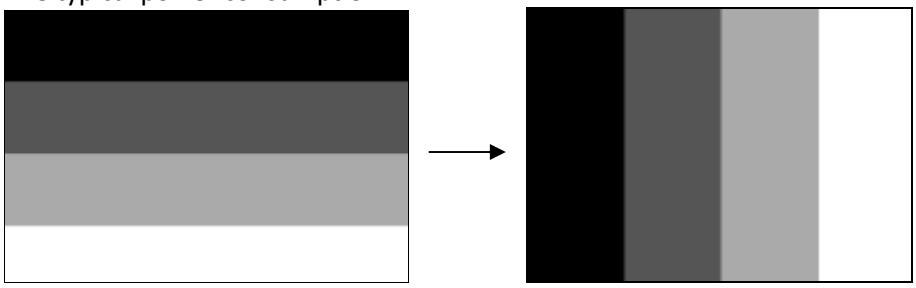
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	V_{SS}		-	0	-	V
Logic Voltage supply	V_{DD}		3.0	3.3	3.6	V
	I_{VDD}	V_{DD}=3.3V	-	3.6	9.1	mA
Gate Negative supply	VGL		-21	-20	-19	V
	I_{GL}	V_{GL} =-20V	-	11.3	28.78	mA
Gate Positive supply	VGH		27	28	29	V
	I_{GH}	V_{GH} = 28V	-	1.52	1.89	mA
Source Negative supply	V_{NEG}		-15.4	-15	-14.6	V
	I_{NEG}	V_{NEG} = -15V	-	4.55	155	mA
Source Positive supply	V_{POS}		14.6	15	15.4	V
	I_{POS}	V_{POS} = 15V	-	2.07	169.44	mA
Border supply	V_{COM}		-	Adjusted	-	V
Asymmetry source	V_{Asym}	V_{POS}+V_{NEG}	-800	0	800	mV
Common voltage	V_{COM}		-	Adjusted	-	V
	I_{COM}		-	13.65	14.4	mA
Panel Power	P		-	379.77	5525.15	mW
Standby power panel	P_{STBY}		-	-	1.22	mW

- The maximum average Currents for power consumption are measured using 85 Hz waveform with following pattern transition: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern . (Note 6-1)
- The Typical power consumption is measured using 85 Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 6-2)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by E Ink.
- Vcom is recommended to be set in the range of assigned value ± 0.1 V
- The maximum I_{COM} inrush current is about 0.8 A

Note6-1
The maximum power consumption



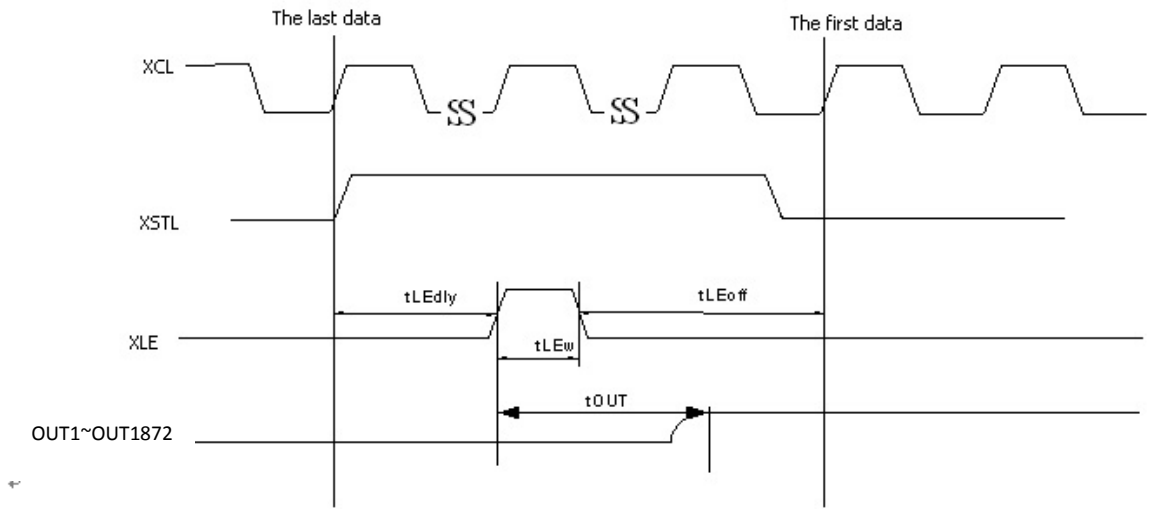
Note6-2
The typical power consumption



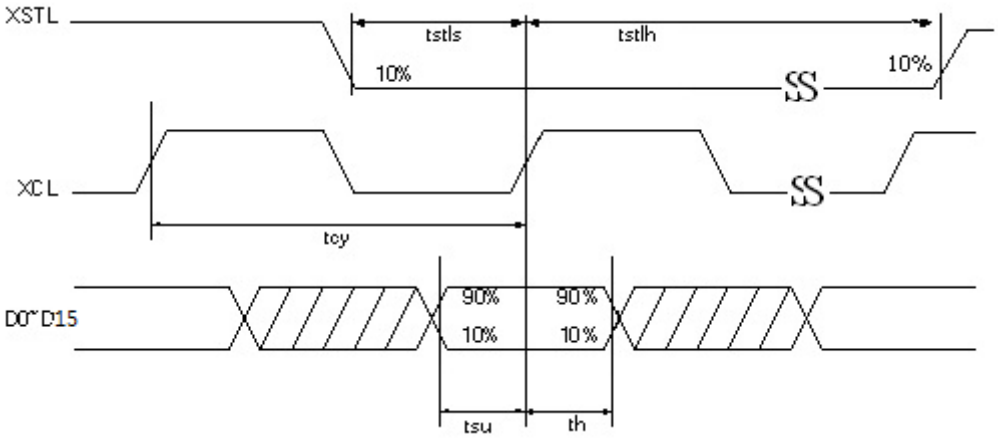
6.3 Display Module AC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fckv	-	-	200	kHz
Minimum “L” clock pulse width	twL	500	-	-	ns
Minimum “H” clock pulse width	twH	500	-	-	ns
Clock rise time	trckv	-	-	100	ns
Clock fall time	tfckv	-	-	100	ns
SPV setup time	tSU	100	-	-	ns
SPV hold time	tH	100	-	-	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock XCL cycle time	tcy	16.67	50	-	ns
D0 .. D7 setup time	tsu	8	-	-	ns
D0 .. D7 hold time	th	8	-	-	ns
XSTL setup time	tstls	0.5*tcy	-	0.8*tcy	ns
XSTL hold time	tstlh	0.5*tcy	-		ns
XLE on delay time	tLEdly	10.5*tcy	-	-	ns
XLE high-level pulse width (When VDD=1.7V to 2.1V)	tLEw	300	-	-	ns
XLE off delay time	tLEoff	200	-	-	ns
Output setting time to +/- 30mV(C_{load}=200pF)	tout	-	-	20	us

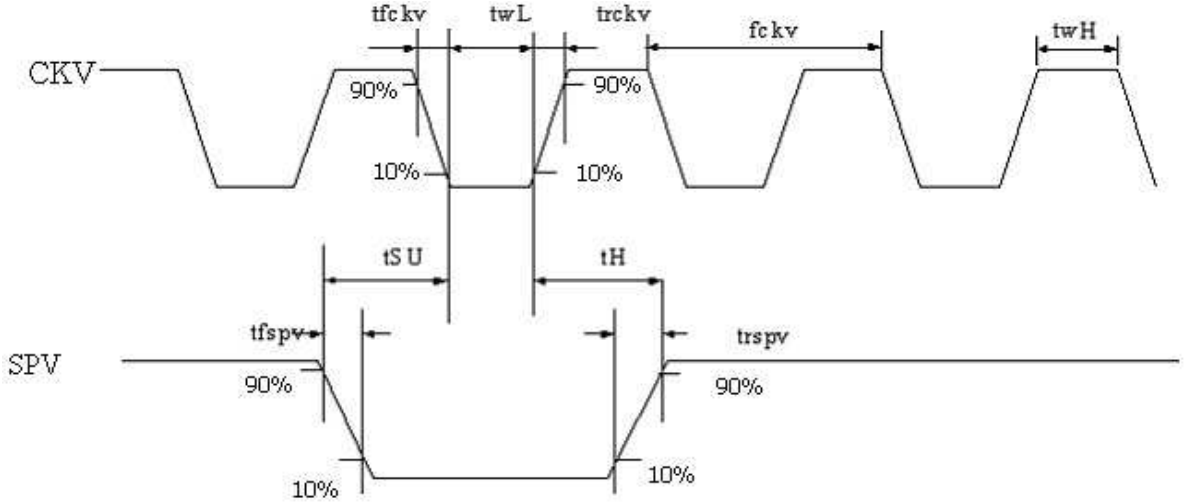
OUTPUT LATCH CONTROL SIGNALS



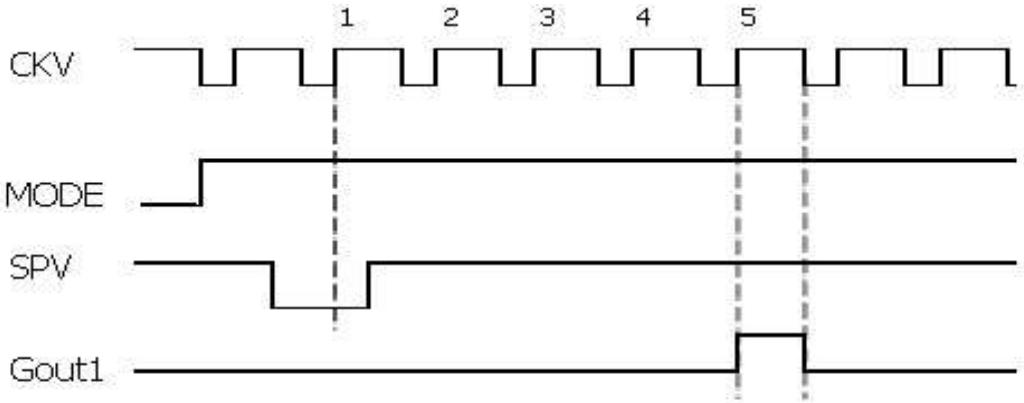
CLOCK & DATA TIMING



CKV & SPV TIMING



GATE OUTPUT TIMING



Note：First gate line on timing

6.4 Refresh Rate

The module is applied at a maximum refresh rate of 85 Hz.

	Min	Max
Refresh Rate	-	85 Hz

6.5 Controller Timing

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, that in this mode LGON follows GDCK timing.

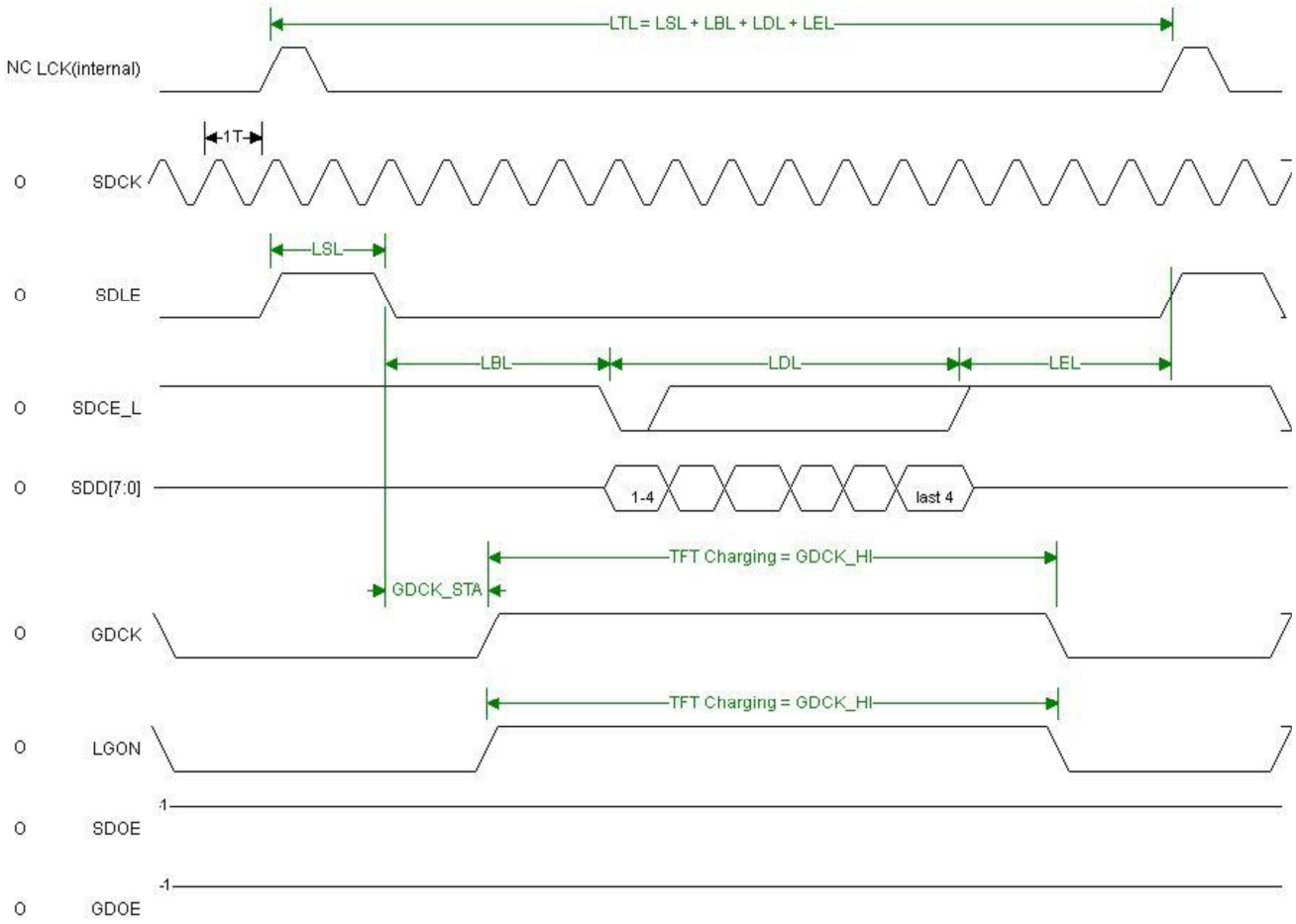


Figure 1. Line Timing in Mode 3

Note 1: LCK is an internal signal and it is shown for reference only.

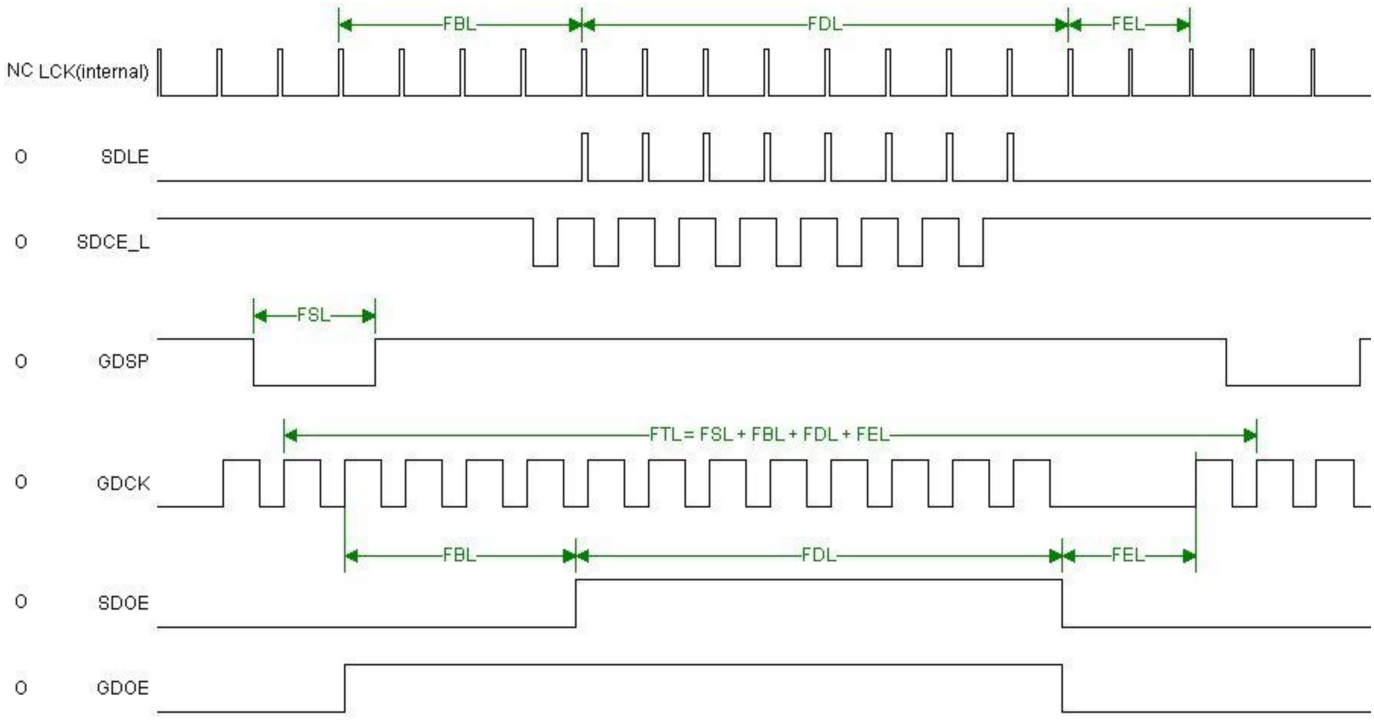


Figure 2 Frame Timing in Mode 3

Timing Parameters Table

Mode	3	**Resolution** 1872x1404				
SDCK [MHz]	33.33					
Pixels Per SDCK	8					
Line	**LSL**	**LBL**	**LDL**	**LEL**	**GDCK_STA**	**LGONL**
Parameters[SDCK]	18	17	234	7	34	192
Line	-	-	-	-	-	-
Parameters[us]	0.54	0.51	7.02	0.21	1.02	5.76
Frame	**FSL**	**FBL**	**FDL**	**FEL**	**-**	**FR [Hz]**
Parameters [lines]	1	4	1404	12	-	84.99
Frame	-	-	-	-	-	-
Parameters [us]	8.28	32.12	11625.12	99.36	-	-

Note 1: For parameters definition, see Appendix- EPD Panel Timing

Note 2: For Isis Controller GDCK_STA and LGONL are not settable parameters; GDCK_STA = LBL, LGONL = LDL+0.5

Note 3: For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL

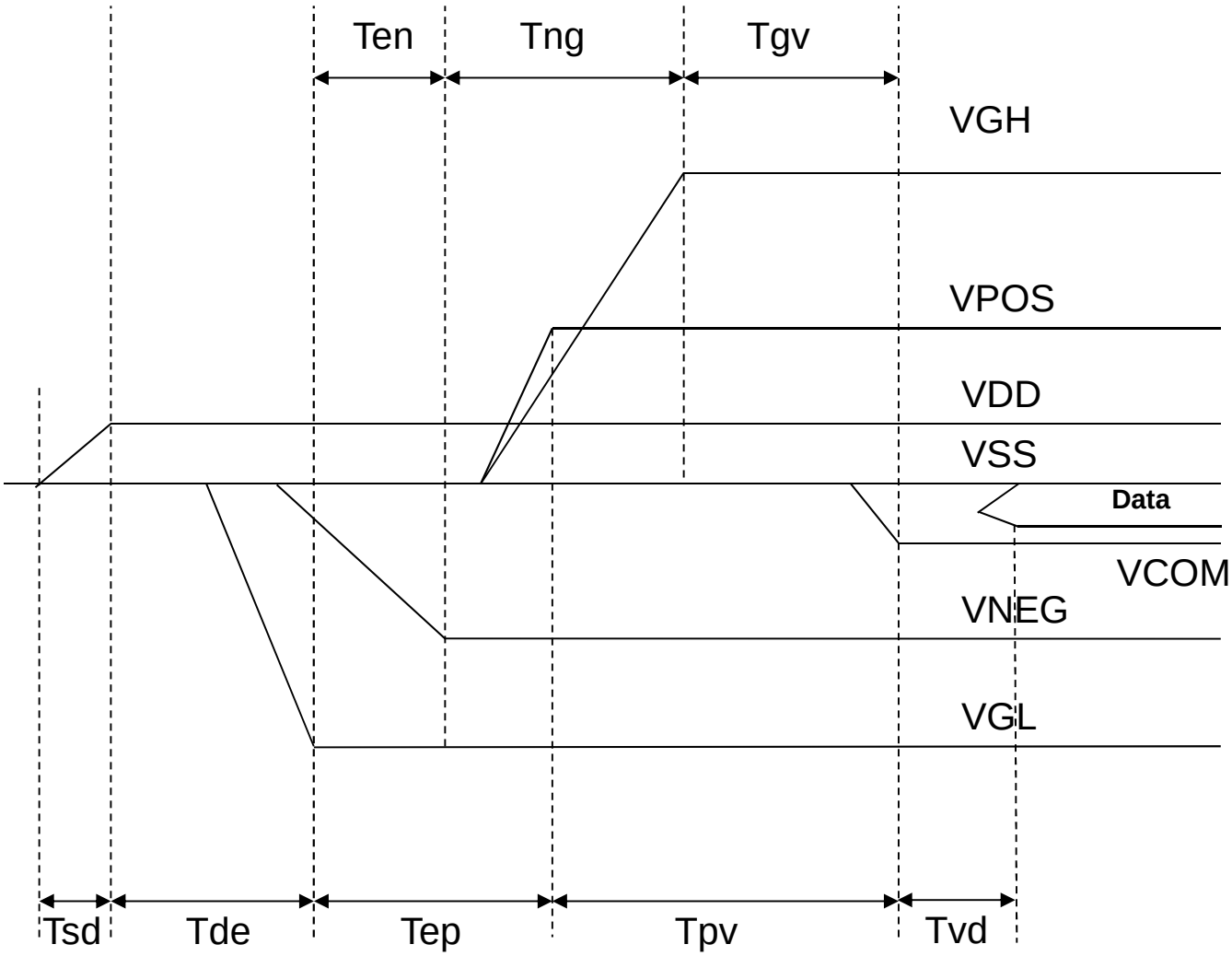
Note 4: SDOE = XOE, SDCE_L = XSTL, SDCK = XCL, GDCK = CKV, GDOE = MODE 1, GDSP = SPV

7. Power Sequence

Power Rails must be sequenced in the following order：

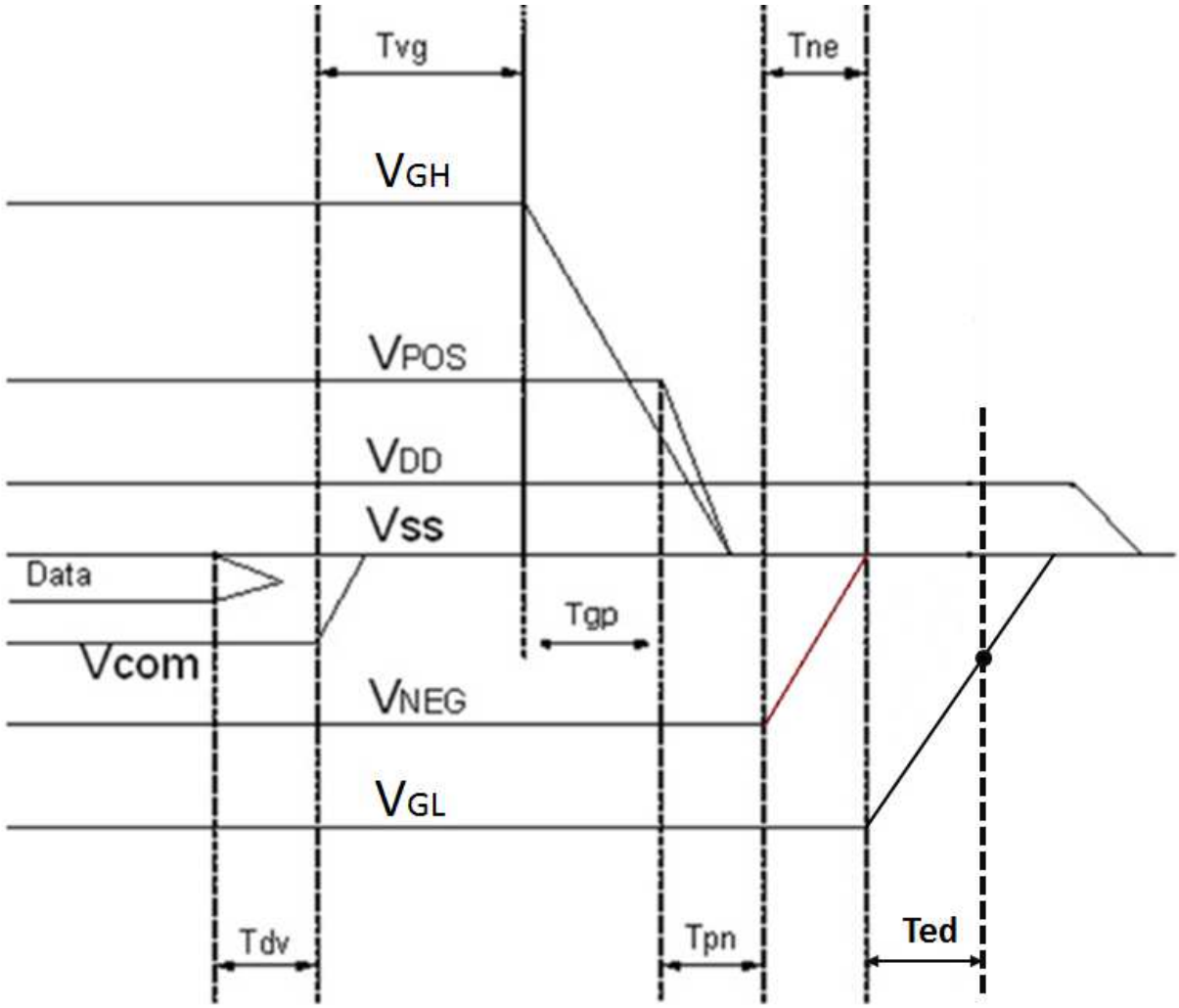
1. VSS → VDD → VNEG → VPOS (Source driver) → VCOM
2. VSS → VDD → VGL → VGH (Gate driver)
3. Fiti Power PMIC FP9928A can meet Power on sequence

POWER ON



	Min	Max
Tsd	30us	-
Tde	100us	-
Tep	1000us	-
Tpv	100us	-
Tvd	100us	-
Ten	0us	-
Tng	1000us	-
Tgv	100us	-

POWER OFF



	Min	Max	Remark
Tdv	100µs	-	-
Tvg	0µs	-	-
Tgp	0µs	-	-
Tpn	0µs	-	-
Tne	0µs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt

Note 8-1：Supply voltages decay through pull-down resistors.

Note 8-2 : Begin to turn off VGL power after VNEG and VPOS are completely or almost discharged to GND state.

Note 8-3：VGL must remain negative of Vcom during decay period

8. Optical Characteristics

8.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

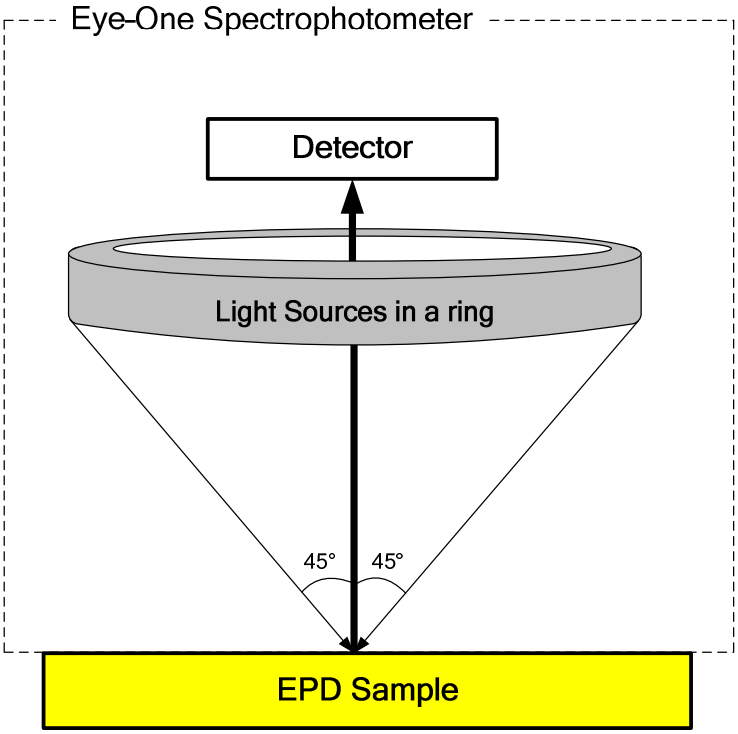
T = 25°C

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	35	43	-	%	Note 9-1
Gn	N_{th} Grey Level	-	-	DS+(WS-DS)×n /(m-1)	-	L*	-
CR	Contrast Ratio	-	10	14	-		-

WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WS
m:4、8、16 when 2、3、4 bits mode
Note 9-1: Luminance meter :Eye – One Pro Spectrophotometer.

8.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd): CR = Rl / Rd



8.3 Reflection Ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Handling, Safety and Environmental Requirements and Remark

Warning
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	This data sheet contains preliminary product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the	

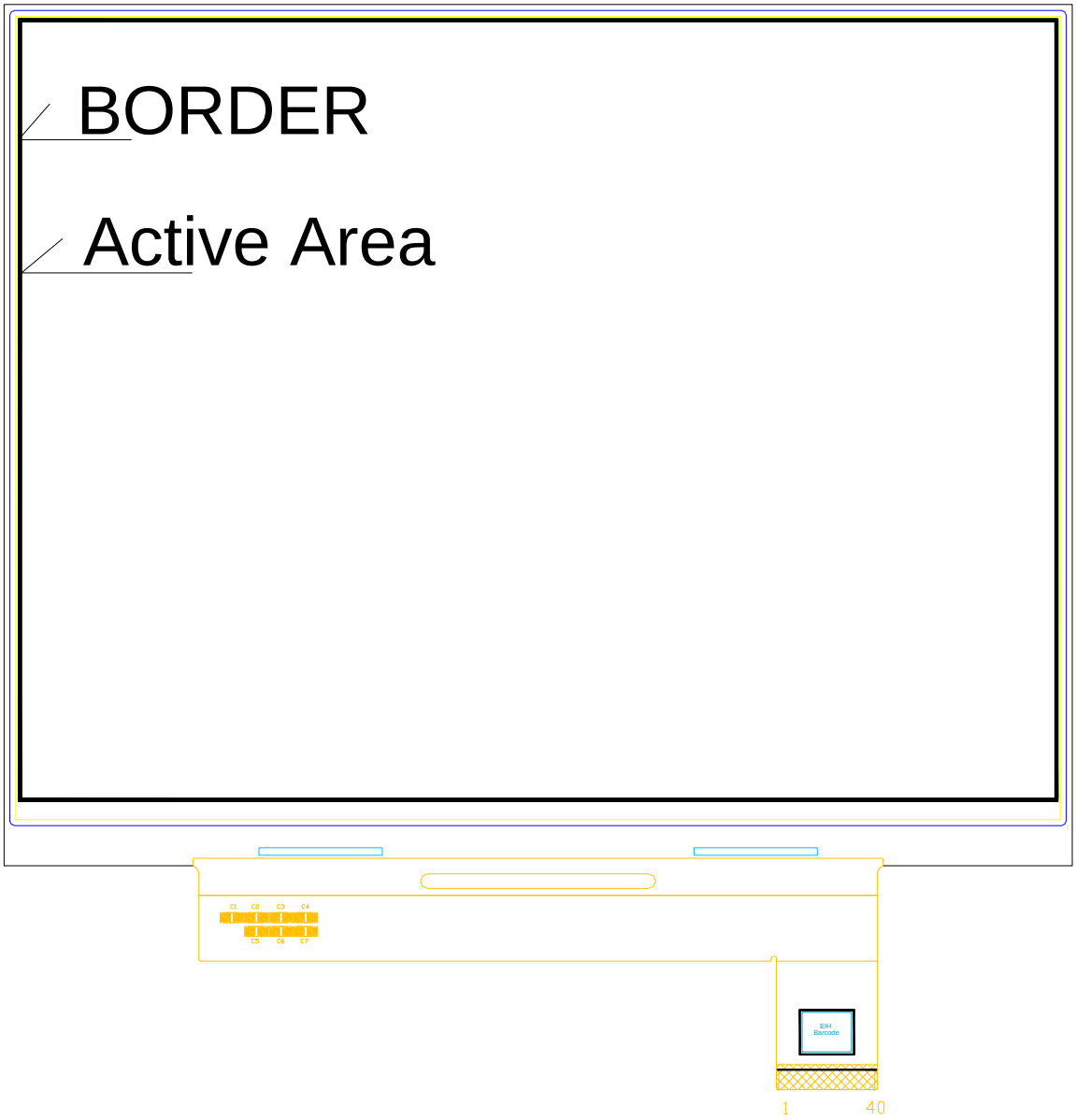
Data sheet status
Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and does not form part of the specification.

Remark
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

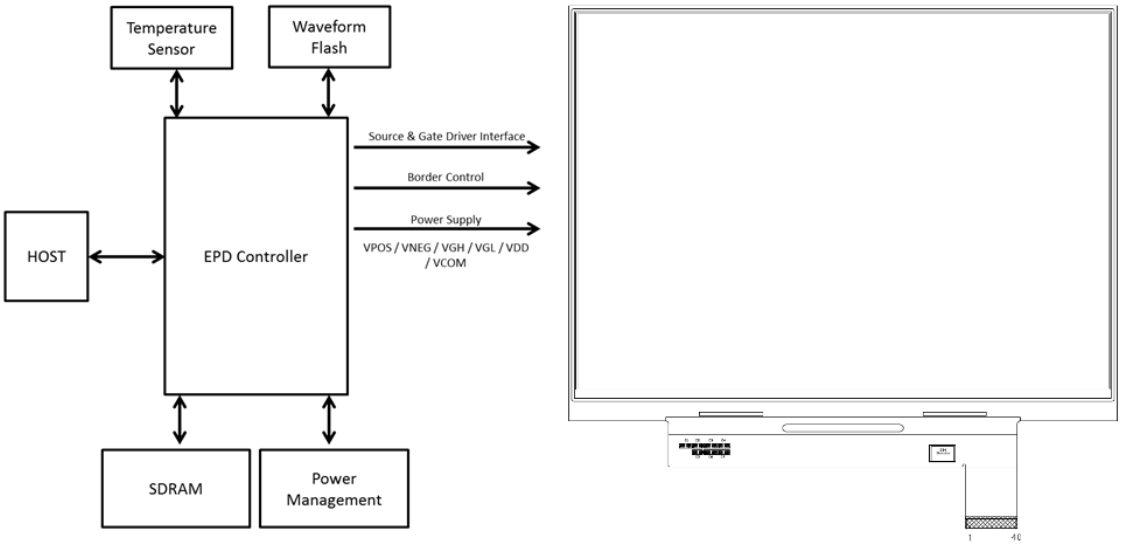
10. Reliability Test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Be	--
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-1Ae	--
3	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-78	
4	Low-Temperature Storage	T = -25°C for 240 hrs (Test in white pattern)	IEC 60 068-2-1Ab	
5	High Temperature High Humidity Storage	T = +60°C, RH = 80% for 240hrs (Test in White Pattern)	IEC 60 068 2-3CA	
6	High Temperature Storage	T = +70°C, RH = 40% for 240hrs (Test in White Pattern)	IEC 60 068-2-2Bb	--
7	Temperature Cycle	-25°C → +70°C, 100 Cycles 30min + 30min (Test in white pattern)	IEC 068-2-14 Nb	--
8	Solar radiation test	765 W/m^2 for 168hrs,40℃ (Test in white pattern)	IEC60 068-2-5Sa	--
9	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	--
10	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner,3 edges,6 faces One drop for each.	Full packed for shipment	--
11	Electrostatic Effect (non-operating)	(Machine model)+/- 250V 0Ω, 200pF	IEC 62179, IEC 62180	--

11. Border Definition

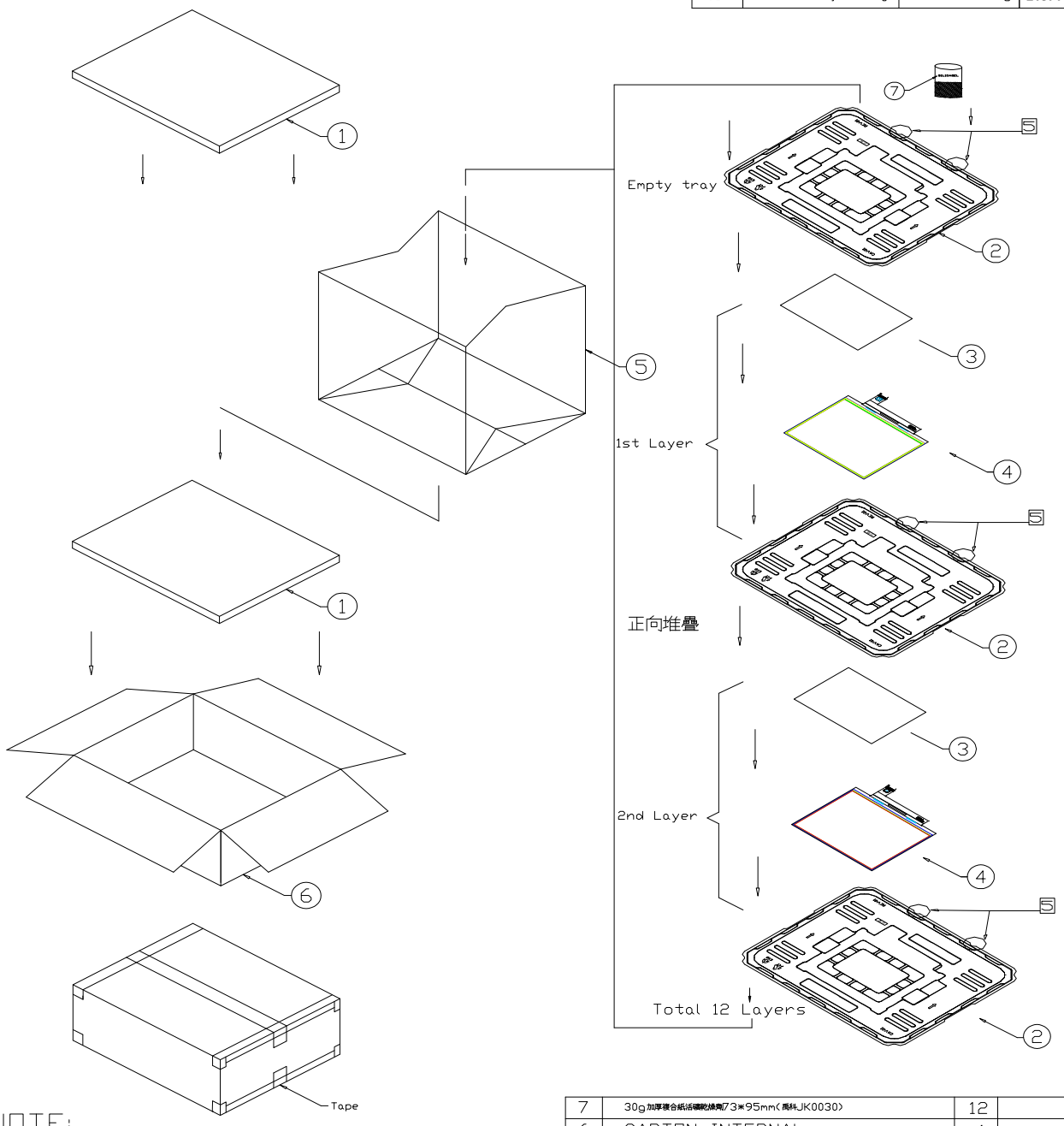


12. Block Diagram



13. Packing

REV	DESCRIPTION	DESIGN	DATE
01	Preliminary drawing	Jamie Chung	20190513



NOTE:
1.One layer include:
1pcs panel,1pc epe cusion sheet , 1pc tray
2.Q'TY:12 pcs panel/carton.
3.Dimension:455*375*190mm
4.Weight: 5 Kg
5.Tray 需0°堆疊, 堆疊後可從側邊檢視圓弧防呆方向是否正確

ITEM	DESCRIPTION	QTY	REMARK
7	30g加厚複合紙活磁吃燒爾73*95mm(高科JK0030)	12	
6	CARTON INTERNAL	1	
5	摺口袋450*380*700mm	1	抗靜電
4	ED103TC2	12	
3	EPE CUSHION SHEET	12	抗靜電
2	TRAY	13	抗靜電
1	EPE FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK

E Ink 元太科技工業股份有限公司 E Ink Holdings Inc.

APPROVE	Kevin Cheng	UNIT	SHEET	DWG.TITLE	A4 SIZE
CHECK	Jamie Chung	mm	1 OF 1	ED103TC2 Packing Draw	
DESIGN	Jamie Chung				