

# **EC25** Reference Design

**LTE Module Series**

Rev. EC25\_Reference\_Design\_Rev.D

Date: 2016-11-11









# 1 Reference Design

## 1.1. Introduction

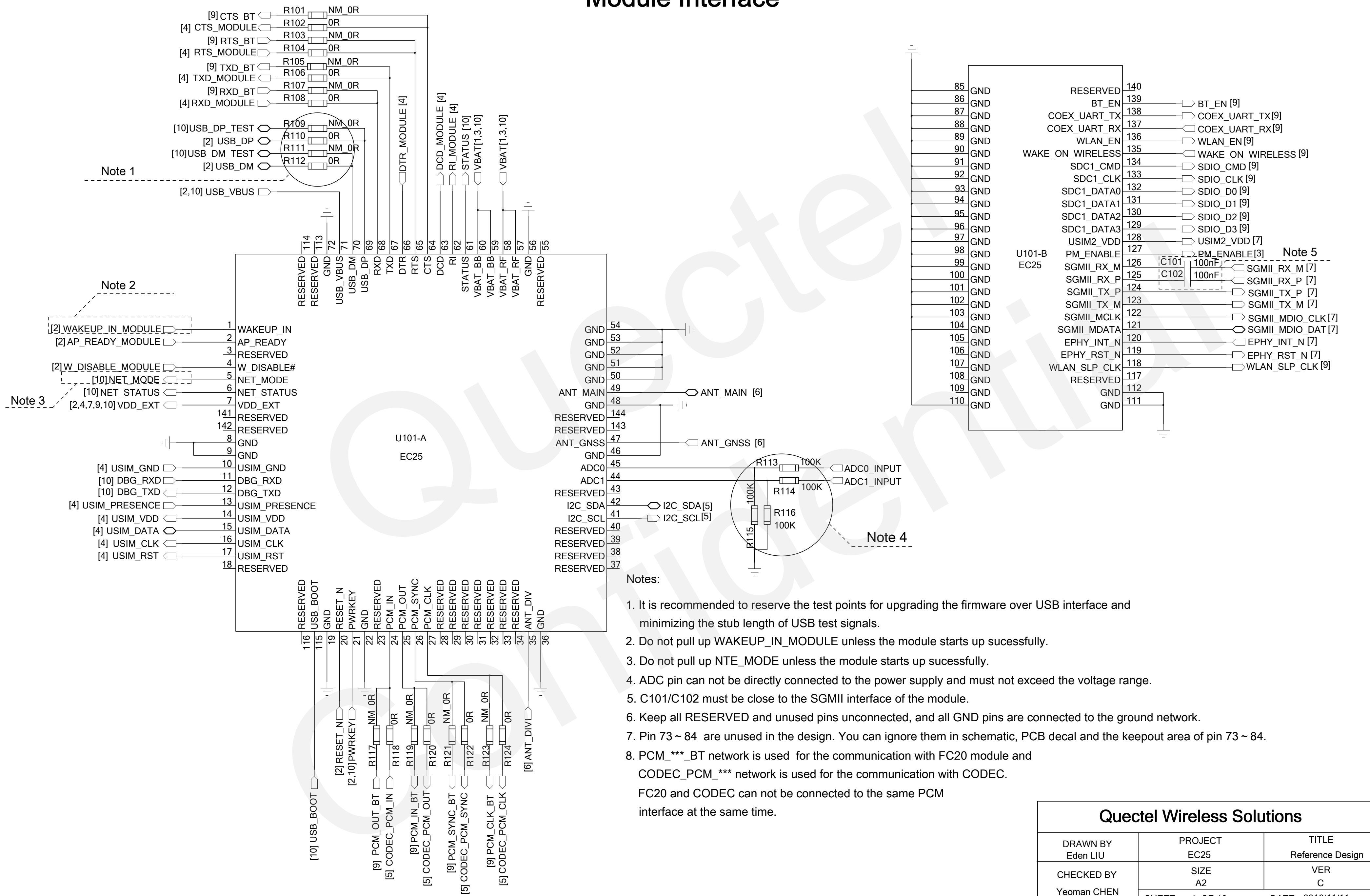
This document provides the reference design for Quectel EC25 module.

## 1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Quectel  
Confidential

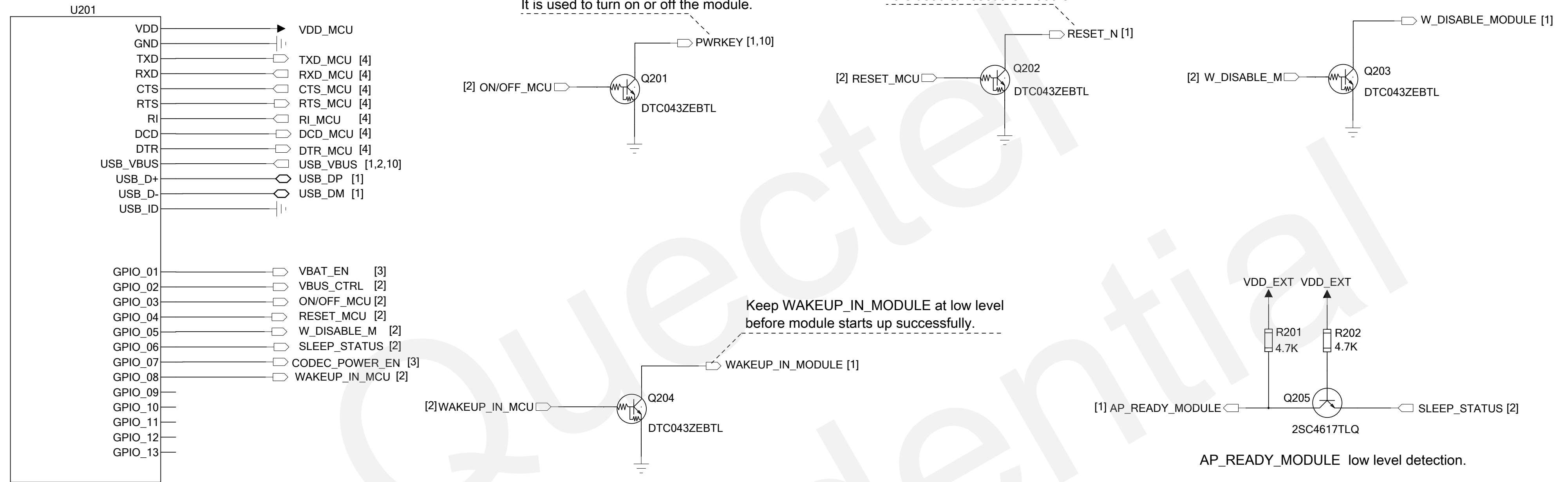
# Module Interface



- Notes:
1. It is recommended to reserve the test points for upgrading the firmware over USB interface and minimizing the stub length of USB test signals.
  2. Do not pull up WAKEUP\_IN\_MODULE unless the module starts up successfully.
  3. Do not pull up NTE\_MODE unless the module starts up successfully.
  4. ADC pin can not be directly connected to the power supply and must not exceed the voltage range.
  5. C101/C102 must be close to the SGMII interface of the module.
  6. Keep all RESERVED and unused pins unconnected, and all GND pins are connected to the ground network.
  7. Pin 73 ~ 84 are unused in the design. You can ignore them in schematic, PCB decal and the keepout area of pin 73 ~ 84.
  8. PCM\_\*\*\*\_BT network is used for the communication with FC20 module and CODEC\_PCM\_\*\*\* network is used for the communication with CODEC. FC20 and CODEC can not be connected to the same PCM interface at the same time.

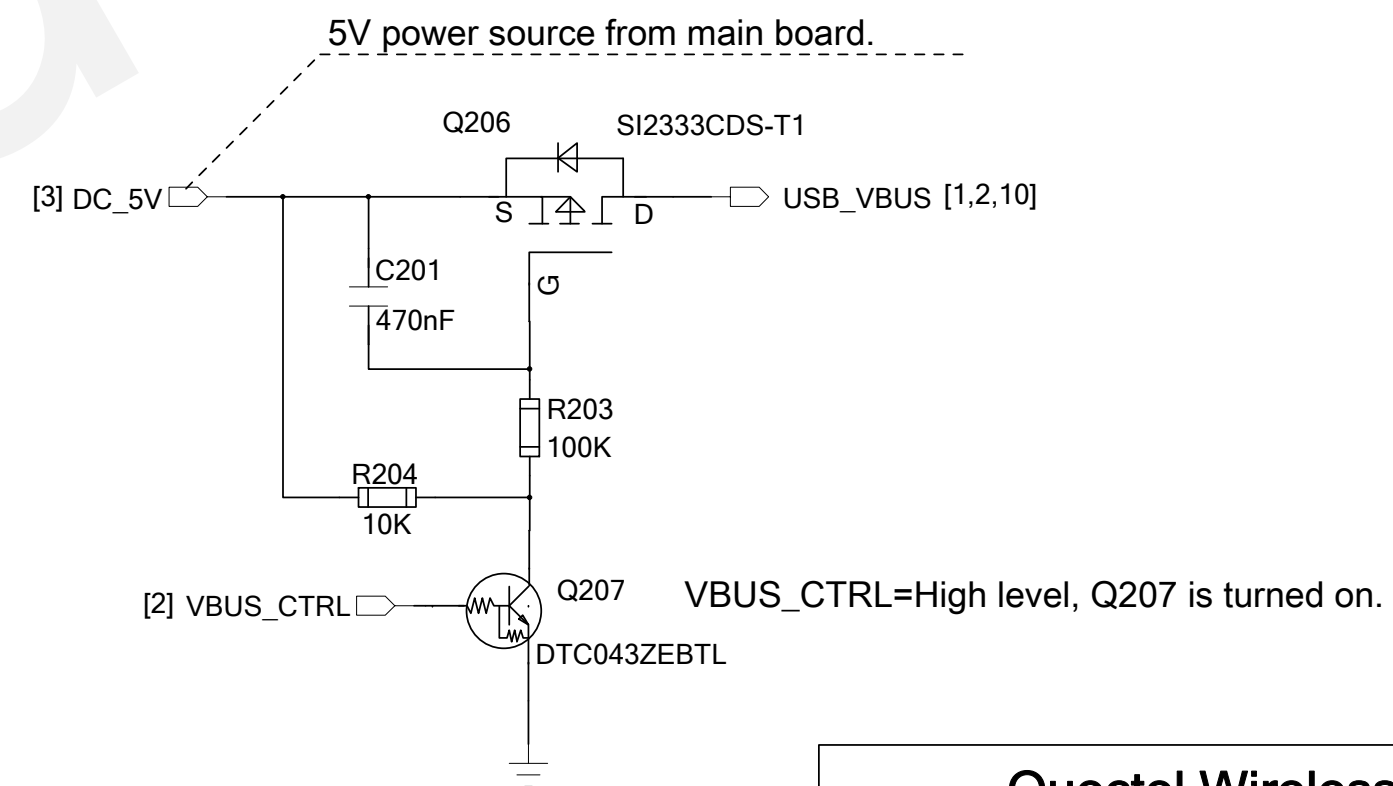
Quectel Wireless Solutions		
DRAWN BY Eden LIU	PROJECT EC25	TITLE Reference Design
CHECKED BY Yeoman CHEN	SIZE A2	VER C
SHEET	1 OF 10	DATE 2016/11/11

# MCU Interface



### Notes:

1. U201 represents customer's MCU.
2. EC25 can only work as a USB device and supports Full Speed and High Speed modes. To communicate with USB interface, MCU needs to support USB host or OTG function. The VBUS pins of MCU and EC25 should be powered by a 5V power system for USB detection, and VBUS-CTRL is used to turn on/off VBUS power supply.
3. AP\_READY can be configured to high level detection and low level detection. For more details about AP\_READY, please refer to *Quectel\_EC25\_Hardware\_Design* and *Quectel\_EC25&EC21\_AT\_Commands\_Manual*.
4. Transistor circuits (Q203~Q206) are used for level translation.



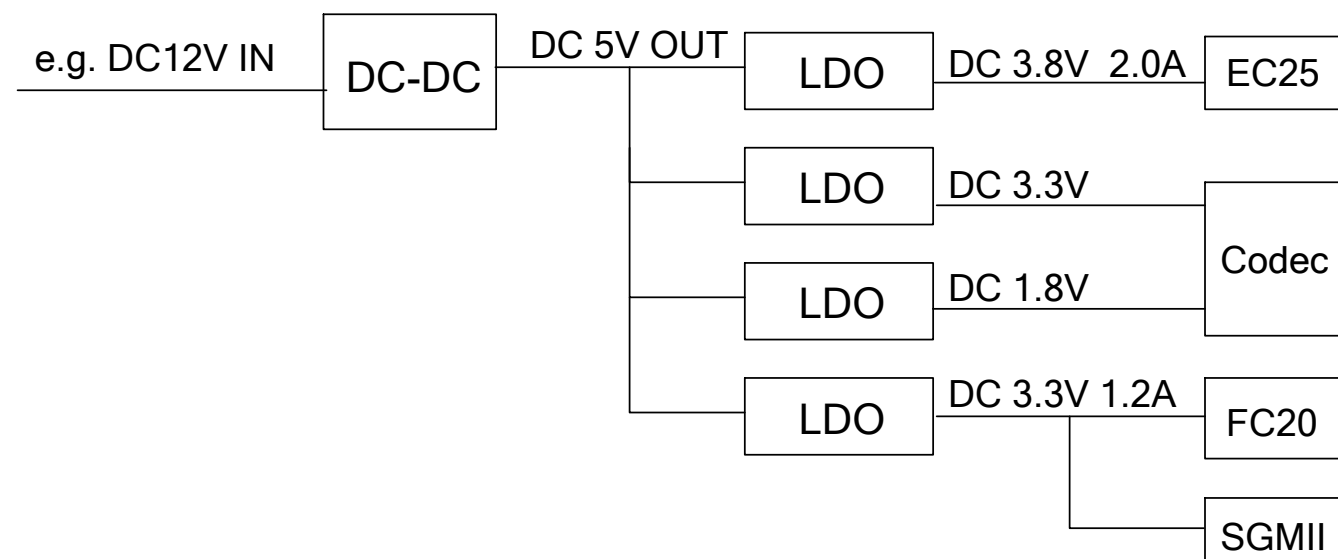
## Quectel Wireless Solutions

DRAWN BY Eden LIU	PROJECT EC25	TITLE Reference Design
CHECKED BY Yeoman CHEN	SIZE A2	VER C
SHEET 2 OF 10		DATE 2016/11/11

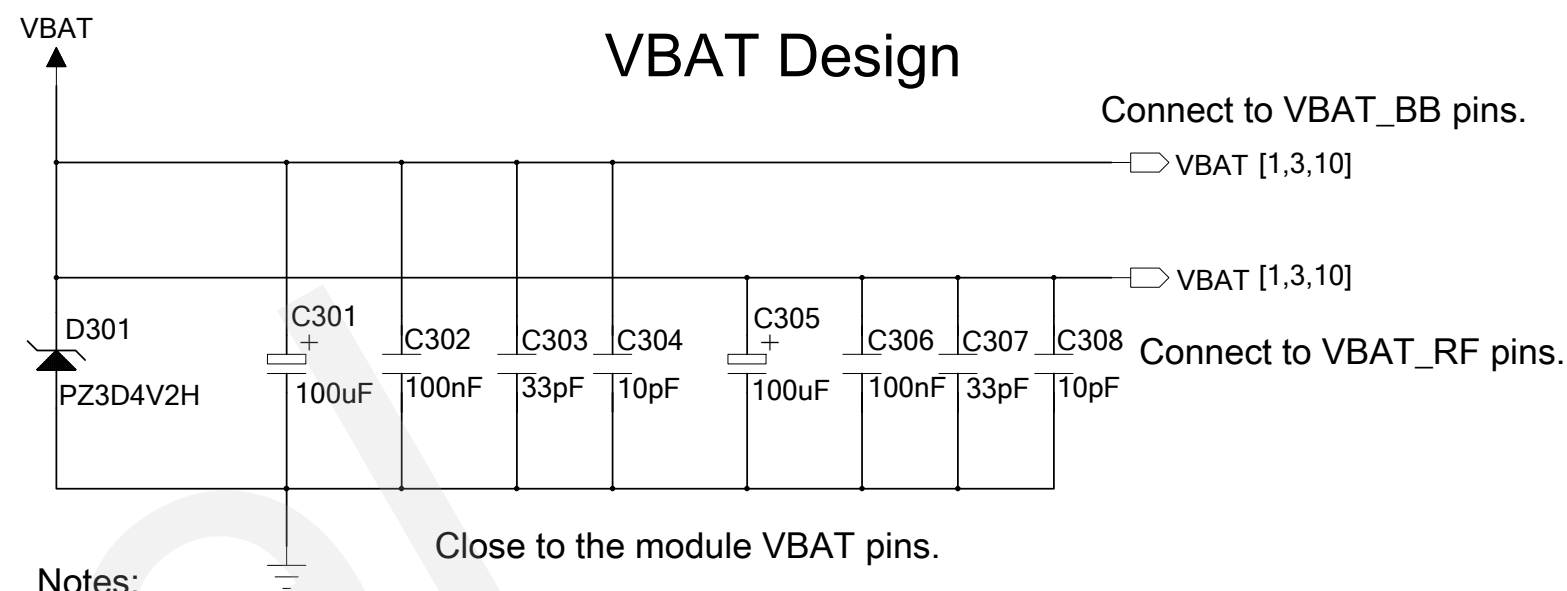
# Power Supply Design

## DC-DC Application

It is used when the input voltage is above 7V. Use a DC-DC converter to convert a high input voltage into 5V output, and then the LDOs will generate 3.8V, 3.3V and 1.8V typical voltages.



## VBAT Design

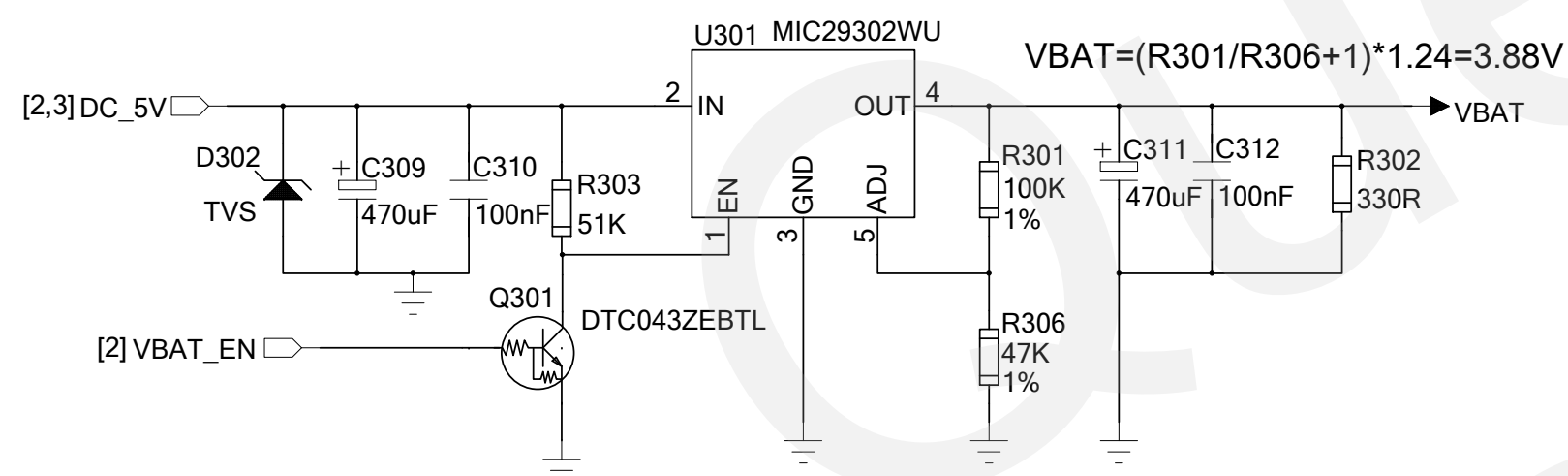


Notes:

1. The power supply must be able to provide sufficient current up to 2A or more.
2. VBAT should be routed in star mode to VBAT\_BB and VBAT\_RF pins.
3. The recommended operating voltage of VBAT is 3.3V~4.3V.

## LDO Application

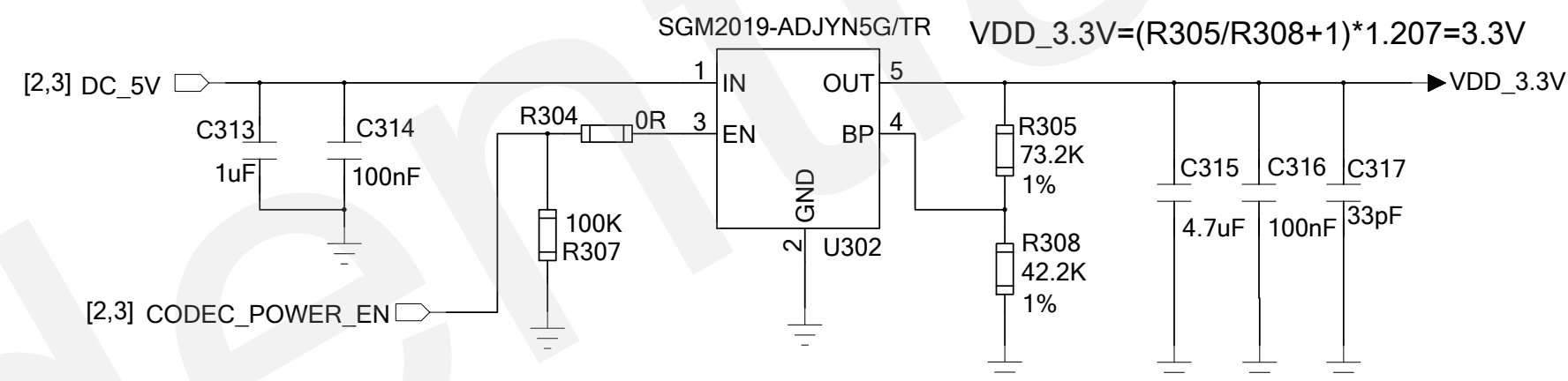
It is used when the input voltage is below 7V.



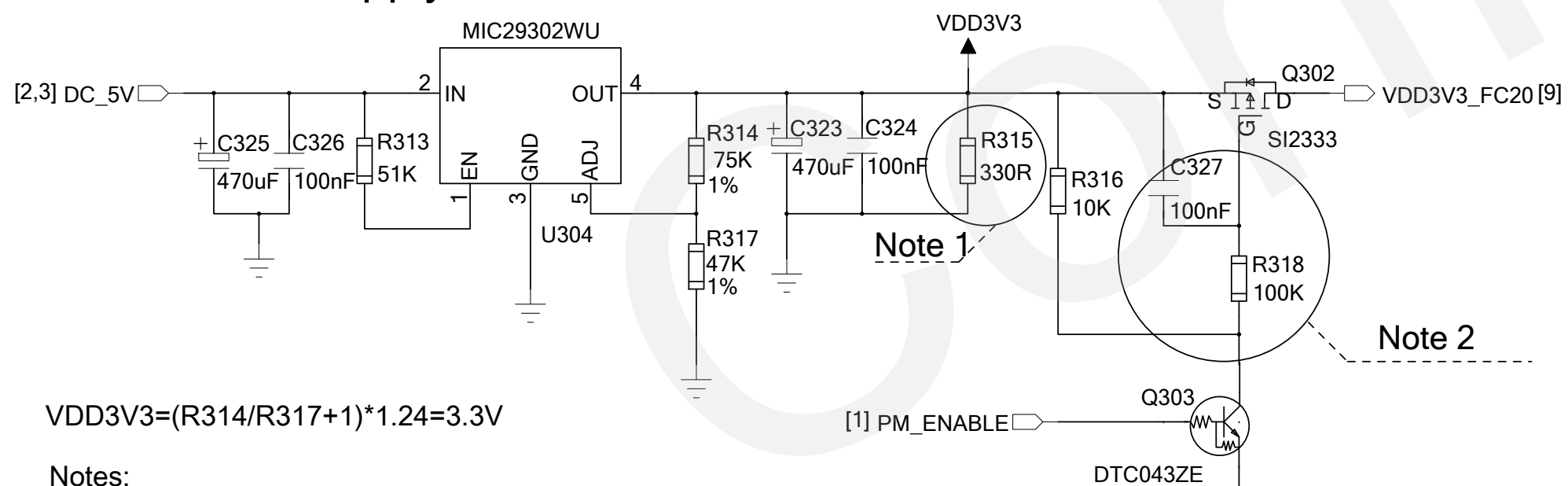
Note:

Recommended load current is greater than 10mA.

## Supply Power for PCM Codec



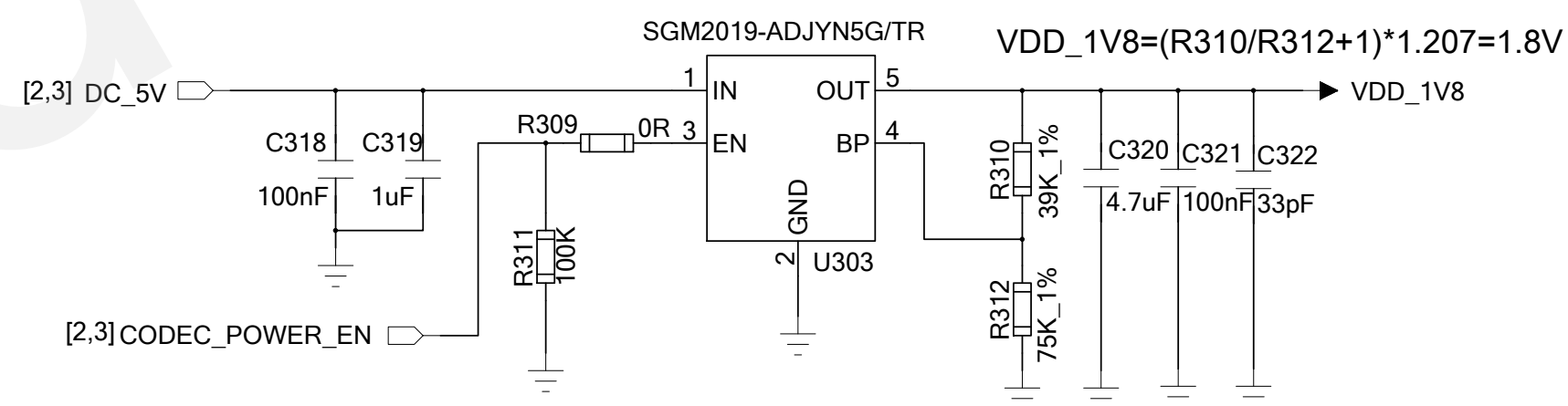
## Supply Power for FC20 and SGMII



$$VDD3V3 = (R314/R317 + 1) * 1.24 = 3.3V$$

Notes:

1. Recommended load current of MIC29302WU is greater than 10mA.
2. RC circuit, which is assembled with R318 and C327, is used to delay the start-up of MOSFET switch circuit.



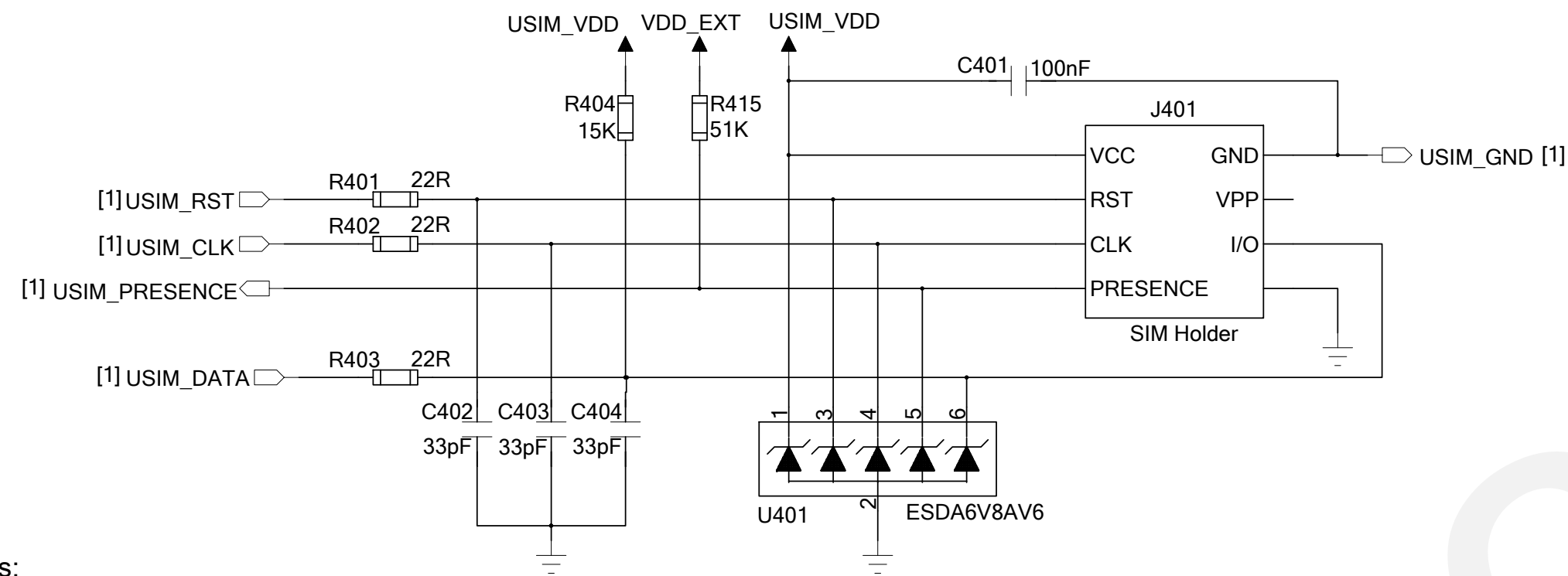
## Quectel Wireless Solutions

DRAWN BY Eden LIU	PROJECT EC25	TITLE Reference Design
CHECKED BY Yeoman CHEN	SIZE A2	VER C
SHEET 3 OF 10		DATE 2016/11/11



# USIM and UART Design

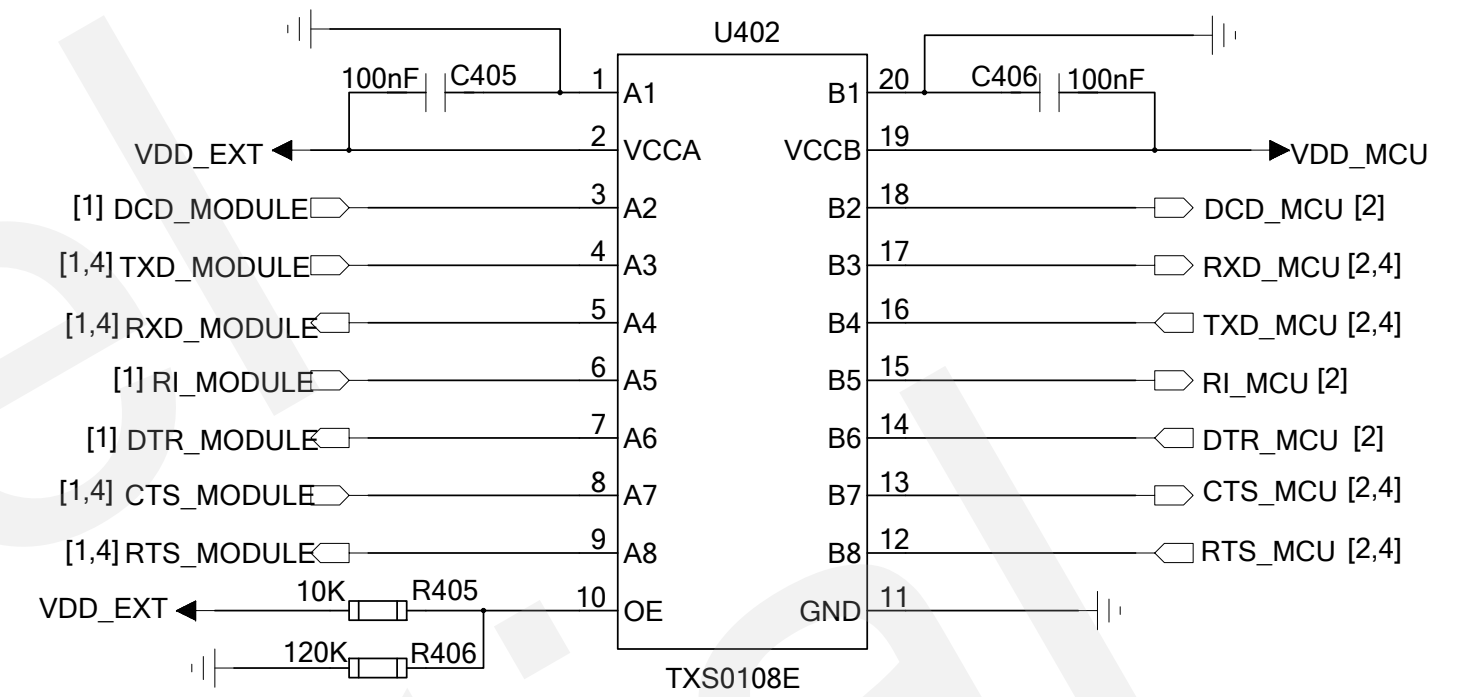
## USIM Interface



### Notes:

1. The decouple capacitor of USIM\_VDD should be less than 1uF and must be near to USIM socket.
2. EC25 module provides an input pin (USIM\_PRESENCE) to detect whether the USIM card exists or not. It supports both low level and high level detections. For more details, please refer to *Quectel\_EC25\_Hardware\_Design*.

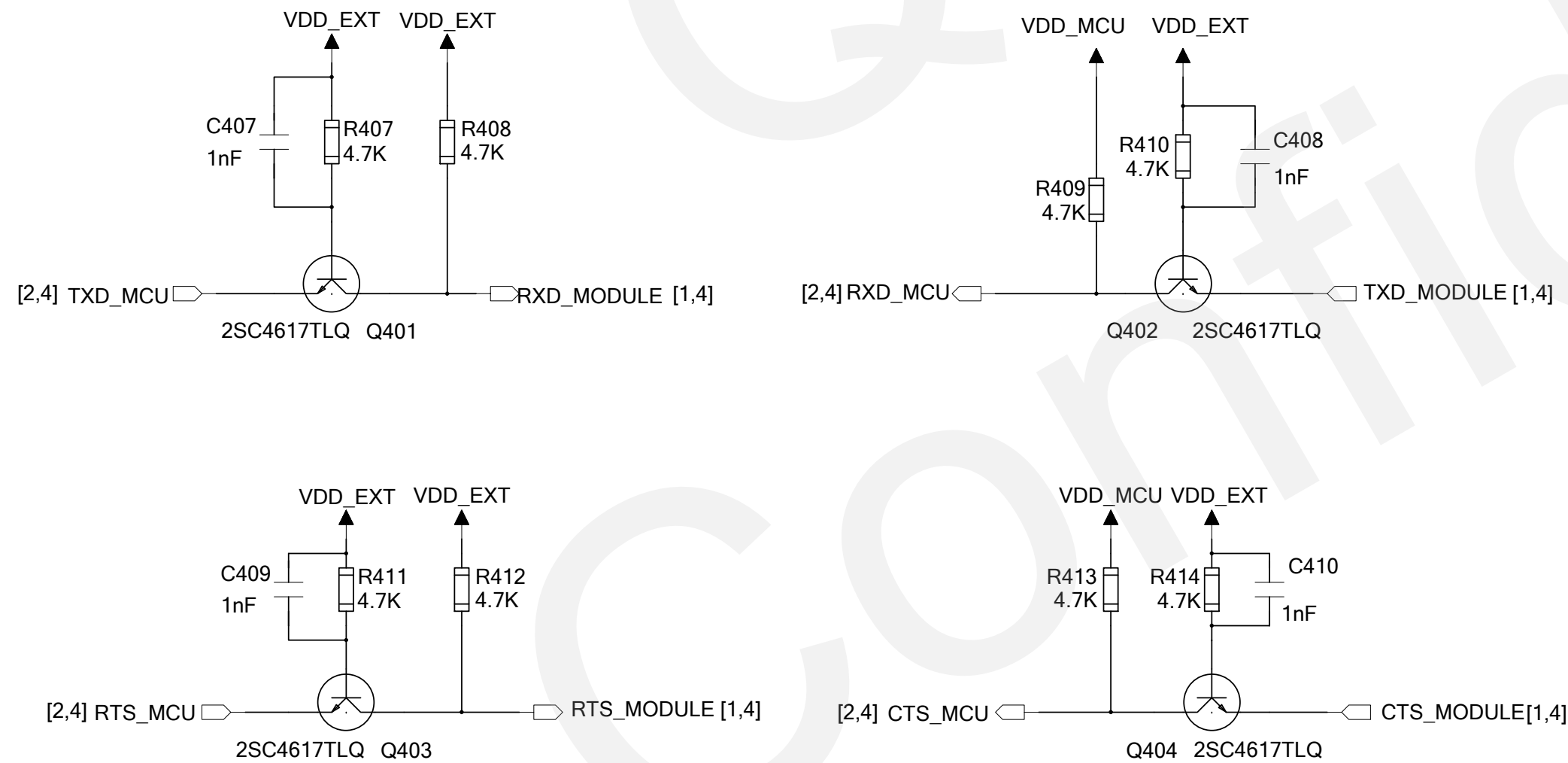
## UART Translation - IC Solution (Recommended)



### Note:

It is recommended to use an IC conversion chip for UART translation.

## UART Translation - Transistor Solution



### Note:

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

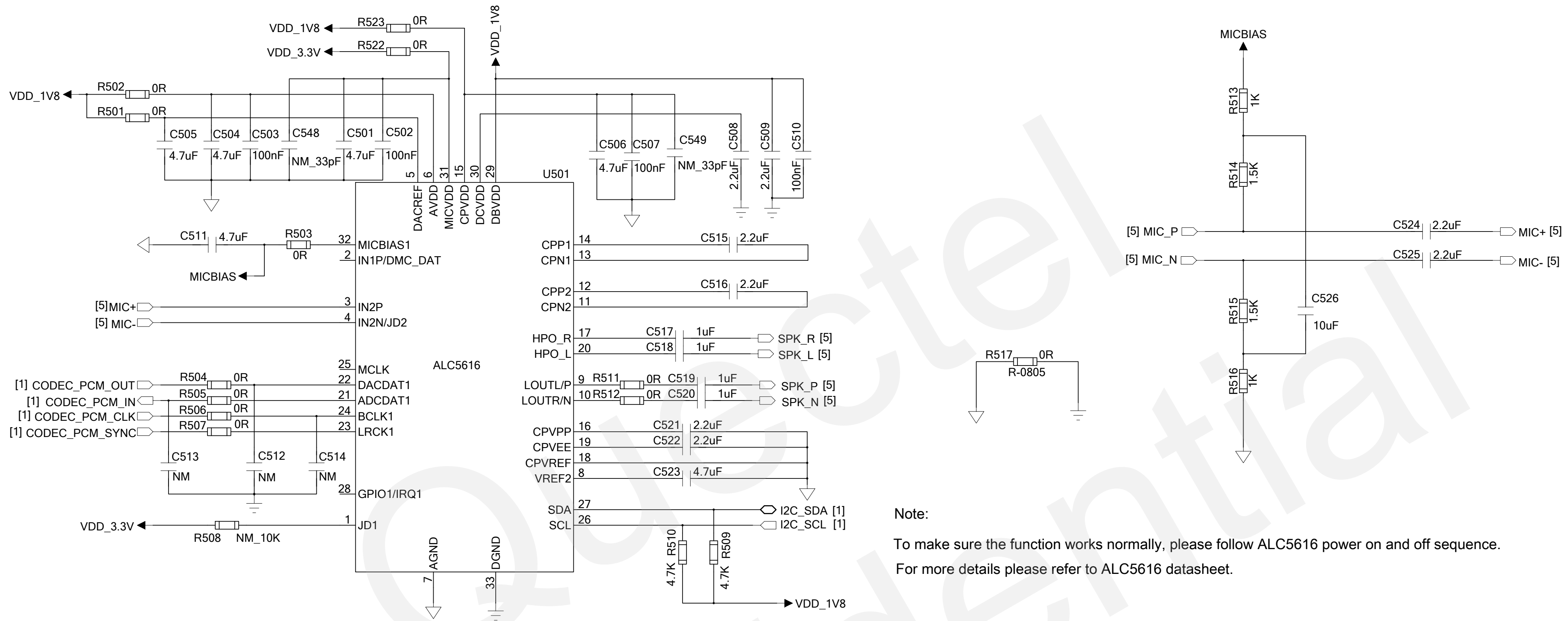
### Notes:

1. R401~R403 are applied to suppress the EMI spurious transmission and enhance the ESD protection.
2. It is recommended to take electrostatic discharge (ESD) protection measures near the USIM card socket. The TVS diode with junction capacitance less than 50 pF must be placed as close as possible to the USIM socket.
3. R404 can improve anti-jamming capability of the USIM circuit, and it should be placed close to the USIM connector.
4. VCCA should not exceed VCCB. For more information about TXS0108E, please refer to the datasheet from TI.
5. If you need to enable high baud rate, it is highly recommended to install a 1nF capacitor (C407/C408/C409/C410) on transistor circuit.
6. The DTR transistor circuit is similar to RTS interface. The RI and DCD transistor circuits are similar to CTS interface.

## Quectel Wireless Solutions

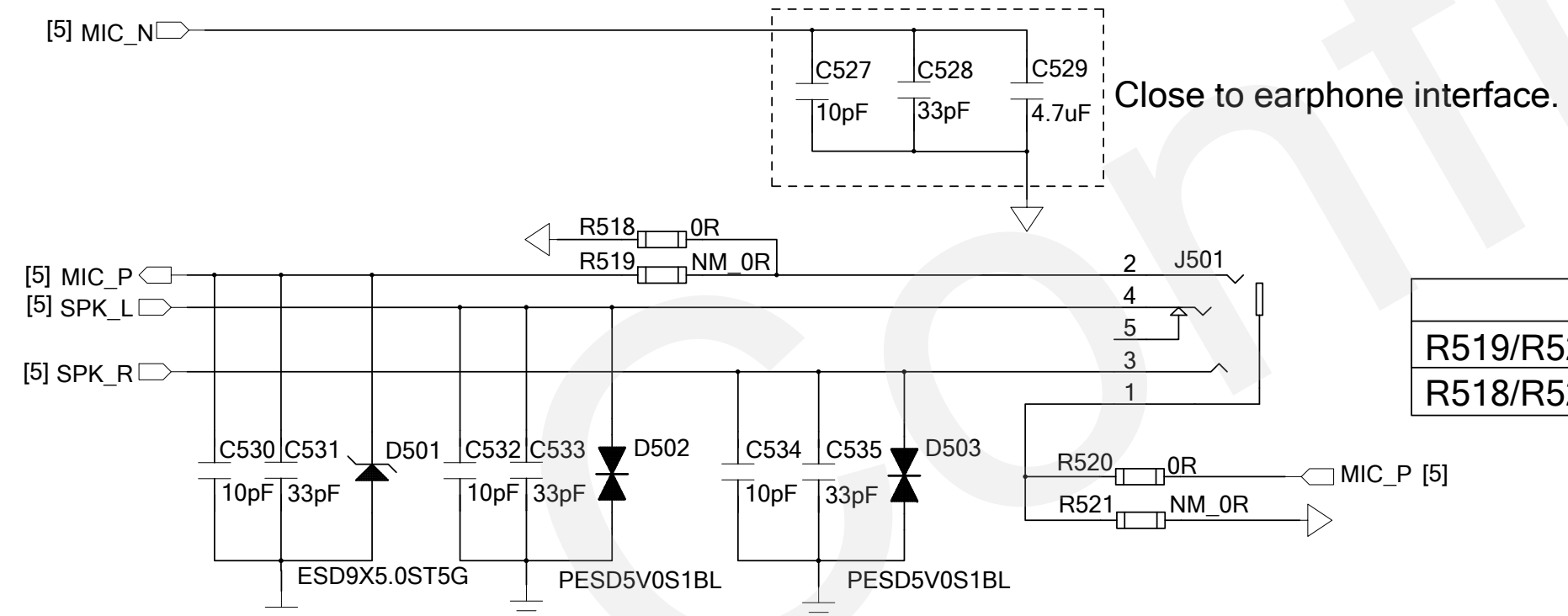
DRAWN BY Eden LIU	PROJECT EC25	TITLE Reference Design
CHECKED BY Yeoman CHEN	SIZE A2	VER C
SHEET 4 OF 10		DATE 2016/11/11

# Audio Design



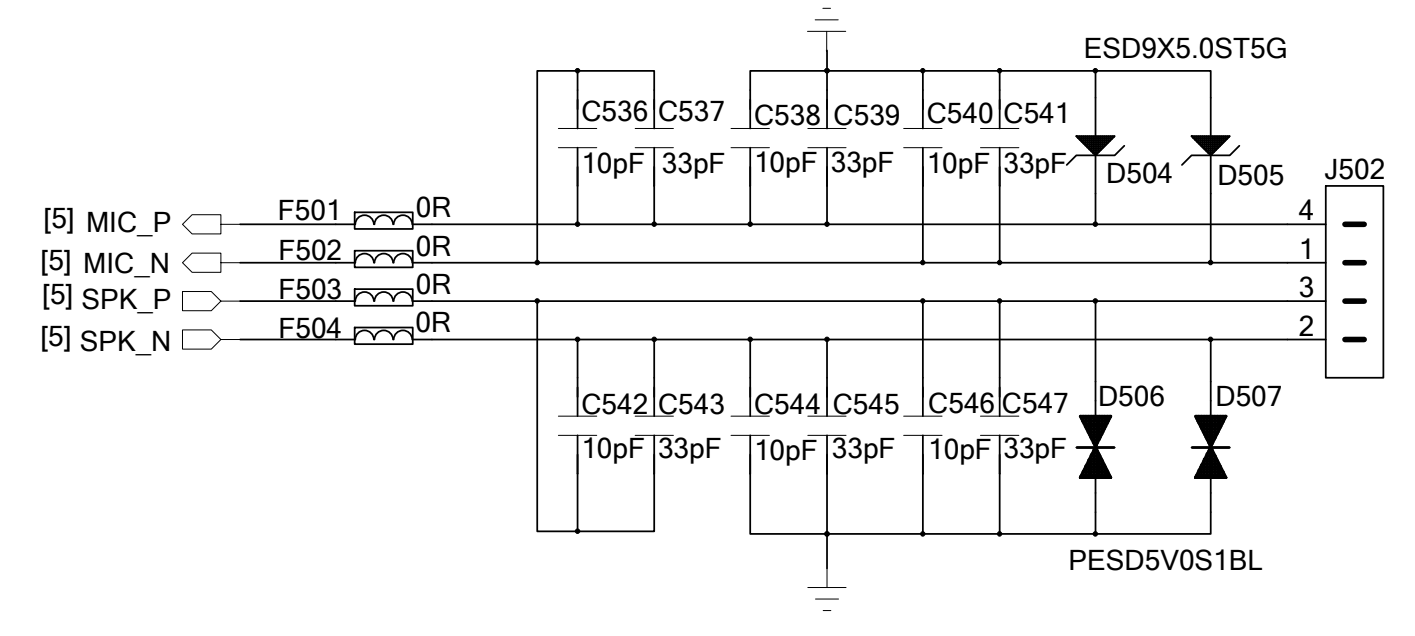
**Note:**  
To make sure the function works normally, please follow ALC5616 power on and off sequence.  
For more details please refer to ALC5616 datasheet.

## Audio - Earphone Application



**Notes:**  
1. The analog output only drives earphone and headset. For larger power loads such as speakers, the design needs to increase the audio power amplifier.  
2. The maximum capacitive loading for SPK is 330 pF and the maximum capacitive loading for MIC is 250 pF.

## Audio - Handset Application

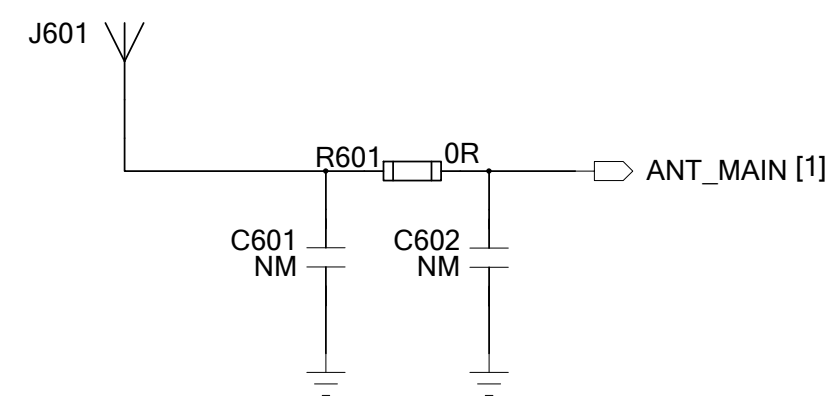


### Quectel Wireless Solutions

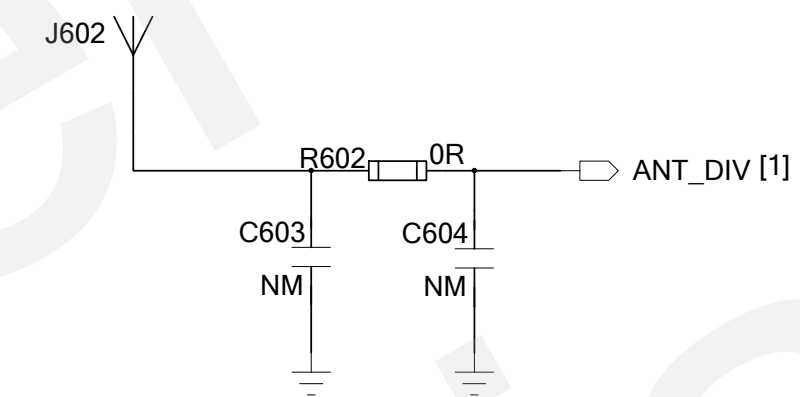
DRAWN BY Eden LIU	PROJECT EC25	TITLE Reference Design
CHECKED BY Yeoman CHEN	SIZE A2	VER C
SHEET 5 OF 10		DATE 2016/11/11

# RF and GNSS Design

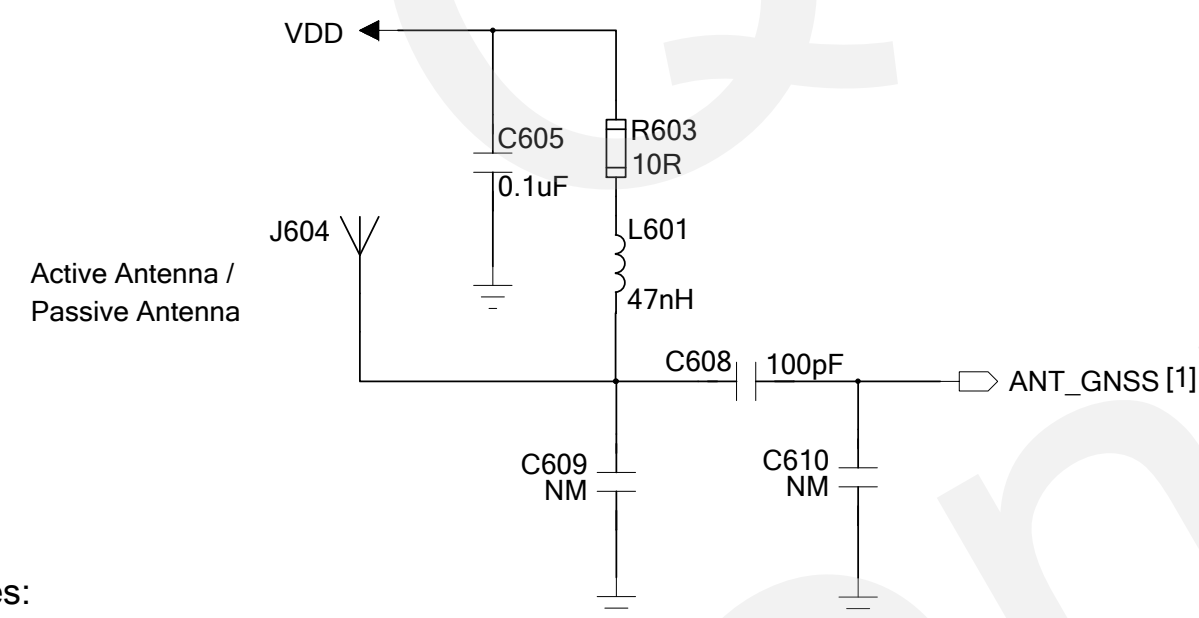
## Main Antenna Interface



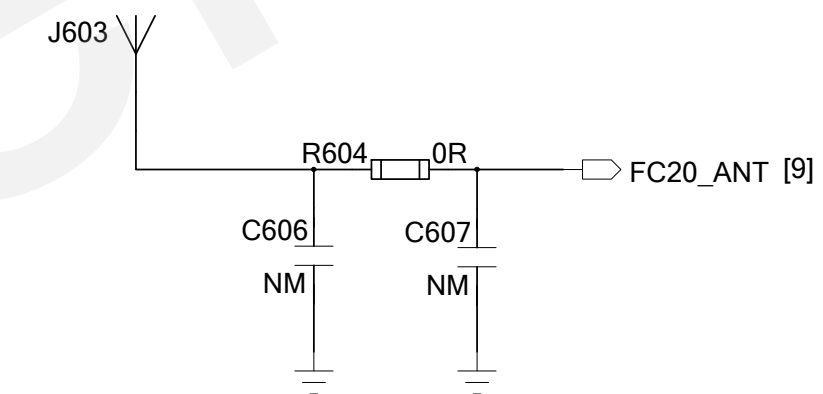
## Diversity Antenna Interface



## GNSS Antenna Circuit



## FC20 Antenna Circuit



### Notes:

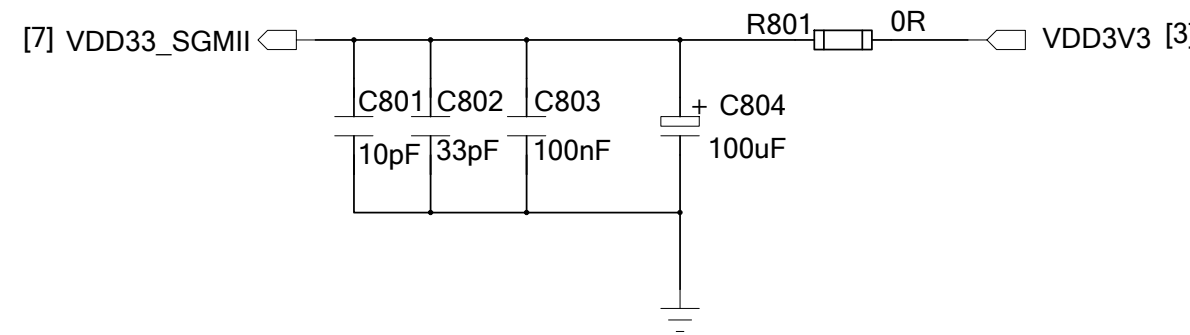
1. The main antenna circuit, diversity receiving antenna circuit and FC20 antenna circuit are recommended to use PI type circuit, which is convenient for subsequent debugging.
2. The diversity reception function is ON by default. If diversity antenna is not used, there is a need to use AT command to turn off diversity reception.
3. You can choose an external LDO according to the active antenna to supply power.
4. If you design the antenna circuit with passive antenna, the R603 and L603 are not needed.
5. ESD protection devices should be added to the GNSS antenna interface, and the parasitic capacitance should be less than 0.05pF.

### Quectel Wireless Solutions

DRAWN BY Eden LIU	PROJECT EC25	TITLE Reference Design
CHECKED BY Yeoman CHEN	SIZE A2	VER C
SHEET	6 OF 10	DATE 2016/11/11

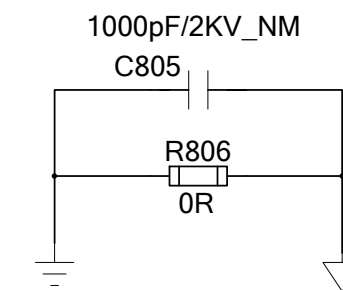
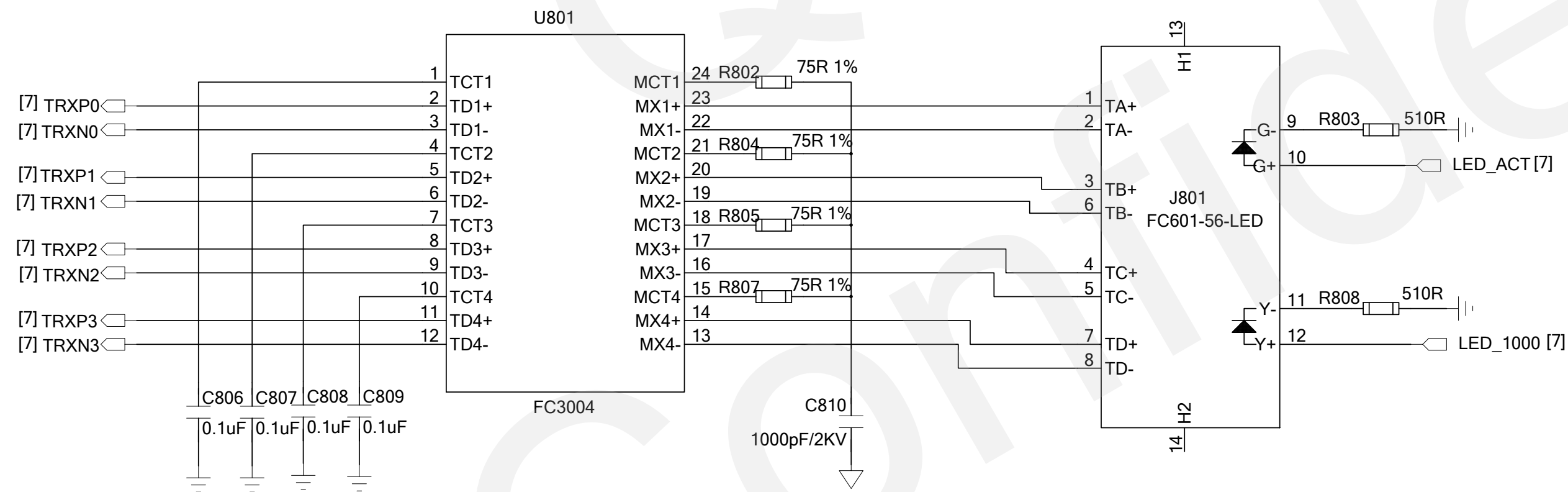


# SGMII Design (Part 2)



PHY core configuration signal	Description	Default internal weak pull-up/down	Application external weak pull-up/down
PHY_AD2	PHY_AD[2:0] set the lower three bits of the physical address. The upper two bits of the physical address are set to 00.	1	0
PHY_AD1		0	0
PHY_AD0		0	0
MODE 3	Mode select bit 3	0	0
MODE 2	Mode select bit 2	0	0
MODE 1	Mode select bit 1	0	0
MODE 0	Mode select bit 0	0	1
EXT_INT_SEL	An external 10K pull-down resistor is required.	1	0

0=Pull-down, 1=Pull-up.



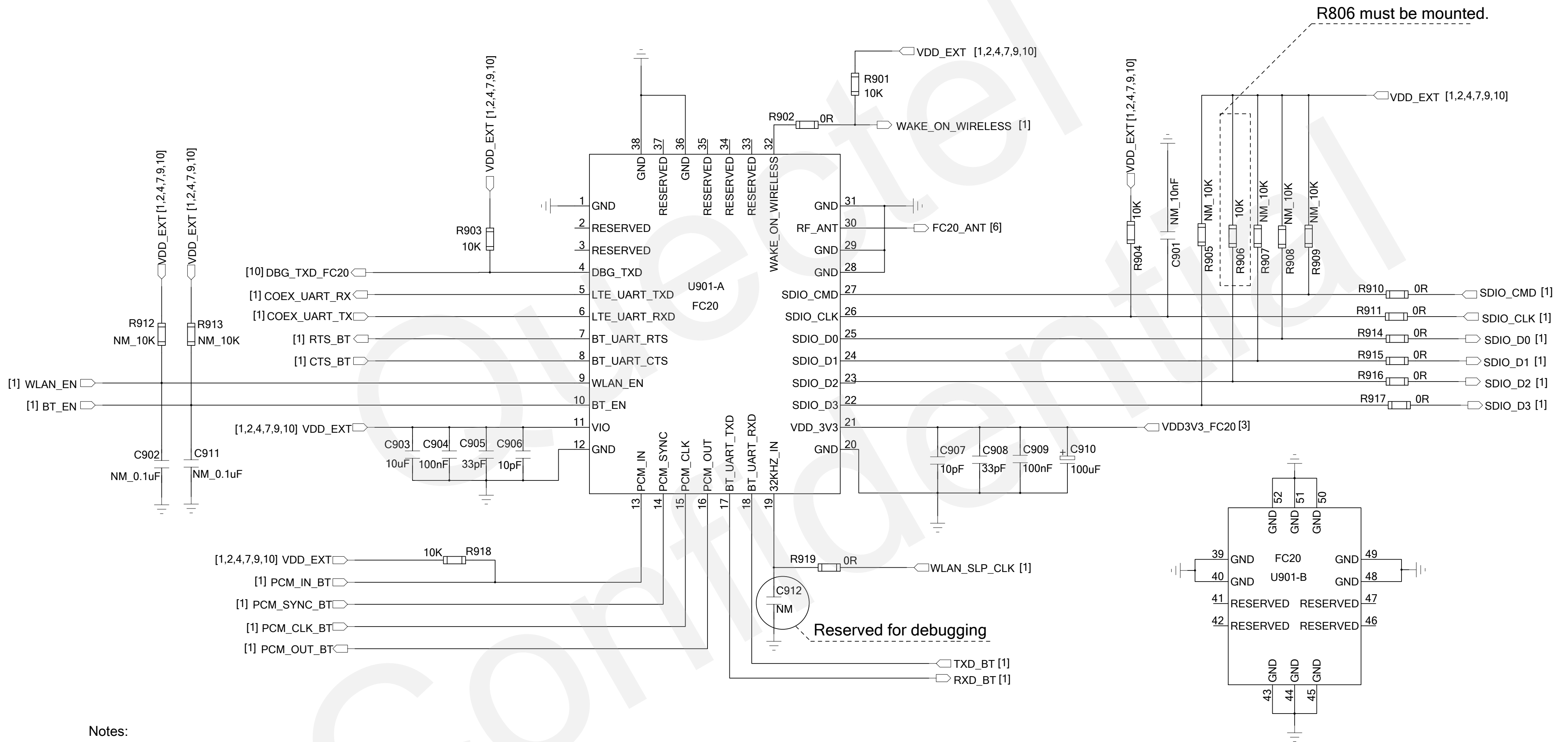
**Notes:**

1. Differential pair P/N skew must be less than 20 mils, and the maximum trace length must be less than 10 inches.
2. Using the 100 ohm ± 10% differential impedance with 50 ohm ± 10% single-ended impedance.
3. To minimize crosstalk, the distance between separate adjacent pairs that are on the same layer must be equal to or larger than 40 mils.
4. Copper filling around transformers is prohibited for better ESD protection performance.
5. For better EMI suppression performance, do not route in top layer.

## Quectel Wireless Solutions

DRAWN BY Eden LIU	PROJECT EC25	TITLE Reference Design
CHECKED BY Yeoman CHEN	SIZE A2	VER C
SHEET	8 OF 10	DATE 2016/11/11

# FC20 Series Design



**Notes:**

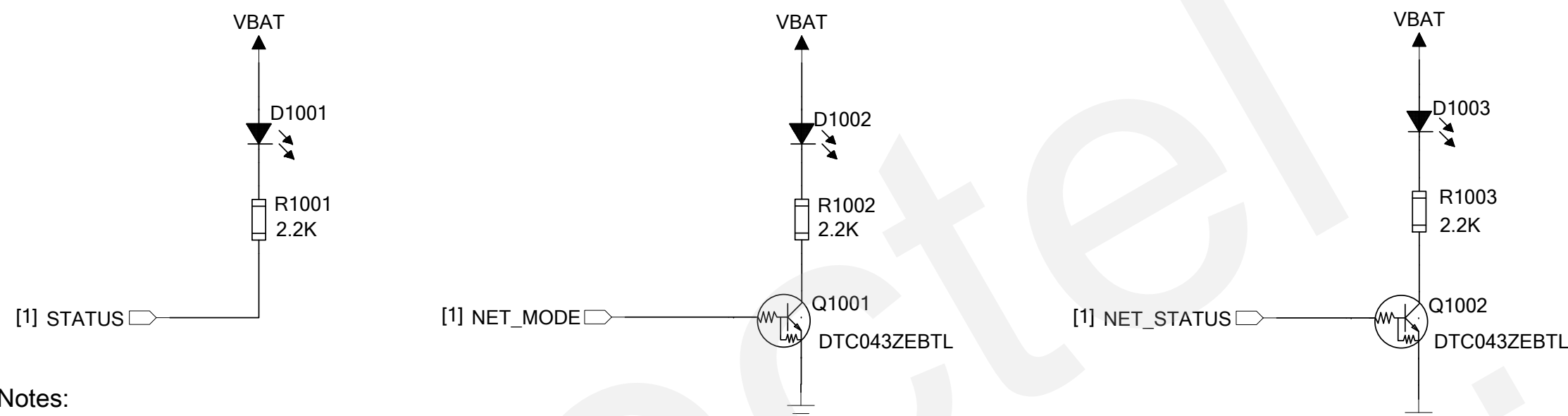
1. Keep all RESERVED and unused pins unconnected.
2. BT function of FC20 is under development.
3. SDIO\_DATA2 is a signal that affects the boot of the module, and should be kept at high level when the power supply resets.
4. The impedance of the SDIO data signal line must be controlled as 50Ω when routing.
5. SDIO data lines should be wrapped together by GND lines; SDIO\_CMD and SDIO\_CLK network lines should be wrapped with GND lines separately.
6. Please keep the pin 5~8, 10, and 13~18 open in FC20-N.

## Quectel Wireless Solutions

DRAWN BY Eden LIU	PROJECT EC25	TITLE Reference Design
CHECKED BY Yeoman CHEN	SIZE A2	VER C
SHEET	9 OF 10	DATE 2016/11/11

# Indicators and Test Points

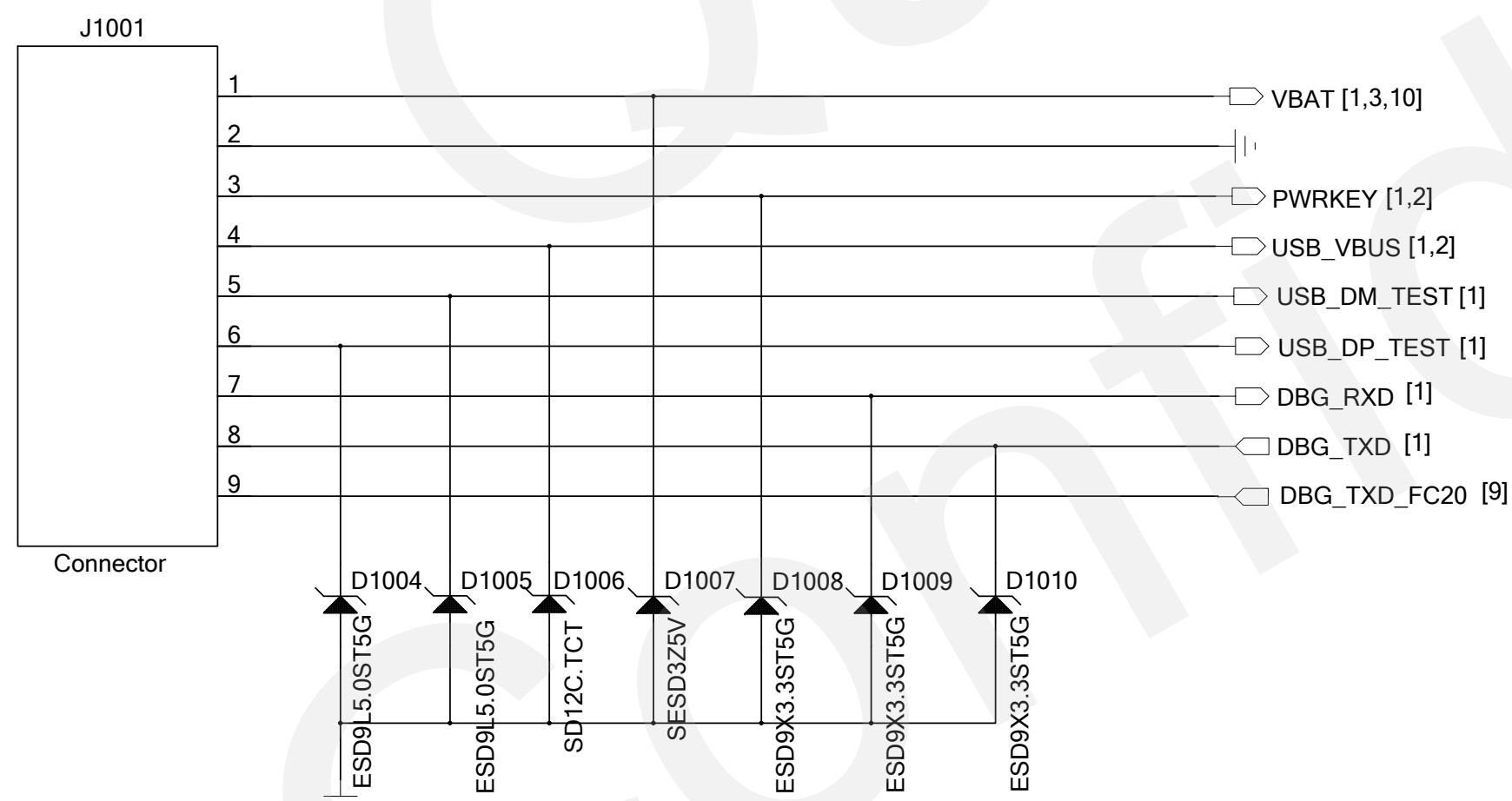
## Indicators



### Notes:

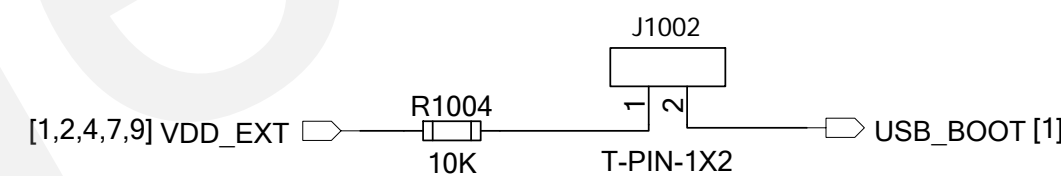
1. The STATUS is an open drain output pin, and its drive current is less than 1mA.
2. For more details about NET\_MODE and NET\_STATUS, please refer to the document *Quectel\_EC25\_Hardware\_Design*.

## Reserved Test Points



### Notes:

1. Both USB and debug UART interfaces are reserved for software debugging.
2. USB interface also can be used to upgrade firmware.
3. Keep USB test points as close as possible to USB pins.  
Junction capacitance of ESD component on USB data lines might influence the signal, please pay attention to it. Typically, the capacitance should be less than 1pF.



### Note:

When USB\_BOOT is at high level, the module will be forced to be in download mode.

## Quectel Wireless Solutions

DRAWN BY Eden LIU	PROJECT EC25	TITLE Reference Design
CHECKED BY Yeoman CHEN	SIZE A2	VER C
SHEET 10 OF 10	DATE 2016/11/11	