e•MMC5.1M100 Series
Product Manual

KM110SS0016GxA-DDD00WT

KM111SS0016GxA-DDD00WT

KM110SS1032GxA-DDD00WT

KM110SS1064GxA-DDD00WT

Datasheet Rev.1.3

JUL.2018

Revision History

Version	Date	Description
1.0	*Apr.2th,2018*	*Preliminary.*
1.1	*May.21th,2018*	*AddKM110SS1032GxA-DDD00WT.*
1.2	*Jun.21th,2018*	*RemoveBus Circuitry Diagram.*
1.3	*Jul.6th,2018*	*AddKM110SS1064GxA-DDD00WT.*

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1.Introduction

1.1 General Description

KimtigoM100 seriese•MMC is a hybrid device combining an embedded thin flash controller and standard 3D TLC NAND flash memory, with an industry standard e•MMC™ 5.1 interface.It's the ideal solution for embedded solutions of mobile phone, tablet, smart TV, Set Top Box and networking appliance.

1.2 Features Overview

- **Embedded Multi-Media Card (e•MMC) Electrical Standard (5.1)**
- **153-ball FBGA - 11.5mm×13.0mm×1.0mm.max**
- **Operating voltage range**
  - VCC (NAND): 2.7–3.6V
  - VCCQ (Controller): 1.7–1.95V/ 2.7–3.6V
- **Temperature range:**
  - Operating temperature range: –25℃ to +85℃
  - Storage temperature range: –40℃ to +85℃
- **Data bus width :** 1bit, 4bit, 8bit
- **MMC –Specific Feature**
  - 11-wirebus(clock, data strobe, 1-bit command, 8-bit data bus) and a hardware reset
  - Supportsawiderangeofpowersupplyvoltage：1.8V and 3.3V
  - Supports HS400 Modewith Enhanced Strobe
  - Upto 200MHzclockfrequency
  - eMMC productionstateawareness
  - eMMC devicehealthreport
  - Supports Command Queuing
  - Programbuswidth：1-bit, 4-bit, and 8-bit
  - Supports Bootoperationin High Speedand DDR mode
  - Supports Bootmodeand Alternative Bootmode
  - ReplayProtected Memory Block (RPMB)
  - Enhanced Partition Attributes
  - High Priority Interrupt (HPI)
  - Background Operations
  - Enhanced Reliable Write
  - Secureremovaltypes
  - Enhancedtechniques: Sleep Notification inpoweroffnotification, datatagging, packedcommands, discard,sanitize, RTC (real time clock)

1.3 Block Diagram

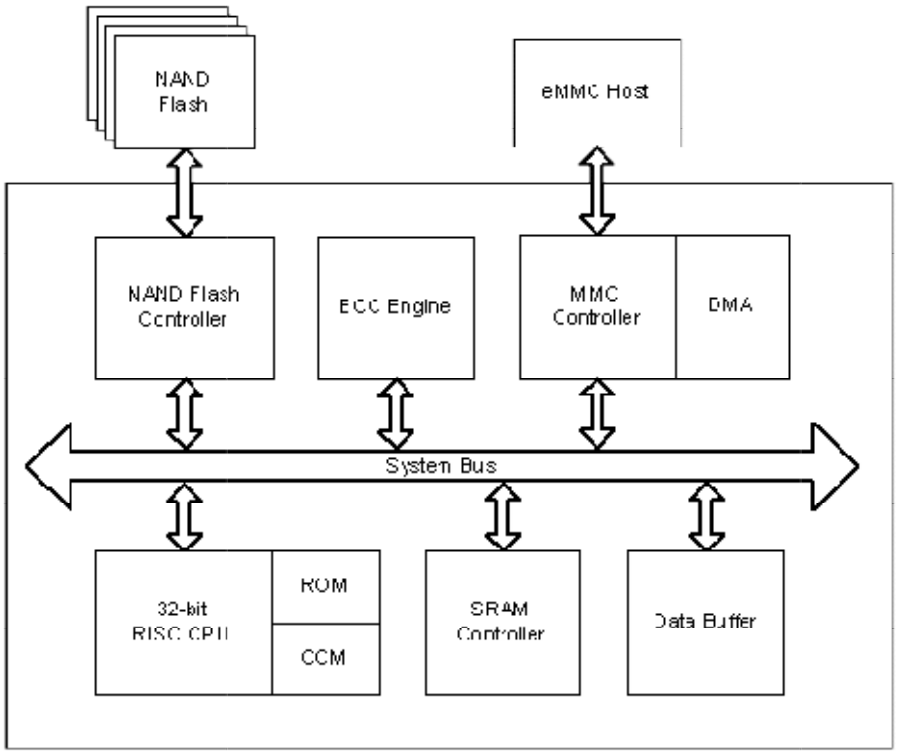


Figure 1-Kimtigoe•MMC I/F Block Diagram

2.Physical Specifications

2.1 153 Ball Pin Configuration

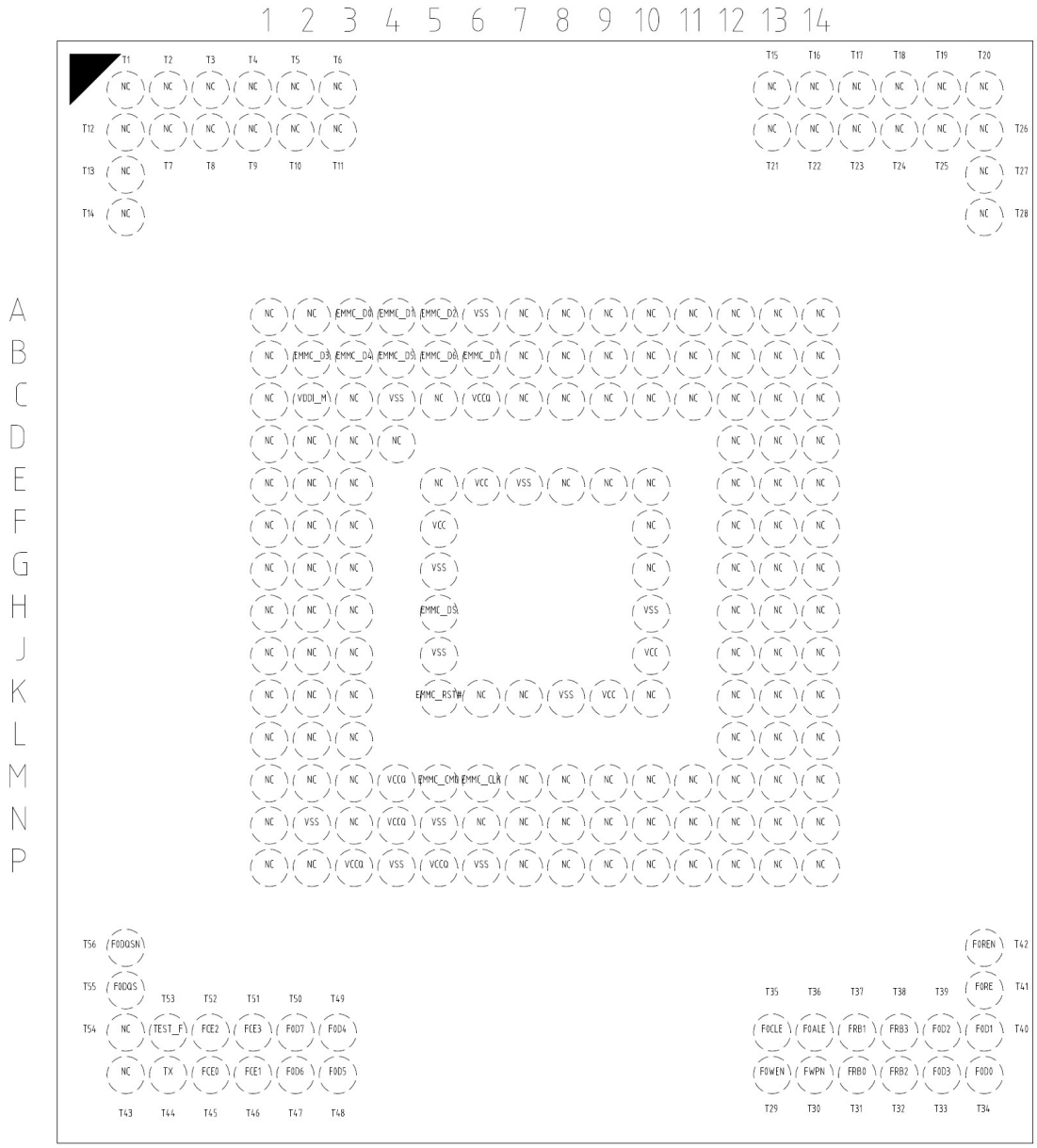


Figure 2-The Kimtigoe•MMC153-Ball FBGA (top view, ball down)

Table 1-153 Ball Information

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A3	DAT0	**C2**	VDDi	**J5**	GND	**N4**	VCCQ
A4	DAT1	**C4**	GND	**J10**	VCC	**N5**	GND
A5	DAT2	**C6**	VCCQ	**K5**	RSTN	**P3**	VCCQ
A6	GND	**E6**	VCC	**K8**	GND	**P4**	GND

B2	DAT3	**E7**	GND	**K9**	VCC	**P5**	VCCQ
B3	DAT4	**F5**	VCC	**M4**	VCCQ	**P6**	GND
B4	DAT5	**G5**	GND	**M5**	CMD		
B5	DAT6	**H5**	STROBE	**M6**	CLK		
B6	DAT7	**H10**	GND	**N2**	GND		

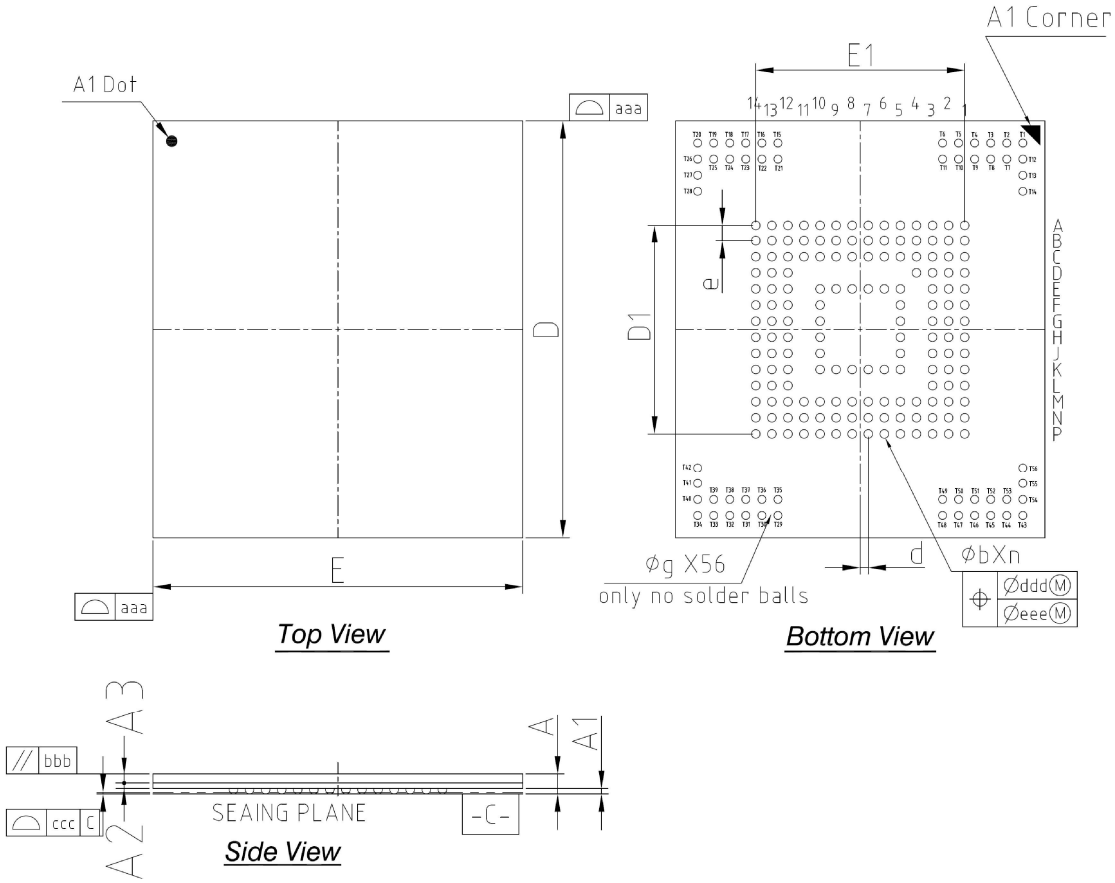
2.2 Pins and Signal Description

Table 2-Pins and Signal Description

Symbol	Type	Ball Function
CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
CMD	Input	Command: A bidirectional channel used for device initialization and command transfer. Command has two operating mode : 1) Open-drain for initialization. 2) Push-pull for fast command transfer.
DAT0	I/O	Data I/O0:Bidirectional channel used for data transfer.
DAT1	I/O	Data I/O1:Bidirectional channel used for data transfer.
DAT2	I/O	Data I/O2:Bidirectional channel used for data transfer.
DAT3	I/O	Data I/O3:Bidirectional channel used for data transfer.
DAT4	I/O	Data I/O4:Bidirectional channel used for data transfer.
DAT5	I/O	Data I/O5:Bidirectional channel used for data transfer.
DAT6	I/O	Data I/O6:Bidirectional channel used for data transfer.
DAT7	I/O	Data I/O7:Bidirectional channel used for data transfer.
RST	Input	Reset signal pin
DS	Output	DS: data strobe
VCC	Supply	VCC:Flash memory I/F and Flash memory power supply.
VCCQ	Supply	VCCQ:Memory controller core and MMC interfaceI/O power supply.
VSS	Supply	VSS:Flash memory I/F and Flash memory ground connection.
VSSQ	Supply	VSSQ: Memory controller core and MMC I/F ground connection
VDDi		VDDi :Connect 1uF capacitor from VDDi to ground.

2.3 11.5mm×13.0mm×1.0mm.maxPackage Dimension

The Kimtigoe•MMC is a 153-pin, thin fine-pitched ball grid array (BGA) and its size is 11.5mm×13.0mm×1.0mm.max.



	Symbol	Dimens or n mm		
		Min	Norir	Max
TOTAL THICKNESS	A	---	---	1.00
STAND OFF	A1	0 18	0.22	0.26
SUBSTRATE THICKNESS	A2	0.19	0.22	0.25
MOLD THICKNESS	A3	0.40	0.42	0.43
BALL DIAMETER(BEFORE)	--		0.30	
BALL OPENING	--		0.27	
Test Pad OPENING	ϕg		0.25	
BALL WIDTH (AFTER)	ϕb	0.25	0.30	0.35
BALL PITCH	e		0.50	
	d		0.25	
BALL COUNT	n		153	
BODY SIZE	D	12.90	13.00	13.10
	E	11.40	11 50	11.60
EDGE BALL CENTER TO CENTER	D1		6.50	
	E1		6.50	
PROFILE OF A SURFACE	aaa		0 15	
MOLD FLATNESS	bbb		0.20	
CO-PLANARITY	ccc		0.20	
BALL OFFSET(PACKAGE)	ddd		0 15	
BALL OFFSET(BALL)	eee		0.10	

Figure 3-11.5mmx13.0mmx1.0mm.max Package Dimension

3.Product Specifications

3.1 Performance

Table 3-Performance

P/N	NAND Type	Density	Withfilesystemoverhead（HS200）		Withoutfilesystemoverhead（HS400）	
			Sequential Read	Sequential Write	Sequential Read	Sequential Write
KM110SS0016GxA-DDD00WT	128 Gb 3D TLC*1	16GB	130MB/s	45MB/s	200MB/s	50MB/s
KM111SS0016GxA-DDD00WT	128 Gb 3D TLC*1	16GB	130MB/s	45MB/s	200MB/s	50MB/s
KM110SS1032GxA-DDD00WT	256 Gb 3D TLC*1	32GB	140MB/s	75MB/s	210MB/s	90MB/s
KM110SS1064GxA-DDD00WT	256 Gb 3D TLC*2	64GB	155MB/s	90MB/s	240MB/s	100MB/s

*Notes:

1.Performancewith file system overheadmeasured by CrystalDiskMark6.0.1.Dviceworkin HS200 mode.

2.Performancewithout file system overheadmeasuredonKimtigo'sinternalboard. Deviceworkin HS400modewithcacheon. Actual performance may vary depending on user conditions and environment.

3.2 User Density

Table 4-User Density

P/N	NAND Type	Density	LBA(Hex)	LBA(Dec)	Capacity(Bytes)

KM110SS0016GxA-DDD00WT	128 Gb 3D TLC*1	16GB	1CD0000	30,212,096	15,468,593,152
KM111SS0016GxA-DDD00WT	128 Gb 3D TLC*1	16GB	1CD0000	30,212,096	15,468,593,152
KM110SS1032GxA-DDD00WT	256 Gb 3D TLC*1	32GB	39A0000	60,424,192	30,937,186,304
KM110SS1064GxA-DDD00WT	256 Gb 3D TLC*2	64GB	7340000	120,848,384	61,874,372,608

3.3 Supply Voltage

Table 5-Supply Voltage

Item	Min	Typ	Max	Unit
VCCQ	1.70	1.80	1.95	V
	2.70	3.30	3.60	V
VCC	2.70	3.30	3.60	V

3.4 Power Consumption

Table 6-Power Consumption

P/N	Item	Typ	Max	Unit
KM110SS0016GxA-DDD00WT	**ICCQ**	70	100	mA
	ICC	70	100	mA
KM111SS0016GxA-DDD00WT	**ICCQ**	70	100	mA
	ICC	70	100	mA
KM110SS1032GxA-DDD00WT	**ICCQ**	90	110	mA
	ICC	80	100	mA
KM110SS1064GxA-DDD00WT	**ICCQ**	90	110	mA
	ICC	160	200	mA

4.e•MMC Interface

4.1 e•MMCPower Up

An e•MMC bus power-up is handled locally in each device and in the bus master. Figure 3 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 10.1 of the JEDEC Standard Specification No.JESD84-B50 for specific instructions regarding the power-up sequence.

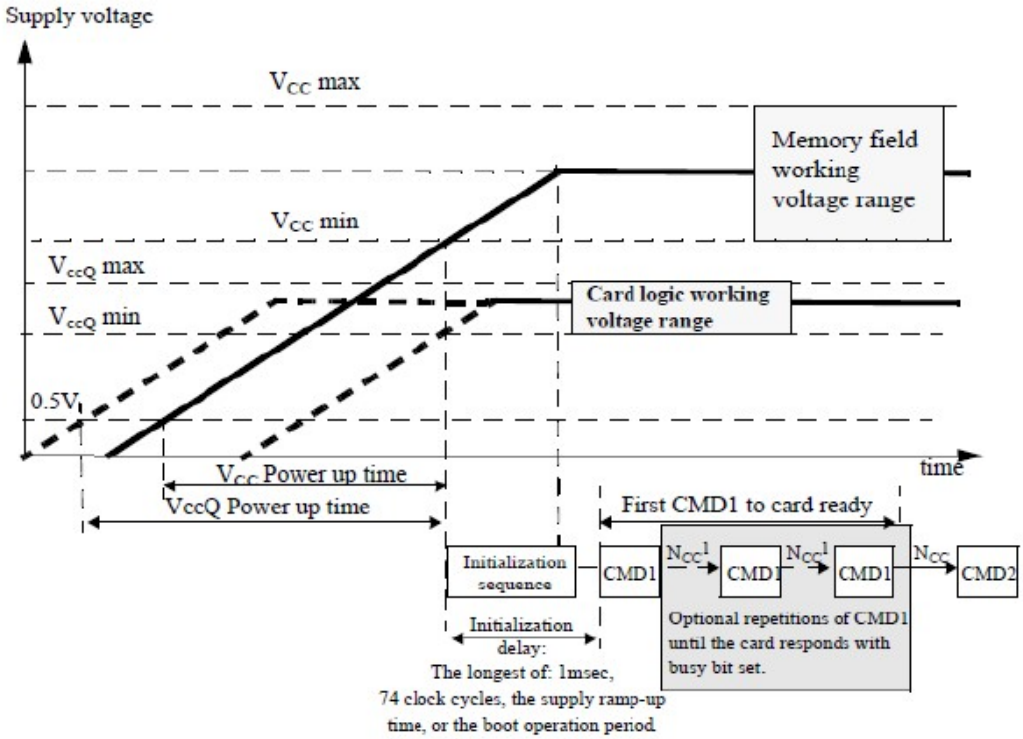


Figure 4-e•MMC Power-up Diagram

4.2 e•MMC Power Cycling

The master can execute any sequence of VCC and VCCQ power-up/power-down. However, the master must not issue any commands until VCC and VCCQ are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down VCC to reduce power consumption. It is necessary for the slave to be ramped up to VCC before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit. For more information about power cycling see Section 10.1.3 of the JEDEC Standard Specification No.JESD84-B50.

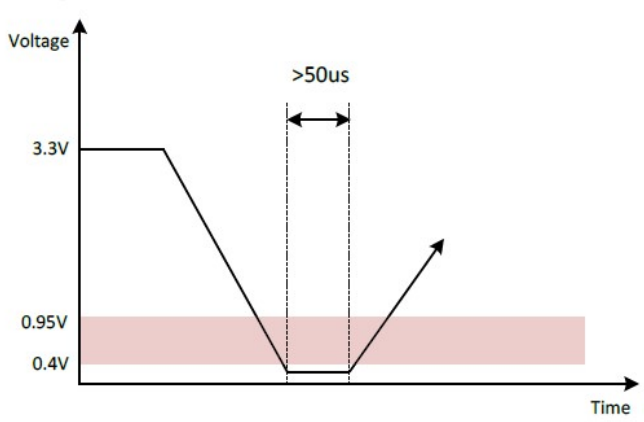


Figure 4-The e•MMCPower Cycle

4.3 Bus Signal Line Load

The total capacitance C_L of each line of the eMMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of the eMMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

Table 7-Bus Signal Line Load

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	100	Kohm	Pull-up resistance should be put on CMD line to prevent bus floating.
Pull-up resistance for DAT0~7	R_{DAT}	10	100	Kohm	Pull-up resistance should be put on DAT line to prevent bus floating.
Internal pull-up resistance for DAT1~7	R_{int}	10	150	Kohm	To prevent unconnected lines floating.
Single device capacitance	C_{DEVICE}		12	pF	
Maximum signal line inductance			16	nH	Fpp≤52MHz
VDDi capacitor value	C_{REG}	0.1		uF	Tostabilizeregulatoroutputwhentargetdevicebusspeedmodeisitherbackward-compatible, highspeed SDR, highspeed DDR, or HS200.
		1		uF	Tostabilizeregulatoroutputwhentargetdevicebusspeedmodeis

					HS400.

Table 8-Capacitance and Resistance for HS400 mode

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	100	Kohm	To prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10	100	Kohm	To prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10	150	Kohm	To prevent unconnected lines floating
Bus signal line capacitance	C_L		13	pF	Single Device
Single Device capacitance	C_{DEVICE}		6	pF	
Pull-down resistance for Data strobe	$R_{Data\ Strobe}$	10	100	Kohm	

5.Register Value

5.1 OCR Register

The 32-bit operation conditions register stores the VDD voltage profile of the e•MMC and the accessmode indication. In addition, this register includes a status information bit. This status bit is set if the e•MMC power up procedure has been finished.

Table 9-OCR Register Definitions

OCR bit	VDD voltage window	Value	Width
[31]	e.MMC power up status bit (busy)1=READY		
[30:29]	Access mode	10b (sector mode)	2
[28:24]	Reserved	0 0000b	5
[23:15]	2.7–3.6V	1 1111 1111b	9
[14:8]	2.0–2.6V	000 0000b	7
[7]	1.70–1.95V	1b	1
[6:0]	Reserved	0000000b	7

5.2 CID Register

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information usedduring the e•MMC identification phase (MultiMediaCard protocol). Each device has a unique identification number.

The structure of the CID register is defined in the following sections.

Table 10-CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0xE1
Reserved	-	6	[119:114]	---
Card/BGA	CBX	2	[113:112]	0x01
OEM/Application ID	OID	8	[111:104]	---
Product name	PNM	48	[103:56]	16GB:0x0000,2100,0105 32GB:0x0000,3200,0105 64GB:0x0000,3300,0105
Product revision	PRV	8	[55:48]	---
Product serial number	PSN	32	[47:16]	---
Manufacturing date	MDT	8	[15:8]	---
CRC7 checksum	CRC	7	[7:1]	---

Not used; always 1	---	1	0	---

5.3 CSD Register

The card-specific data (CSD) register provides information about accessing thee•MMCcontents. The CSD register defines the data format, error correction type, maximum dataaccess time, and data transfer speed, as well as whether the DSR register can be used.The programmable part of the register (entries marked with W or E in the following table)can be changed by the PROGRAM_CSD (CMD27) command.

R: Read only.

W: One time programmable and not readable.

R/W: One time programmable and readable.

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 resetand not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 resetand readable.

R/W/C_P: Writable after value cleared by power failure and H/Wrest assertion (the value not cleared byCMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0reset and readable.

W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0reset and not readable.

Table 11-CSD Register

Name	Field	Width	Cell Type	CSD slice	CSD Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03
Systemspecification version	SPEC_VERS	4	R	[125:122]	0x04
Reserved	-	2	R	[121:120]	0x00
Data read access-time 1	TAAC	8	R	[119:112]	0x27
Data read access-time 2in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x01
Max. busclock frequency	TRAN_SPEED	8	R	[103:96]	0x32
Device command classes	CCC	12	R	[95:84]	0x0F5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00
DSR implemented	DSR_IMP	1	R	[76:76]	0x00

Reserved	-	2	R	[75:74]	0x00
Device size	C_SIZE	12	R	[73:62]	0xFFF
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x07
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x07
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x07
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x07
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x0F
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x00
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x02
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00
Reserved	-	4	-	[20:17]	0x00
Contentprotection application	CONTENT_PROT_APP	1	R	[16:16]	0x00
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x00
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00
File format	FILE_FORMAT	2	R/W	[11:10]	0x00
ECC code	ECC	2	R/W/E	[9:8]	0x00
CRC	CRC	7	R/W/E	[7:1]	TBD
Not used, always'1'	--	1	—	[0:0]	0x01

5.4 Extend CSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties andselected modes. The most significant 320 bytes are the properties segment. This segmentdefines devicecapabilities and cannot be modified by the host. The lower 192bytes

are the modes segment. The modes segment defines the configuration in whichthe device is working. The host can change the properties of modes segments using theSWITCH command.

Table 12-Extend CSD Register

Name	Field	Size	Cell Type	CSD-slice	ECSD Value
Reserved	-	6	-	[511:506]	-
Extended Security CommandsError	EXT_SECURITY_ERR	1	R	[505]	0x00
Supported Command Sets	S_CMD_SET	1	R	[504]	0x01
HPI Features	HPI_FEATURES	1	R	[503]	0x01
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	0x01
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0x00
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0x00
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x78
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x01
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03
Supported modes	SUPPORTED_MODES	1	R	[493]	0x01
FFU features	FFU_FEATURES	1	R	[492]	0x00
Operation codes timeout	OPERATION_CODE_TIME_OUT	1	R	[491]	0x17
FFU Argument	FFU_ARG	4	R	[490:487]	0xFFFAFFF0
Barriersupport	BARRIER_SUPPORT	1	R	[486]	16GB:0x00 32GB:0x01 64GB:0x01
Reserved	-	177	-	[485:309]	-
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	16GB:0x00 32GB:0x01

					64GB:0x01
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	16GB:0x00 32GB:0x1F 64GB:0x1F
Reserved	-	1	-	[306]	-
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0x0000
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	TBD
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0x01
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0x01
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x01
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x40
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x40
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x07
Device version	DEVICE_VERSION	2	R	[263:262]	16GB:0x4105 32GB:0x4205 64GB:0x4305
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	TBD
Power class for 200MHz,DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x00
Cache size	CACHE_SIZE	4	R	[252:249]	0x0400
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x05
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x64
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
1st Initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x0A

Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	0x01
Power class for 52MHz, DDR at VCC=3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00
Power class for 52MHz, DDR at VCC=1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00
Power class for 200MHz at VCCQ=1.95V,VCC =3.6V	PWR_CL_200_195	1	R	[237]	0x00
Power class for 200MHz, at VCCQ=1.3V,VCC= 3.6V	PWR_CL_200_130	1	R	[236]	0x00
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00
Reserved	-	1	-	[233]	-
TRIM Multiplier	TRIM _MULT	1	R	[232]	0x02
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x0A
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x0A
Boot Information	BOOT_INFO	1	R	[228]	0x07
Reserved	-	1	-	[227]	-
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	0x20
Access size	ACCESS_SIZE	1	R	[225]	0x06
High Capacity Erase unit size	HC_ERASE_GROUP_SIZE	1	R	[224]	0x01
High capacity erase time out	ERASE_TIMEOUT_MULT	1	R	[223]	0x02

Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01
High capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	16GB:0x10 32GB:0x10 64GB:0x20
Sleep current [VCC]	S_C_VCC	1	R	[220]	0x07
Sleep current [VCCQ]	S_C_VCCQ	1	R	[219]	0x07
Production state awareness timeout	PRODUCTION_STATE_ AWARENESS_TIMEOUT	1	R	[218]	0x17
Sleep/Awake time out	S_A_TIMEOUT	1	R	[217]	0x13
Sleep Notification Timout1	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x0C
Sector count	SEC_COUNT	4	R	[215:212]	16GB: 0x01CD0000 32GB:0x039A 0000 64GB: 0x07340000
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0x01
Minimum Write Performance for 8bit @52MHz	MIN_PERF_W_8_52	1	R	[210]	0x00
Minimum Read Performance for 8bit @52MHz	MIN_PERF_R_8_52	1	R	[209]	0x00
Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00
Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00
Minimum Write Performance for 4bit @26MHz	MIN_PERF_W_4_26	1	R	[206]	0x00

Minimum Read Performance for 4bit @26MHz	MIN_PERF_R_4_26	1	R	[205]	0x00
Reserved	-	1	-	[204]	-
Power Class for 26MHz @ 3.6V 1R	PWR_CL_26_360	1	R	[203]	0x00
Power Class for 52MHz @ 3.6V 1R	PWR_CL_52_360	1	R	[202]	0x00
Power Class for 26MHz @ 1.95V 1R	PWR_CL_26_195	1	R	[201]	0x00
Power Class for 52MHz @ 1.95V 1R	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x06
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x05
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	0x1F
Card Type	CARD_TYPE	1	R	[196]	0x57
Reserved	-	1	-	[195]	-
CSD Structure	CSD_STRUCTURE	1	R	[194]	0x02
Reserved	-	1	-	[193]	-
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	16GB:0x07 32GB:0x08 64GB:0x08
Command Set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved	Reserved	1	-	[190]	-
Command Set Revision	CMD_SET_REV	1	R	[189]	0x00
Reserved	Reserved	1	-	[188]	-
Power Class	POWER_CLASS	1	R/W/E_P	[187]	0x00
Reserved	Reserved	1	-	[186]	-
High Speed Interface Timing	HS_TIMING	1	R/W/E_P	[185]	0x01
Strobe Support	STROBE_SUPPORT	1	R	[184]	16GB:0x00 32GB:0x01 64GB:0x01
Bus Width Mode	BUS_WIDTH	1	W/ E_P	[183]	-
Reserved	Reserved	1	-	[182]	-

Content of explicit erased memory range	ERASE_MEM_CONT	1	R	[181]	0x00
Reserved	Reserved	1	-	[180]	-
Partition Configuration	PARTITION_CONFIG	1	R/W/E_P& R/W/E	[179]	0x00
Boot config protection	BOOT_CONFIG_PROT	1	R/W& R/W/C_P	[178]	0x00
Boot bus width1	BOOT_BUS_WIDTH	1	R/W/E	[177]	0x00
Reserved	Reserved	1	-	[176]	-
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x00
Boot area write protect register	BOOT_WP	1	R/W& R/W/C_P	[173]	0x00
Reserved	Reserved	1	-	[172]	-
User area write protect register	USER_WP	1	R/W/E&R/ W& R/W/C_P	[171]	0x00
Reserved	Reserved	1	-	[170]	-
FW Configuration	FW_CONFIG	1	R/W	[169]	0x00
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x20
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	16GB:0x05 32GB:0x15 64GB:0x15
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00
Partitioning	PARTITIONING SUPPORT	1	R	[160]	0x07

support					
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	16GB:0x0266 32GB:0x04CD 64GB:0x04CD
Partitions Attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00
Partitioning Setting	PARTITION_SETTING_ COMPLETED	1	R/W	[155]	0x00
General Purpose Partition Size	GP_SIZE_MULT	12	R/W/	[154:143]	0x00
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0
Reserved	Reserved	1	-	[135]	-
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00
Production state awareness	PRODUCTION_STATE_ AWARENESS	1	R/W/E	[133]	0x00
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_ SUPPORT	1	R	[130]	0x00
Reserved	–	2	TBD	[129:128]	-
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	vendor specific	[127:64]	0x3700C8 (Value of EMMC_SET_D URATION)
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x01
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x0A
Class 6	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00

commands control					
Number of addressed groupto be Released	DYNCAP_NEEDED	1	R	[58]	0x00
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x00
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00
Packed command failureindex	PACKED_FAILURE_INDEX	1	R	[35]	0x00
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00
Control to turn the CacheON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x00
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0x00
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00
Reserved	Reserved	2	TBD	[28:27]	-
FFU status	FFU_STATUS	1	R	[26]	0x00
Per loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x00
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	16GB: 0x01CD0000 32GB:0x039A 0000 64GB: 0x07340000
Product state	PRODUCT_STATE_AWARENESS_	1	R/W/E & R	[17]	0x01

awareness enablement	ENABLEMENT				
Secure removal type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x3B
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0x00
Reserved	-	15	-	[14:0]	-

6.Ordering Information

Part Number	Description
KM110SS0016GxA-DDD00WT	11.5mm x 13.0mm x 1.0mm.max 16GB e•MMC *v5.1* 153-ball FBGA
KM111SS0016GxA-DDD00WT	11.5mm x 13.0mm x 1.0mm.max 16GB e•MMC *v5.1* 153-ball FBGA
KM110SS1032GxA-DDD00WT	11.5mm x 13.0mm x 1.0mm.max 32GB e•MMC *v5.1* 153-ball FBGA
KM110SS1064GxA-DDD00WT	11.5mm x 13.0mm x 1.0mm.max 64GB e•MMC *v5.1* 153-ball FBGA