5W WPC Wireless Power Receiver

Features

- Single Chip WPC1.2.4 Wireless Power Receiver for 5W application
- Vrect Range: 4-24V Operational, 28V Max
- 5W Maximum Output Power
- Fully Synchronous Rectifier Optimized for Multi-Mode Operation
- Integrated Buck Regulator with Fine Vout Steps and High-Efficiency Bypass Mode
  - Range 1: 4.940-10.040V in 20mV steps
  - Range 2: 3.952-8.032V in 16mV steps
- Comprehensive Power Regulation
  - Output Current Regulation in CC Mode
    - 100mA to 1000mA in 50mA steps
    - 1000mA to 2200mA in 100mA steps
  - Input Impedance Regulation to Maintain Vrect Voltage
- Very Low Standby Current: 7μA Typical
- I^2C Interface with SM, FM and FM^+ Modes
  - Optional PSNS Generation for Downstream 6-channel ADC for Comprehensive Power and Temperature Monitoring
  - Programmable Input and Output Power Regulation
  - Output Over-Current Protection (OCP)
  - Vrect Over-Voltage Protection (OVP)
  - Over Temperature Protection (OTP)
- 5mm x5mmQFN-32 (QFN)

Applications

- Mobile Devices
- Wireless Charging Accessories

Order Information

Part Number	Device ID	I2C Address	Max Output Power	Max Input Current	Vout Range	Package	Packing Method
HL6111RFNWP55	0x10	0011000	5W	1.0A	5V	QFN	Tape & Reel
HL6111RFNWP5C	0x01	0011000	5W	1.2A	5V	QFN	Tape & Reel

For other options, contact a Halo Micro sales representative.

Typical Application Diagram

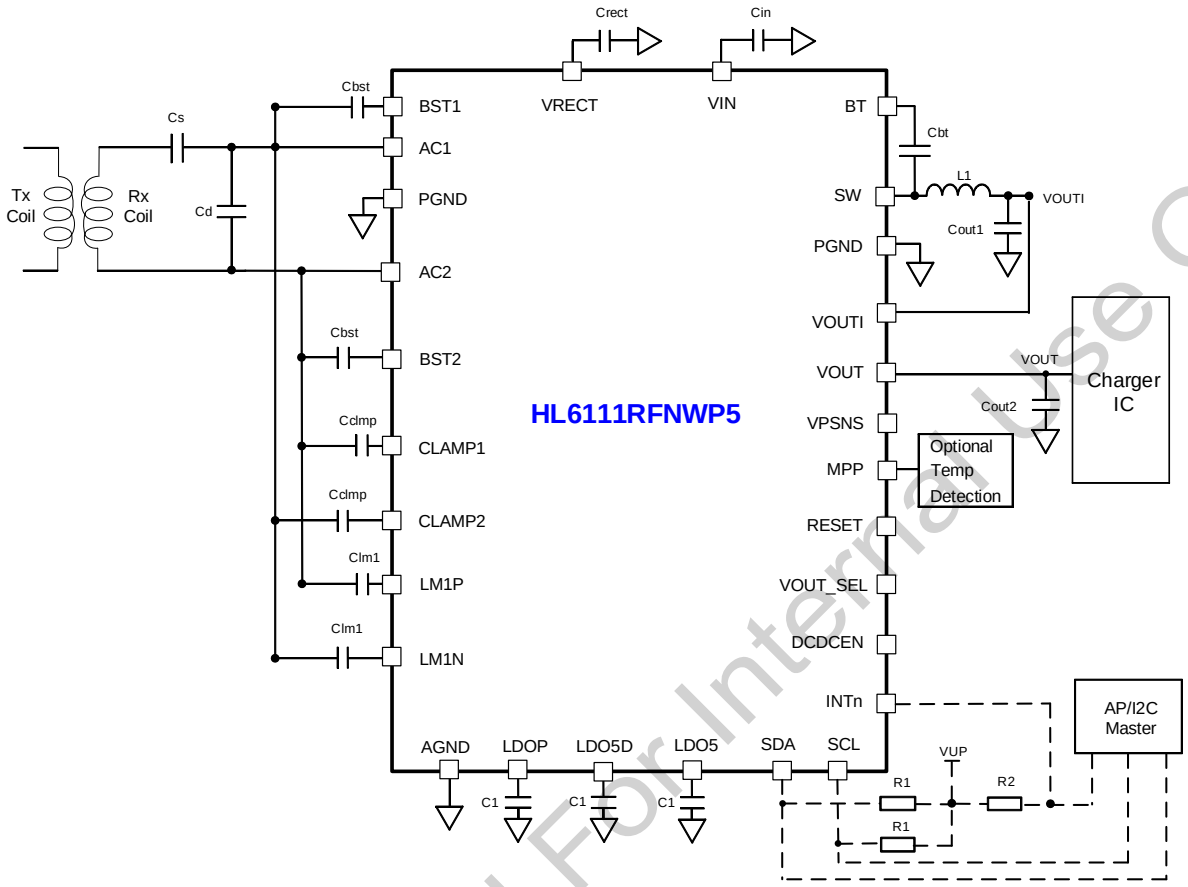


Figure 1 HL6111RFNWP5 Typical Application and Functional Diagram

Component	Part Number	Value	Size	Vendor
L1	See Table2	1uH-2.2uH	2016	See Table2
Crect	C2012JB1H475K125AB	4.7uF /50V	0805	TDK
Cin	C2012JB1H475K125AB	4.7uF /50V	0805	TDK
Cout1	C2012JB1H105K085AB	1uF /50V	0805	TDK
Cout2	C2012JB1H475K125AB	4.7uF /50V	0805	TDK
Cbt	CGJ3E2X7R1C104K080AA	47nF-100nF /10V	0603	TDK
C1	C1608JB1A105K080AC	1uF-4.7uF /10V	0603	TDK
Cbst	CGJ3E2X7R1C333K080AA	33nF /10V	0603	TDK
Cclmp	C2012X6S1H474M125AB	470nF /50V	0805	TDK
Clm1	C2012C0G1H223J125AA	22nF /50V	0805	TDK
Clm2	C2012X8R1H683K125AA	68nF /50V	0805	TDK
R1	--	2.2-4.7kΩ	--	--
R2	--	2.2-4.7kΩ	--	--

Table 1 Recommended External Components

Manufacturer	Part Number	L (uH)	DCR(mΩ)	I_{MAXDC} (1)	Component Dimension		
					L（mm）	W（mm）	H（mm）
MURATA	DFE252012F-1R0M	1	40	4.7	2.5	2.0	1.2
CYNTEC	HMLQ20161B-1R0MDR	1	50	3.0	2.0	1.6	1.0

Table 2 Recommended Inductors

Manufacturer	Part Number	L(uH)	DCR(mΩ)	Q-Factor	Component Dimensions		
					L（mm）	W（mm）	H（mm）
SUNLORD	MQQRR505012S8R2IDD	8.2	85	60	50	50	1.2
LINE PRINTING	Y01	8.5	326	16	48	48	0.26

Table 3 Recommended Receiver Coils

Notes:

1. I_{MAXDC} is the smaller current to produce 40°C temperature rise or 30% effective inductance reduction.

Description

HL6111RFNWP5 is a highly integrated wireless charging power receiver IC that is compatible with popular wireless charging power delivery standards: Wireless Power Consortium V1.2.4 (WPC/Qi) standard. It integrates a fully synchronous rectifier and a high-performance buck post regulator with bypass mode to deliver a maximum of 5W with best-in-class conversion efficiency, while providing maximum design flexibility between the wireless charging receiver (Rx) coil design and output voltage to match down-stream Li-Ion battery charge ICs.

The output voltage of HL6111RFNWP5 can be programmed with fine steps of 16mV/20mV to accommodate a wide variety of Li-ion battery chargers, including switch-mode chargers and charge-pump chargers. It also includes output constant-current (CC) mode in steps of 50mA/100mA for ease of usage. On the input side, an input impedance control scheme is included so that the Rx coil output voltage Vrect does not collapse when output load is suddenly increased. As an option, HL6111RFNWP5 also provides a PSNS output voltage which is proportional to its output current or power, so that down-stream charger can use this information to control its power delivery to the battery.

A 6-channel 10b ADC monitors the input and output power, die temperature, etc. information, as well as an external MPP channel to ensure safe operation under different operational modes and power conditions. The IC also includes input over-voltage, output over-current, die over-temperature and coil over-temperature protection mechanism.

HL6111RFNWP5 includes an I2C interface with SM, FM and FM+ support, a highly flexible digital processing unit and one-time-programmable (OTP) memory cells so that system level controllability, programmability and flexibility are maximized.

The HL6111RFNWP5 is available in a 5mm x 5 mm 32-pin QFN.

Functional Block Diagram

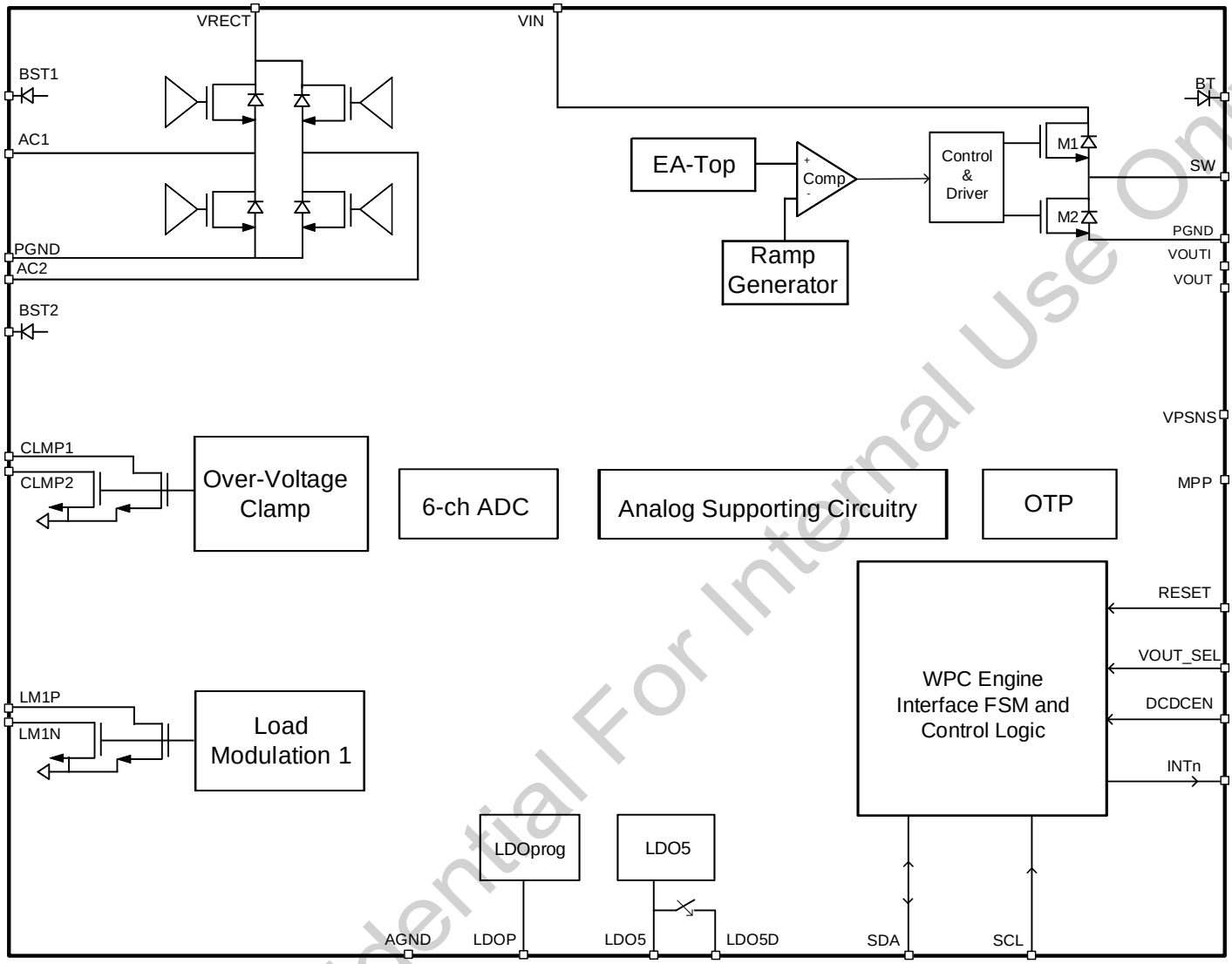


Figure 2 HL6111RFNWP5 Internal Functional Block Diagram

Pin Diagram

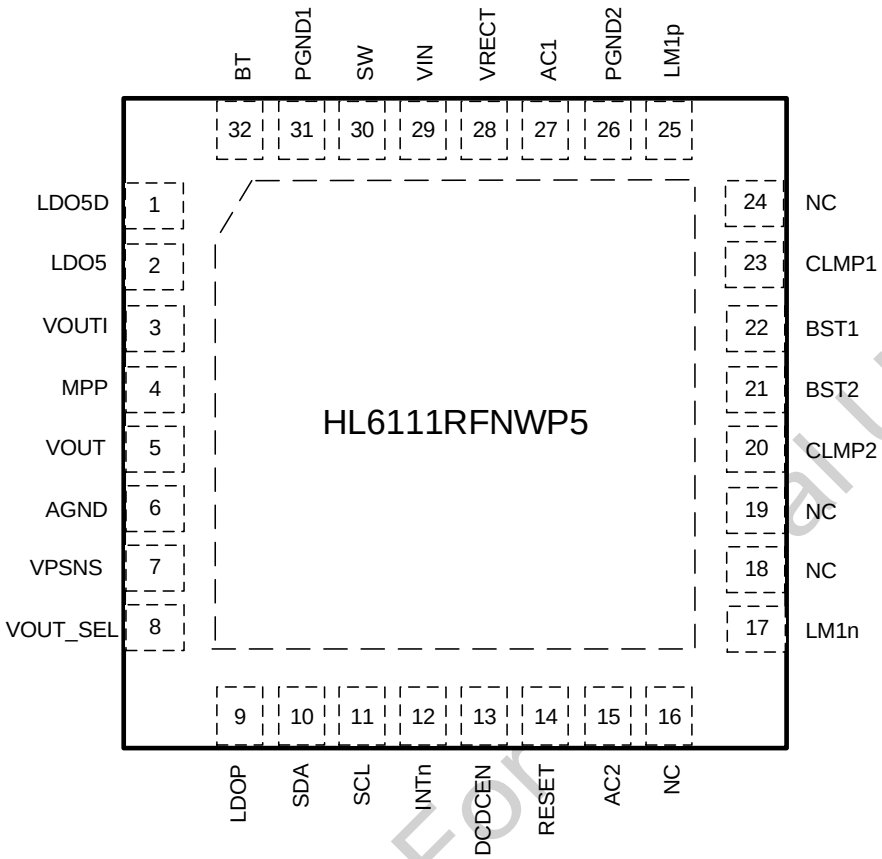


Figure 3 HL6111RFNWP5 Pin-out Diagram, Top View

Pin Description

Pin Name	Vmax or Voltage Range	Analog, Power, or I/O/IO	Pin #	Description
AC1, AC2	**28**	**Power**	**27,15**	Full synchronous rectifier power input pins
BST1, BST2	**AC1/2+5.5**	**Power**	**22,21**	Full synchronous rectifier boot pins
CLMP1, CLMP2	**28**	**Power**	**23,20**	Overvoltage clamp switch outputs
LM1p, LM1n	**28**	**Power**	**25, 17**	WPC/PMA load modulation switches
VRECT	**28**	**Power**	**28**	Full synchronous rectifier output voltage bypass pin
VIN	**28**	**Power**	**29**	Buck regulator bypass pin. Internally shorted with VRECT pin
SW	**28**	**Power**	**30**	Buck regulator switch node. Connect to the inductor
BT	**SW+5.5**	**Power**	**32**	Buck regulator boot driver pin
VOUTI	**28**	**Analog**	**3**	Buck output, Iout sense positive node
VOUT	**28**	**Analog**	**5**	Buck output feedback node, Iout sense negative node
LDO5	**5.5**	**Power**	**2**	Internal 5V regulator bypass pin
LDO5D	**5.5**	**Power**	**1**	Qualified 5V regulator as down-stream PON signal
LDOP	**5.5**	**Power**	**9**	Internal LDO with programmable output voltage: 1.2V, 1.8V(default), 2.5V, 3.3V
PGND1,PGND2	**0**	**Power**	**31,26**	Power ground
AGND	**0**	**Power**	**6**	Analog ground
VPSNS	**0-3.3, 5.5**	**Analog output**	**7**	Feed forward voltage feedback for downstream input current loop
MPP	**0-5, 5.5**	**Analog input/output**	**4**	Multi-purpose input port that is connected to internal ADC.
VOUT_SEL	**Low: 0, High: LDOP, Max: 5.5**	**IO**	**8**	function: input to enable forced 5V Vout for OTG mode: =0: force buck mode and Vout=5V; =1: allow internal logic to decide Vout value 250kΩ pull-up to LDOP
DCDCEN	**Low: 0, High: LDOP, Max: 5.5**	**I**	**13**	DCDC post regulator enable pin, 300kohm pull down to GND. =0: regulator disabled; =1: regulator enabled 250kΩ pull-down
INTn	**Open-drain, Max: 5.5**	**O**	**12**	Interrupt output, open drain, active low
SCL, SDA	**Low: 0, High: 1.8 Max: 5.5**	**I, IO**	**11,10**	I2C clock and data lines. These two pins are pulled down to 0V.
RESET	**Low: 0, High: LDOP, Max: 5.5**	**I**	**14**	IC logic reset input: =1 resets entire chip, 270kohm pull down to GND.

Table 4 HL6111FNWP5 Pin Definition

Absolute Maximum Ratings (1)

AC1/2, LM1p/n, CLMP1/2, VRECT, VIN, SW, VOUTI, VOUTO pin voltage:

IC Not Switching ---------- −0.7V ~ 28V

IC Switching ---------- −0.7V ~ 24V

BST1, BST2 pin voltage ---------- −0.3V ~ AC1/2+5.5V

BT pin voltage ---------- −0.3V ~ SW+5.5V

All other pin voltage: ---------- −0.3V ~ 5.5V

Junction-to-ambient thermal resistance ---------- 45(TBD)℃/W

Junction-to-case thermal resistance ---------- 0.20(TBD)℃/W

Junction temperature T_J ---------- −40℃ ~ 150℃

Storage temperature T_{stg} ---------- −65℃ ~ 150℃

Lead soldering temperature T_L(10s) ---------- 260℃

ESD: HBM ---------- 2000V

ESD: CDM ---------- 500V

ESD: Latch-up ---------- ±100mA

Recommended Operating Conditions (2)

Supply voltage, VRECT ---------- 4V ~ 24V

Output current, IOUT ----------0 ~ 1.2A

Operating free-air temperature T_A ---------- −40℃ ~ 85℃

Junction temperature T_J ---------- −40℃ ~125℃

Note

(1) Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device.

(2) Functional operation of the device at any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltage values are defined at ambient temperature range from -40℃ to +85℃ unless otherwise noted.

Electrical Specification

Minimum and maximum values are at Vrect=5-24V, T_A=-40°C~+85°C, unless otherwise noted. Typical values are at T_A=25°C, V_{rect} =9V, L1=1.0uH

Symbol	Parameter		Min.	Typ.	Max	Unit
Power Supplies						
I_Q	Quiescent Current	Digital running, I_{LOAD}=0, APFM		2		mA
		Digital running, I_{LOAD}=0, Forced PWM		20		mA
I_{SB}	Standby Current	Only Vout has power, IC standby, Vout=4.5V		7		μA
I_{StndBy_LDO}	Standby current when LDO5 block is enabled with 0-load current	LDO5		110		uA
		LDOP		110		uA
V_{REG_LDO5}	LDO5 output DC accuracy	Vin>=6.0V	4.7	5.0	5.5	V
I_{OCP_LDO5}	LDO5 output over-current protection Threshold			150		mA
V_{REG_LDO5D}	LDO5D output DC accuracy	Vin>=6.0V	4.5	5.0	5.5	V
I_{MAX_LDO5D}	LDO5D maximum current loading				20	mA
R_{on_LDO5D}	Switch resistance between LDO5 and LDO5D	VLDO=5V		1.1	1.6	Ω
V_{REG_LDOP}	LDOP output DC accuracy	V_{LDOP} output set at 1.2V, 1.8V,2.5V, 3.3V. Iload= 0-30mA	-4%	0	+2%	V
I_{OCP_LDOP}	LDOP output over-current protection Threshold			70		mA
I_{OCP_HYST}	LDO output OCP hysteresis	Release current as a percentage of trigger current		(TBD)		%
Logic I/O pins, LDOP domain: VOUT_SEL, DCDCEN						
V_{IH}	High-Level Input Voltage		0.67* LDOP			V
V_{IL}	Low-Level Input Voltage				0.22* LDOP	V
I_{INIO_LDOP}	Input Bias Current:	Input tied to LDOP		0.01	1	μA
Logic I/O pins, fixed: SCL, SDA						
V_{IH}	High-Level Input Voltage		1.2			V
V_{IL}	Low-Level Input Voltage				0.5	V
I_{INIO_LDO5}	Input Bias Current:	Input tied to 1.8V		0.01	1	μA
Synchronous Rectifier Section						
Ronsr	Synchronous rectifier FET resistance	Vrect=8V		90		mΩ

F_sr	Synchronous rectifier operating frequency		80		8000	kHz
Buck and Bypass Section						
Vout	Vout range			5.1		V
V_{REG}	V_{OUT} DC Accuracy	$I_{OUT(DC)}$=0, buck in forced PWM, Vout=5.0V, Vin=9V	-1.5		1.5	%
		V_{OUT} = 5V-12V, $I_{OUT(DC)}$=0-2.0A, Buck in forced PWM	-2.0		2.0	%
$\frac{\Delta V_{OUT}}{\Delta I_{LOAD}}$	Load Regulation	$I_{OUT(DC)}$=0 to 2A, FPWM		-0.3		%/A
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	6V≤V_{RECT}≤24V, $IOUT_{(DC)}$=0.5 A, FPWM		-0.1		%/V
I_{q_buck}	Buck power consumption, excluding support circuitry like BG, bias, oscillator etc	PFM mode, Iload=0, Vin=9V, Vout=5V		50		uA
		PWM mode, Iload=0, Vin=9V, Vout=5V		18		mA
F_{PWM}	PWM switching frequency		1.23	1.37	1.51	MHz
t_{SS}	Soft-start Time, from Enable to Regulated V_{OUT}	R_{LOAD} > 5Ω; V_{OUT}=5V (95%)		1		ms
I_{LIMPK}	Buck High-Side Peak Current Limit	DC trigger point	2.9	3.2	3.5	A
I_{LIM_BP}	Bypass FET Current Limit	DC trigger point	2.1	2.5	2.9	A
I_{RECT_TARGET}	Vrect current regulation target	Register programmable	200		2000	mA
V_{th_BPsw}	Bypass exit threshold, rising edge	Vrect target value set by register,		5.1		V
V_{hyst_BPsw}	Bypass entry/exit hysteresis			0.5		V
Protection						
T_{LIMIT}	Thermal Shutdown			149		°C
T_{HYST}	Thermal Shutdown Hysteresis			22		°C
V_{UVLO1}	Vrect Under-Voltage Lockout 1 Threshold	Rising edge		4.0		V
$V_{UV1HYST}$	Vrect Under-Voltage Lockout 1 Hysteresis			1.0		V
V_{UVLO2}	Vrect Under-Voltage Lockout 2 Threshold	Rising edge		4.5		V
$V_{UV2HYST}$	Vrect Under-Voltage Lockout 2 Hysteresis			1.1		V
V_{OVP_VRECT}	Vrect Over-Voltage	Rising Threshold, programmable	19.4	22.9	22.9	V
		Falling Threshold	6.5	7.0	7.5	V

Multiple-channel ADC						
VFS_{ADC}	ADC Full-scale range			1.8		V
	Resolution			10		Bits
$Freq_{ADC}$	ADC sampling clock rate		-2%	220	+2%	kHz
	Differential Nonlinearity	Monotonicity guaranteed by design.			1.0	LSB
Clock Reference						
$Freq_{clk}$	On-chip reference clock frequency		-2%	11	+2%	MHz
Detuning Switch Drivers						
T_{dly_dsw}	Delay from VRECT> $V_{th\_dsw\_rising}$ to DSW gate voltage reaches 90% of final value(5V)	Vrect rising edge: 0.4V/100ns 1.5nF load		500		ns

Table 5 Electrical Specification

Typical Characteristics

The following performance characteristics were taken using a 5W WPC V1.2.4-compliant wireless power transmitter at T_A = 25°C unless otherwise noted.

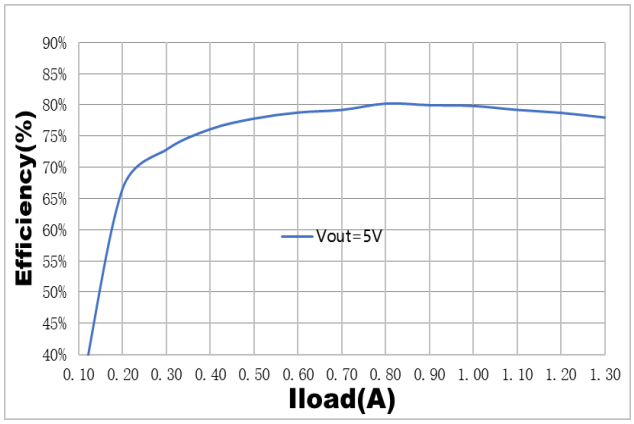


Figure 4 Efficiency vs. Output Load: VOUT = 5V

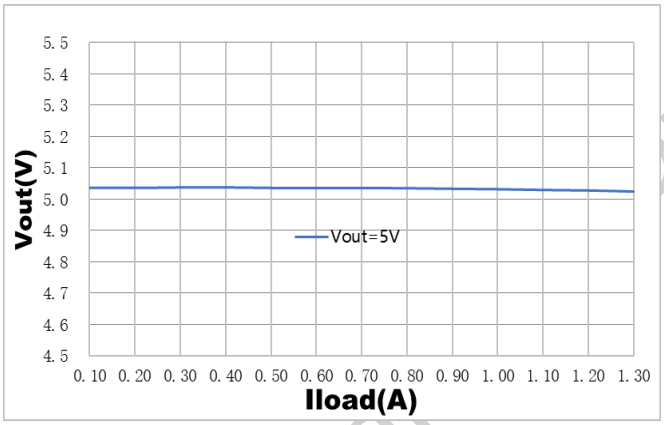


Figure 5 Load Reg. vs. Output Load: VOUT = 5V

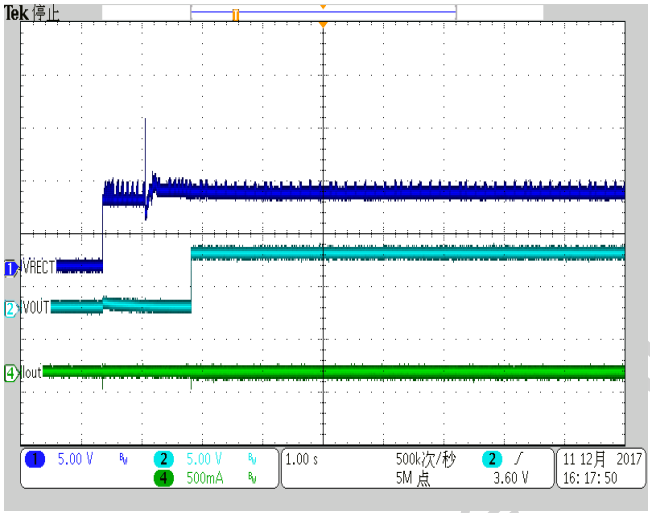


Figure 6 Enable Startup: VOUT = 5V

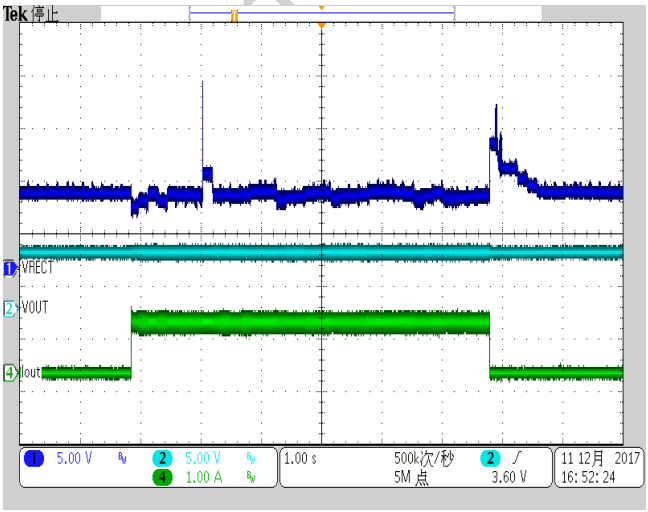


Figure 7 Load Transient: VOUT = 5V; IOUT = 0 -> 1.0A ->0A

Detailed Description

Power Detection and Validation

HL6111RFNWP5 takes power from its Vin pin. Vin can be powered up by two sources: a wireless charging source on AC1/AC2 pins supplying power to Vrect pin via the full-wave rectifier, or from Vout pin through the body diodes of the buck HS FET M1. Vout is connect to the PMID node of the down-stream charger which has non-zero voltage when the charger is connected to a battery or an USB source.

HL6111RFNWP5 detects which source is connected by comparing Vrect and Vout voltage level using a Vrect_Vout comparator. If Vrect > Vout, a wireless charging source is detected. The LDO5 regulator is enabled to power up the voltage reference and bias block. After that the Vrect comparator block is enabled to detect whether Vrect has risen over Vrect_UV1 threshold. Once Vrect_UV1 is clear, the entire chip powers up. If Vrect < Vout, the chip stays powered down, consuming minimum standby power. If a wireless charger is plugged in, but its detected output voltage Vrect is less than Vout, then it will be ignored and the chip still stays in power-down state.

On-Chip Power Supply

LDO5

LDO5 is a fixed 5V supply powering everything on chip.

LDOP

LDOP a programmable LDO whose output is selectable via register to be 1.8V(default), 2.5V or 3.3V. This rail provides power to the logic I/O interface of HL6111RFNWP5, including DCDCEN, VOUT_SEL, RESET. LDOP is enabled only when Vrect_UV1=0.

Both LDOs feature soft-start and output over-current protection.

LDO5D "PON" Generation

LDO5D is a "qualified" version of LDO5 that is connected to the down-stream charger as the Power-on (PON) signal. LDO5D is enabled only when the following conditions are all met: 1.Vrect_UV2 is set low, i.e. Vrect higher than Vrect_UV2 threshold, and 2.a WPC source is identified.

After steps 1 and 2, LDO5D is turned on by the load switch between LDO5 and LDO5D. To avoid in-rush current, a soft-start mechanism on LDO5D is included. LDO5D does not have a separate OCP protection: it is protected by the LDO5's OCP function.

Full-Wave Synchronous Rectifier

The full-wave synchronous rectifier (SR) block operates in one of the two modes: passive and full synchronous mode.

Passive Mode

None of the 4 power MOSFETs are turned on. Only their body diodes are used to form the full-wave rectification. This mode is used when Vrect_UV1 is high, or when the load on Vrect becomes light enough.

Full Synchronous Mode

This is the main operation mode of the SR. Diode emulation circuitry is used around all 4 power MOSFETs to make them behave like ideal diodes. In WPC mode, full sync mode is turned on when Irect current becomes greater than a light-load threshold, or turned off when Irect current becomes less than that.

Load Modulation, Over-Voltage Clamp and Detuning Switch Driver

Load Modulation

One pair of load modulation switches, LM1P/N are provided for WPC operation. They are designed to sustain up to 1A RMS current.

Over-Voltage Clamp

Two Vrect over-voltage clamps, CLMP1/2, are provided to sustain up to 1.2A RMS current, they are turned on when Vrect_OV is flagged, and turned off when Vrect_OV is cleared.

6-Channel ADC

A 6-channel time-multiplexing Analog-to-Digital Converter (ADC) is used to monitor the following parameters: Vrect voltage, Irect current, Vout voltage, Vout load current, die temperature and an external MPP channel. The MPP channel can be used for optional Rx coil temperature detection and over-temperature alarm (OTA). The ADC core is a 10b ADC running at 220kHz clock rate. A 6:1 MUX does the time-multiplexing function and converts 6 channels in succession in 600us.

The MPP channel offers 10b resolution with 5V full-scale. Its full scale is achieved only if LDO5 is at 5V or above. Other 5 channels have 8b resolution.

Optional VPSNS Voltage Generation

VPSNS mode selection

VPSNS voltage is an analog feed-forward output voltage to the down-stream charger. Its function is defined by VPSNS_MODE register. When not used, VPSNS is pulled to a fixed high voltage. When in use, VPSNS can indicate either output power or output current, based on factory configuration.

VPSNS voltage generation for downstream charger's Iin control loop

In this configuration, VPSNS voltage is a representation of the instant power delivered at Vout pin to the down-stream charger. This signal is used by the down-stream charge's input current-limit loop and regulated to Vref point when the loop is in control. VPSNS voltage is defined as:

VPSNS=[SF/POUT_MAX]*[VOUT*IOUT]*VPSNS_VREF, up to VPSNS_MAX, where

SF is a scaling factor defined by PR_AD<1:0> register bits:

SF=1 if PR_AD<1:0>=2b'00 or 2b'11, or WPC charging

SF=1.51 if PR_AD<1:0>=2b'01

SF=3.03 if PR_AD<1:0>=2b'10

POUT_MAX is max power defined by Tx (WPC mode), it is 5W.

VOUT is the ADC measured VOUT voltage, updated every 600us or slower.

VPSNS_VREF is the reference voltage defined by VPSNS_VREF register (default 1.2V).

VPSNS_MAX is the maximum allowed VPSNS voltage when the down-stream charger is in the input current-limit loop mode, as defined by VPSNS_MAX register (default 1.5V).

VPSNS Representing Output Current

In this configuration, VPSNS voltage represents instant output current on VOUT pin. Its output voltage is defined as:

VPSNS=0.8 * IOUT

DCDC Post Regulator

The DCDC post regulator provides a programmable 3.952-10.04V output voltage, a maximum 2.2A load current to deliver 5W maximum output power. Operating at nominal 1.375MHz PWM frequency, it uses small form-factor 1uH~2.2uH inductor to minimize total system PCB area. Light-load PFM mode is also included. The transition between PWM and PFM modes occurs automatically, or the switcher can be placed in forced PWM mode by I2C interface. The regulator can only be enabled when all below conditions are met:

1. No flags or warnings, including Vrect_UV1, Vrect_UV2, OTA etc.
2. DCDCEN pin is set to 1

When the regulator is enabled by DCDCEN signal, an internal soft-start scheme is used to so that Vout ramps up slowly, and Vrect in-rush current is limited during the entire soft start period.

Vout is I2C programmable but can be also forced to a fixed 5V if VOUT_SEL pin is pulled low.

A cycle-by-cycle current limit is implemented to protect the buck from Vout over-loading or short circuit fault. If the high-side current reaches ~3.4A, the high-side FET is

turned off right away, and a cycle-by-cycle current-limit event is generated. If a total of 512 such events are recorded, the buck shuts down, and attempts to re-start after a hick-up period of 1.6s.

When DCDCEN pin is lowered, or if Vrect_UV1, Vrect_UV2, OTA etc warnings are flagged, the buck is disabled right away. No active discharge is used, so Vout is lowered by only external loading.

Optional Bypass Mode

In bypass mode, the MOSFET's current is actively monitored by a bypass over-current comparator. If the bypass current exceeds its threshold I_{LIM_BP}, bypass mode is immediately disabled and buck mode resumed. The IC cannot enter bypass mode again until a time-out period has elapsed in which the buck operation does not hit OCP condition.

Mode Transition Between Buck and Bypass

When the DCDC regulator is turned on the first time, it always uses the buck mode to finish soft-start of Vout. After soft-start, the mode control circuit becomes active. An internal comparator constantly compares Vrect with Vout_bypass threshold and decides which mode to use. If Vrect ≤ (Vth_bypass-Vhyst_bypass) and is true for the entire duration of a programmable qualification timer, the bypass mode is enabled. The buck is placed in Hi-Z mode. At any time when Vrect > Vth_bypass, bypass mode is disabled and buck mode starts. The buck converter starts from its Hi-Z mode to take over and supplies Vout without going through a soft-start sequence.

Vout Target Selection

HL6111RFNWP55 Vout target voltage is defined by registers 0x0E and 0x30. A 2b range selector in 0x30 selects three separate ranges, and an 8b DAC in 0x0E defines actual Vout target value. The sets of range and step are defined as below:

1.Range 1: 4.940mV-10.040mV in 20mV steps;

2.Range 2: 3.952-8.032V in 16mV steps

I2C host controls which range to use and set the appropriate DAC value. For example, in BPP mode, I2C host should select range 1 by setting 0x30=00(default) and set Vout=5.0V (0x0E=0x03).

Input Impedance (Zlim) Regulation

The Zlim target can be automatically calculated based on negotiated Tx/Rx maximum power.

Maximum Output Current (Iout) Regulation

To limit maximum output power, HL6111RFNWP55 includes an output current regulation. It continuously limits Iout to be no more than the target value. The target value range is 100mA-1200mA, in steps of 50mA or 100mA, as defined in register 0x28.

Oscillator/Time Reference

An on-chip 11MHz oscillator is used to provide reference clock to the digital control state machine, WPC protocol handler, etc.

Protection

Vrect Over-Voltage Protection (OVP)

When Vrect voltage rises above the threshold defined in CLAMP_TH, actions will be different depending on IC's operation mode.

In WPC mode, two internal clamps, clamp1 and clamp2 are turned on to lower AC1/AC2 voltage. The Vrect over-voltage (OVA_I) flag will be set in LATCHED_STATUS and STATUS registers. The clamps are kept on until Vrect voltage is lowered to be less than the Vrect_OV clear voltage, at which point they are turned off, and the OVA status cleared in register STATUS. At the same time, a current source Idvrect_dac is also turned on to provide loading on Vrect pin. Idvrect_dac value is set internally and stays on until Vrect_OV flag is clear or the die-ot flag is on.

Iout Over-Current Protection (OCP)

In buck mode, over-current on Vout is detected and protected by the buck's cycle-by-cycle over-current protection as described in the DCDC Post Regulator

section. The over-current (OCA) flag will be set in LATCHED_STATUS and STATUS registers.

In bypass mode, if over-current is detected, bypass mode is turned off, and the buck mode resumes right away. The rest of the protection process is the same as that in buck mode. OCA Flags will also be set the same way.

Optional Thermal Regulation

When internally measured die temperature reaches around 120°C, HL6111RFNWP5 has an optional feature to dynamically reduce max output current regulation target so that die temperature stays around 120°C. A 5°C hysteresis window is used in this regulation loop.

Over-Temperature Flag (OTA) and Die Over Temperature Shut-Down

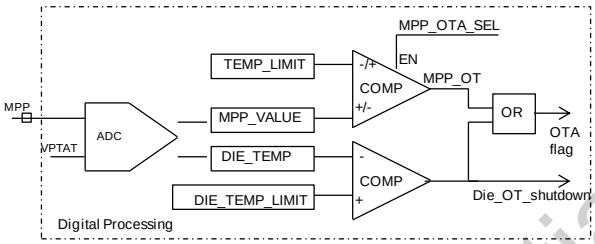


Figure 8 Over-temperature Flag and Shutdown

The IC's die temperature is monitored by an on-chip PTAT voltage, which is measured by the ADC continuously. If it is higher than the preset threshold, thermal shutdown happens. The post regulator shuts down, and the SR enters passive mode. Vrect clamps and LM switches are also shut down for protection.

The IC also generates over temperature flag OTA, which can either be an indication of die over-temperature only, or a combination of die over-temperature and the external MPP channel measured over-temperature event. See Figure 9 for details on how these two signals are combined to generate the OTA flag.

MPP/External Temperature Sense

HL6111RFNWP5 support external temperature monitoring via MPP pin through an external resistor divider with an NTC or PTC resistor.

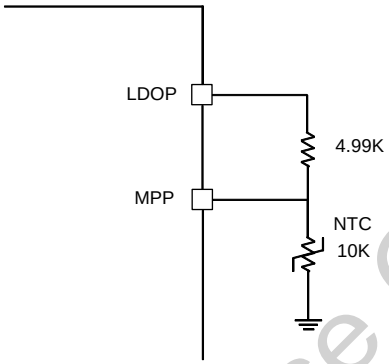


Figure 9 MPP external connection

As shown in Figure 9, MPP is connected to a voltage divider made of a 1% pull-up resistor to LDOP, and a pull-down NTC/PTC resistor placed closed to where temperature needs to be monitored. Triggering and clearing temperature target are digitally set in MPP_OTA_CONFIG register.

Under-Voltage Lockout (UVLO)

HL6111RFNWP5 has two under-voltage lock-out threshold Vrect_UV1 and Vrect_UV2.

Vrect_UV1 is used to determine when the WPC control engine can be turned on to communicate with the Tx. If Vrect_UV1=1, the part stays in standby mode. When Vrect_UV1=0, the WPC engine turns on.

Vrect_UV2 is used to determine whether the DCDC post regulator can be enabled to provide power to Vout. If Vrect has risen above Vrect_UV2, the post regulator can be enabled.

Digital I/O Description

There are several digital I/O signals that interface with the down-stream charger, PMIC and/or Blue-tooth controllers, DCDCEN, VOUT_SEL, RESET, I2C(SCL/SDA) and INTn. Except I2C and INTn, all of these signals' logic levels are set to be the built-in programmable LDOP, whose output can be 1.8V(default), 2.5V or 3.3V. I2C(SCL/SDA) interface uses a fixed 1.8V logic level. INTn is an open-drain output.

DCDCEN

DCDCEN=1 enables HL6111RFNWP5's post regulator to provide power to Vout pin.

VOUT_SEL

VOUT_SEL pin also defined Vout target of the DCDC post regulator. If VOUT_SEL=1 or floating, Vout is defined in register. If VOUT_SEL=0, Vout is forced to be fixed 5V.

RESET

A logic high on RESET pin resets the digital controller in this IC. All register bits are reset to their default values.

I2C

I2C Interface (SCL, SDA) is enabled When a WPC source is detected, SCL and SDA pins are pulled low internally by 200-ohm switch to disable this port.

INTn

INTn is an open drain output driver to send interrupt signals to external host. When any bit in LATCHED_STATUS register changes value, and is allowed by INT_ENABLE register, INTn pin will be pulled low. After the I2C host reads LATCHED_STATUS, this register will be cleared, and INTn is released to open.

Operation Mode

WPC/Qi Mode

In WPC mode, HL6111RFNWP5's internal state machine controls the operation mode of HL6111RFNWP5, negotiates power level with the Tx side, determines Vout value and maximum allowed power level at Vout. I2C pins are pulled low, so no communication exists between HL6111RFNWP5 and external host. HL6111RFNWP5 supports WPC V1.2.4 including BPP operation.

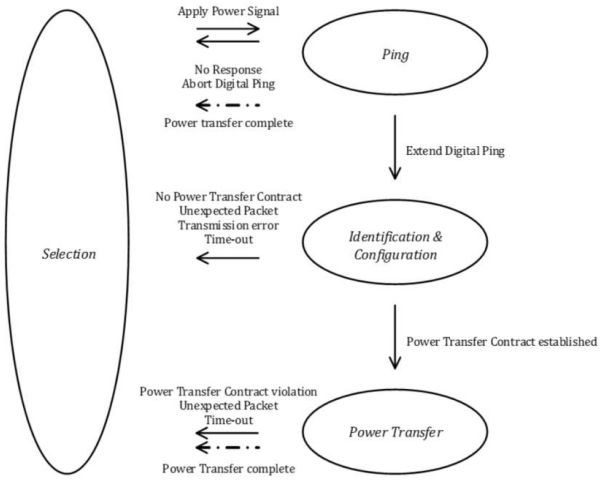


Figure 10 Simplified WPC State Diagram

Vrect Target Selection in WPC Mode

To maximize system design flexibility and optimize power efficiency, HL6111RFNWP5 allows the user to change Vrect target value on the fly via I2C communication. Register 0x27 defines the target Vrect value as the following:

Vrect_target = Vout_target + vrect_hdrm[5:0]*0.25V

Where Vout_target is the selected target output voltage, and vrect_hdrm[5:0] is defined in register 0x27[7:2]. The host can change Vrect target to an optimum value any time, based on the actual charging condition of the battery.

I2C Interface Description

I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C Bus Specification, version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with a pull-up device. When the bus is idle, both SDA and SCL lines are pulled high. All I²C compatible devices connect to the I²C SDA and SCL buses through open drain I/O pins. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific condition that indicates the START and STOP of data transfer. A slave device receives and /or transmits data on the bus under control of the master device.

HL6111RFNWP5 works as a slave and is compatible with the following data transfer modes as defined in the I²C Bus Specification: Standard mode (100kbps), Fast mode (400kbps), Fast mode plus (1000kbps) and High-speed mode (up to 3.4Mbps in write mode). The interface adds flexibility to the device by making most functions and parameters programmable through the I²C host.

The data transfer protocol for Standard mode, Fast mode and Fast mode plus is the same, therefore referred to as F/S mode in this document. The protocol for High-speed mode is different and referred to as HS mode. The HL6111RFNWP5 device has an initial 7b I²C address of 1100000 (60h).

F/S Mode Protocol

The master initiates data transfer by generating a START condition. The START condition is when a high-to-low transition occurs on the SDA line while SCL is high. The master stops data transfer by generating a STOP condition, in which a low-to-high transition occurs on the SDA line while SCL is high. This is shown in Figure 11.

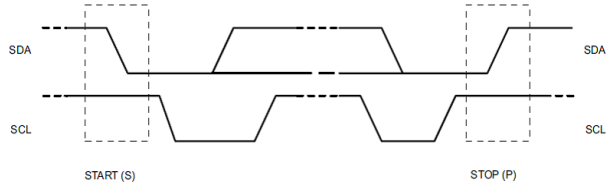


Figure 11 START and STOP Condition

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 12.)

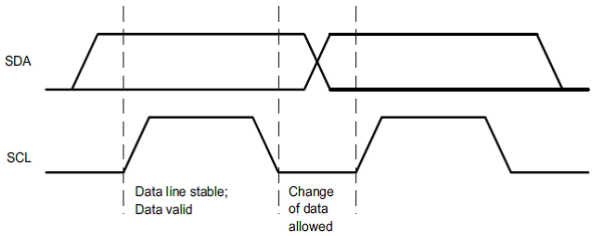


Figure 12 Bit Transfer on the Serial Interface

All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 13) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

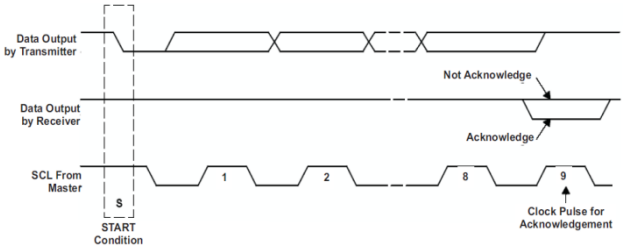


Figure 13 Acknowledge on the I2C Bus

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an

acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high. This releases the bus and stops the communication link with the addressed slave.

All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address. If a transmission is terminated in advance, the master needs to send a STOP condition to prevent the slave I²C logic from getting stuck in a bad state. Attempting to read data from register addresses not listed in this section will result in FFh being read out.

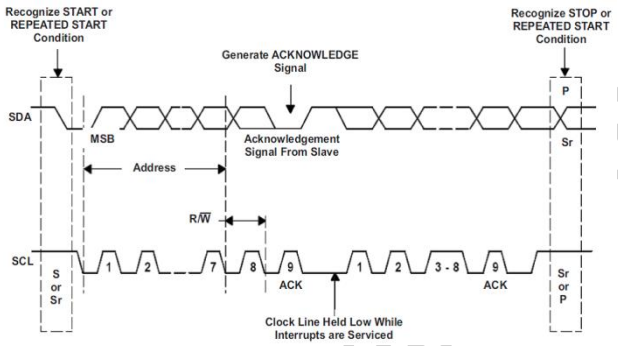


Figure 14 Bus Protocol

H/S Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode with speed less than 1Mbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4Mbps are allowed. A stop condition ends the H/S mode and switches all the internal settings of the slave devices to support F/S mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS mode. If a transmission is terminated in advance, the master needs to send a STOP condition to prevent the slave I²C logic from getting stuck in a bad state. Attempting to read data from register addressed not listed in this section results in FFh being read out.

I²C Update Sequence

The IC requires a START condition, a valid I²C address, a register address byte, and a data byte for a single update. After receiving of each byte, the IC sends acknowledge by pulling the SDA line low during the high period of a single clock. A valid I²C address will selects this IC. The IC performs an update on the falling edge of the acknowledge signal that follows the LSB bit.

For the first update, the IC requires a START condition, a valid I²C address, a register address byte and a data byte. For all consecutive updates, the IC needs a register address byte and a data byte. Once a STOP condition is received, the IC releases the I2C bus and waits for a new START condition.

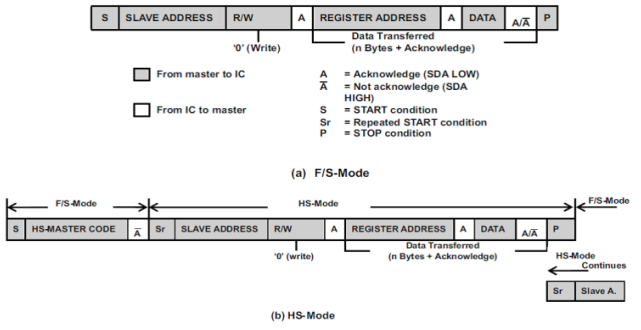


Figure 15 Data Transfer Format in F/S and H/S mode

Slave Address Byte

MSB LSB

0	0	1	1	0	0	0	R/W

The slave address byte is the first byte received following the START condition from the master device. HL6111RFNWP5's default slave address is **0011000**.

Register Description

Name	Register Address	Type	Comments
LATCHED_STATUS	0x00	R	
VRECT	0x01	R	
IRECT	0x02	R	
TEMP	0x03	R	
CLAMP_TH	0x04	R/W	
Reserved	0x05	--	
Reserved	0x06	--	
STATUS	0x07	R/W	
Reserved	0x08-0x09	--	
ID	0x0A	R/W	
TEMP_LIMIT	0x0B	R/W	
POWER_LIMIT	0x0C	R/W	
Z_LIMIT	0x0D	R/W	
VOUT_TARGET	0x0E	R/W	
Reserved	0x0F	R/W	
VPSNS_SEL and VPSNS_REF	0x10	R/W	
VPSNS_MAX	0x11	R/W	
INTERRUPT_ENABLE	0x12	R/W	
VPSNS_MODE	0x13	R/W	
Reserved	0x14	--	
Reserved	0x15	--	
Reserved	0x16	--	
MPP_VALUE_H & MPP_VALUE_L	0x17, 0x18	R/W	
MPP_OTA_CONFIG	0x19	R/W	
I2C_Address	0x1A	--	
Reserved	0x1B-0x1F	--	
VOUT_BYPASS CONFIG	0x20	R/W	
Reserved	0x21	--	
Reserved	0x22	--	
Reserved	0x23-0x26	--	
VRECT_HEADROOM	0x27	R/W	
IOUT_LIM_SEL	0x28	R/W	
Reserved	0x29-0x2F	-	
VOUT_RANGE_SEL and GP2_CONFIG	0x30	R/W	

LDO_REF	0x31	R/W	
Reserved	0x31-0xFF	--	

Table 6 HL6111RFNWP5 Register Map

Bit Definition

The following table defines the operation of each register bit.

Bit	Name	Value	Type	Description
LATCHED_STATUS, Address: 0x00, Default Value: 0x01. **1. This byte will be cleared upon I2C read.** **2. For b[7:1], bit value 0->1 change causes an interrupt, if enabled by INT_ENABLE register.** **3. For b[0], bit value 1->0 change causes an interrupt, if enabled by INT_ENABLE register.**				
7	I_LDO5_L	0	R	5V LDO over current, latched. =1: over current
6	SPARE	0	R	Reserved
5	OCA_L	0	R	Vrect over-current flag, latched. =1: Vrect node over current
4	OTA_L	0	R	Over-temperature flag, latched. =1: Over-temperature flagged, can be die over temperature flag, or (die over temperature or MPP channel over temperature)
3:2	SPARE	00	R	Reserved
1	OVA_L	0	R	Vrect over-voltage flag, latched. =1: Vrect over clamp threshold
0	OUT_EN_L	1	R	Follow DCDCEN pin. =0: Buck not enabled; =1: buck enabled
VRECT, Address: 0x01, Default Value: 0x00				
7:0	VRECT[7:0]	0x00	R	ADC measured Vrect voltage, top 8 MSBs. VRECT=this byte value*(24/256) 0x00=0V, 0x01=93.75mV, 0x02=187.5mV, 0xFF=23906mV
IRECT, Address: 0x02, Default Value: 0x00				
7:0	IRECT[7:0]	0x00	R	ADC measured Irect current, top 8 MSBs. In bypass mode, this byte indicates Iout current. **IRECT=this byte value*13mA** 0x00=0mA, 0x01=13mA, 0x02=26mA... 0x4D=1001mA... 0xFF=3315mA
Die Temperature, Address: 0x03, Default Value: 0x00				
7:0	TEMP[7:0]	0x00	R	ADC measured die temperature, top 8 MSBs. Temperature=(220.09-this byte value)/0.6316 0x00=disabled, 0x01=346.9C... 0x80=145.8C... 0xAA=79.3C,... 0xFF=-55.3C
CLAMP_VTH_VRECT, Address: 0x04, Default Value: 0x72				
7	SPARE	0	R/W	Reserved
6:4	CLM_VTH[2:0]	111	R/W	Vrect clamp threshold, rising edge: 000=19.4V, 001=19.9V...100=21.4V...**111=22.9V(Default)**
3	SPARE	0	R/W	Reserved
2:0	SPARE	010	R/W	Reserved
STATUS, Address: 0x07, Default Value: 0x01				
7	I_LDO5_I	0	R	5V LDO over current. =1: over current
6	MODE	0	R	Buck Mode: =0: in bypass mode; =1: in buck mode
5	OCA_I	0	R	Vrect over-current flag. =1: Vrect node over current

4	OTA_I	0	R	Die over-temperature flag. =1: die over-temperature
3:2	SPARE	00	R	Reserved
1	OVA_S	0	R	Vrect over-voltage flag. =1: Vrect > over-voltage clamp threshold
0	OUT_EN_S	1	R	Follows DCDCEN pin. =1 if DCDCEN pin =1, =0 if DCDCEN pin=0
ID, Address: 0x0A				
7:6	SPARE	00	R/W	Reserved
5:0	ID[5:0]	010000	R/W	HL6111RFNWP55
		000001		HL6111RFNWP5C
TEMP_LIMIT, Address: 0x0B, Default Value: 0xAA				
7:0	MPP_TLIM[7:0]	0xAA	R/W	MPP over temperature threshold. Its format is the ADC measured MPP channel data value.
POWER_LIMIT, Address: 0x0C, Default Value: 0x14				
7:0	POUT_MAX[7:0]	0x14	R/W	Maximum output power allowed 0x00=0W,0x01=0.25W,0x02=0.5W...0x04=1.0W...**0x14=5.0W(default)**...0x28=10W...0x3C=15W...0xFF=63.75W
Z_LIMIT, Address: 0x0D, Default Value: 0x03				
7:3	SPARE	00000	R/W	Reserved
2:0	Reserved	011	R/W	Reserved
VOUT_TARGET, Address: 0x0E, Default Value: 0x03				
7:0	VOUT_TRGT[7:0]	00000011	R/W	Vout target value, based on 0x30 range definition 0x30[7:6]=00: Vout=4.940mV-10.040mV in 20mV steps; 0x30[7:6]=11: Vout=3.952mV-8.032mV in 30mV steps: Default=0x03 : 5.00V (0x30[7:6]=00)
VPSNS_REF, Address: 0x10, Default Value: 0x07				
7	SPARE	0	R/W	Reserved
6	VPSNS_EN	0	R/W	=0: VPSNS disabled, VPSNS pin outputs fixed V_MODE value as defined in 0x13. =1: VPSNS enabled, VPSNS pin voltage proportional to Vout output power or current.
5	SPARE	0	R/W	Reserved
4:0	VPSNS_VREF[4:0]	0x0B	R/W	PSNS output voltage reference value 0x00=0.1V,0x01=0.2V....**0x0B=1.2V(default)**...0x1F=3.2V
VPSNS_MAX, Address: 0x11, Default Value: 0x1F				
7:5	SPARE	0x000	R/W	Reserved
4:0	VPSNS_VMAX[4:0]	0x1F	R/W	PSNS output voltage reference value 0x00=0.1V,0x01=0.2V....0x0E=1.5V...**0x1F=3.2V(default)**
INTERRUPT_ENABLE, Address: 0x12, Default Value: 0x00				

7	I_LDO_L_EN	0	R/W	Enable LDO5 over-current interrupt. =0: disable; =1: enable
6	SPARE	0	R/W	Reserved
5	OCA_L_EN	0	R/W	Enable Vrect over-current interrupt. =0: disable; =1: enable
4	OTA_L_EN	0	R/W	Enable die over-temperature interrupt. =0: disable; =1: enable
3:2	SPARE	00	R/W	Reserved
1	OVA_L_EN	0	R/W	Enable Vrect over-voltage interrupt. =0: disable; =1: enable
0	OUT_EN	0	R/W	Enable OUT_EN indicator interrupt. =0: disable; =1: enable
VPSNS_MODE, Address: 0x13, Default Value: 0x00				
7:5	SPARE	0x000	R/W	Reserved
4:0	VPSNS_MODE[4:0]	0x0B	R/W	PSNS output voltage reference value **0x00=1.7V(default)**, 0x01=1.8V...0x1F=4.8V
MPP_VALUE_H, Address: 0x17, Default Value: 0x00				
7:0	MPP_VALUE[9:2]	0x00	R	MPP channel ADC read-out, top 8MSBs MPP[9:2]: 0x00=0, 0x01=19.548mV,0x02=39.096mV...0xFF=4984.74mV
MPP_VALUE_L, Address: 0x18, Default Value: 0x00				
7:6	MPP_VALUE[1:0]	00		MPP channel ADC read-out, bottom 2LSBs MPP[1:0]: 00=0, 01=4.887mV,02=9.774mV,03=14.661mV
5:0	SPARE	000000	R	
MPP_OTA_CONFIG, Address: 0x19, Default Value: 0x00				
7:2	SPARE	000000	R	Reserved
1	MPP_OTA_TC	0	R/W	Configures temperature coefficient (TC) of MPP channel =0: negative TC. OTA will flag if MPP_VALUE < TEMP_LIMIT register value(default) =1: positive TC. OTA will flag if MPP_VALUE > TEMP_LIMIT register value
0	MPP_OTA_SEL	0	R/W	Enables MPP link to OTA flag =0: MPP channel not linked to OTA flag (default) =1: MPP channel linked to OTA flag, "or"ed with die temperature flag
I2C_ADDRESS, Address: 0x1A, Default Value: 0x30				
7:1	I2C Address	0011000	R	
0	R_Wn	0	R	Read/Write
VOUT_BYPASS_CONFIG, Address: 0x20, Default Value: 0x00				
7:4	VOUT_BP[3:0]	**0000**	R/W	Vout 100% duty cycle target: **0000=5V(Default),** 0001=5.5V, 0010=6V, 0011=6.5V, 0100=7V, 0101=7.5V, 0110=8V, 0111=8.5V, 1000=9V, 1001=9.5V, 1010=10V, 1011=10.5V, 1100=11V, 1101=11.5V, 1110=12V, 1111=12V
3	SPARE	0	R/W	Reserved
2	Reserved	0	R/W	Reserved
1:0	PR_AD[1:0]	00	R/W	Reserved

VRECT_HEADROOM, Address: 0x27, Default Value: 0x10				
7:2	VRECT_HDRM[5:0]	000100	R/W	Vrect headroom voltage above Vout target value as defined in 0x0E Vrect_target=Vout_target + (VRECT_HDRM[5:0]) x 0.25V. Default=100(1.0V)
1:0	SPARE	00	R/W	Reserved
IOUT_LIM_SEL, Address: 0x28				
7:3	IOUTLIM[4:0]			Maximum output current regulation target. 00000=100mA, 00001=150mA, …10001=950mA, 10010=1000mA (HL6111RFNWP55), 10011=1100mA, 10110=1200mA (HL6111RFNWP5C), 10111=1300mA, ... 11110=2200mA, 11111=No limit.
2:0	SPARE	000	R/W	Reserved
VOUT_RANGE_SEL and GP2_CONFIG , Address: 0x30, Default Value: 0x00				
7:6	VOUT_RNG_SEL[1:0]	00	R/W	Vout range selection. See 0x0E register for definition.
5:4	SPARE	00	R/W	Reserved
3:2	Reserved	00	R/W	Reserved
1:0	SPARE	00	R/W	Reserved
LDOP_REF, Address: 0x31, Default Value: 0x00				
7:2	SPARE	000000	R/W	Reserved
1:0	LDOP_REF	00	R/W	LDOP output voltage. 00=1.8V(default), 01=2.5V, 10=3.3V, 11=reserved

Table 7 I²C Register Definition

Application Information

DCDC Regulator Input and Output Capacitors

HL6111RFNWP5 is designed for low-ESR ceramic capacitors both at the input and output rails. Actual capacitance and voltage rating of these capacitors should be selected based on “Recommended External Components” Table. Also consider the voltage coefficients of the capacitor, which reduce the effective capacitance significantly from its rated value.

Output capacitor determines Vout ripple and load transient performance. A large output capacitor generally helps reducing Vout ripple and load transient. Several capacitors in parallel can also be used. The IC can accommodate up to 15uF of total output capacitance (Cout1 and Cout2) without affecting loop stability.

Output Inductor Current Rating

The ripple current of the inductor is determined by

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \bullet \left(\frac{V_{IN} - V_{OUT}}{L \bullet f_{SW}} \right) \quad (1)$$

Where *L* is the inductance value and f_{SW} is the PWM switching frequency, respectively. Therefore, the maximum peak current of the inductor is given by

$$I_{MAXPK} = I_{MAXLOAD} + \frac{\Delta I}{2} \quad (2)$$

Where $I_{MAXLOAD}$ is the maximum DC load. Because the IC's over-current protection (OCP) circuit limits only the peak inductor current, larger than 1.2A of DC load current can be supported under worst-case conditions without triggering the OCP. Therefore, the selected inductor should be capable of sustaining a current up to I_{LMPK} (3.2A typical) or failing in a safe manner. If a lower current rating inductor needs to be used, it should still have a *rms* current rating higher than

$$I_{RMS} = \sqrt{I_{MAXLOAD}^{2} + \frac{\Delta I^{2}}{12}} \quad (3)$$

Where $I_{MAXLOAD}$=1.2A. In this case, HL6111RFNWP5 may still protect the inductor in the event of a short circuit, but may not be able to protect the inductor from failing if the DC load is able to draw higher currents than the *rms* rating of the inductor.

DCDC Regulator Output Inductance Selection

In additional to current rating, the output inductor must also have a proper inductance value for the intended application. The inductor value affects the average current limit, the output voltage ripple, and the efficiency. The HL6111RFNWP5 is optimized for operation with L=1 uH, but is stable with inductances up to 2.2uH (typical). The inductor should be rated to maintain at least 80% of its value at I_{LIMPK}. Failure to do so reduces the amount of DC current the IC can deliver safely.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR, but the *rms* current increases which produces slightly bigger V_{OUT} ripple, additional loss in the inductor and the on-resistance of the IC's power switches. Increasing the inductor value produces lower *rms* currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

Thermal Consideration

For long-term reliable operation of HL6111RFNWP5, its junction temperature(T_J) should be maintained below 125℃. Good PCB layout helps power dissipation from a small package with reduced temperature rise. Recommended guidelines include:

1. Use large area copper especially in top layer to help thermal conduction and radiation.
2. Additional vias are preferred around IC to connect the inner ground layers with reduced thermal resistance.
3. A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.

4. Use two layers of PCB or more for high current paths (PVIN, PGND, SW) to split current in two different paths and limit PCB copper self- heating.

PCB Layout Reference

The HL6111RFNWP5 device pins can be classified as following:

Digital I/O Traces

1. Pins include INT, RST, SCL, SDA, DCDCEN, VOUT_SEL.
2. Make sure these traces are isolated from the noisy traces

Analog Sensing Traces

1. Pins include MPP
2. Make sure these traces are isolated from the noisy traces using ground planes on the side and below.

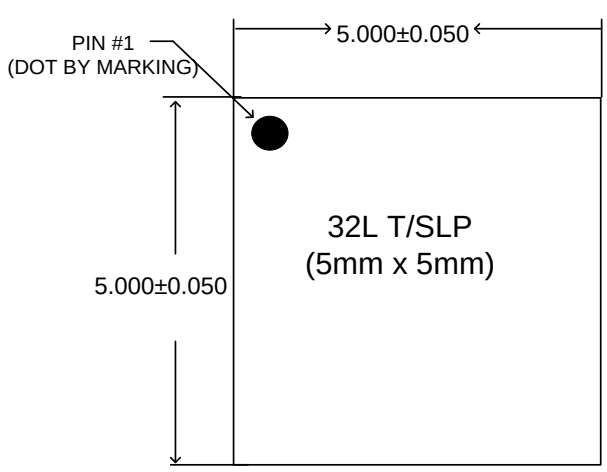
Noisy Traces

1. Pins include AC1, AC2, BOOT, BST1, BST2, LM1P/1N, LMA2P/2N, CLAMP1/2 and SW.
2. Make sure these traces are isolated from other traces using ground plane.

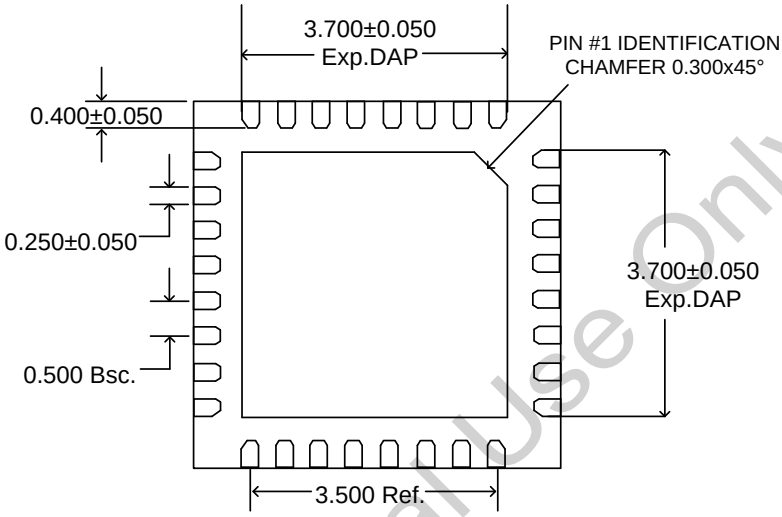
Power Traces

1. Pins include AC1, AC2, BOOT, BST1, BST2, LM1P/1N, LMA2P/2N, CLAMP1/2, SW, AGND and PGND.
2. Make sure these traces are wide enough to carry their respective maximum DC or rms current, and to minimize IR loss. Avoid using vias on these traces, i.e. lay out these traces on the top PCB plate.
3. Minimize loop area for AC power signals. This includes AC1/AC2 to PGND, and SW to Vin/Vrect and PGND. The PGND return paths for these signals should be as short as possible. Bypass capacitors on Vin and Vrect should have terminals connected to the IC's pins as short as possible.

Package Information



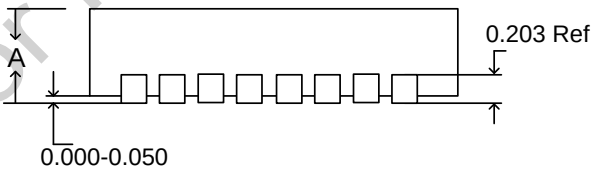
TOP VIEW



BOTTOM VIEW

NOTE:
(1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM	0.750	0.850
	MIN	0.700	0.800



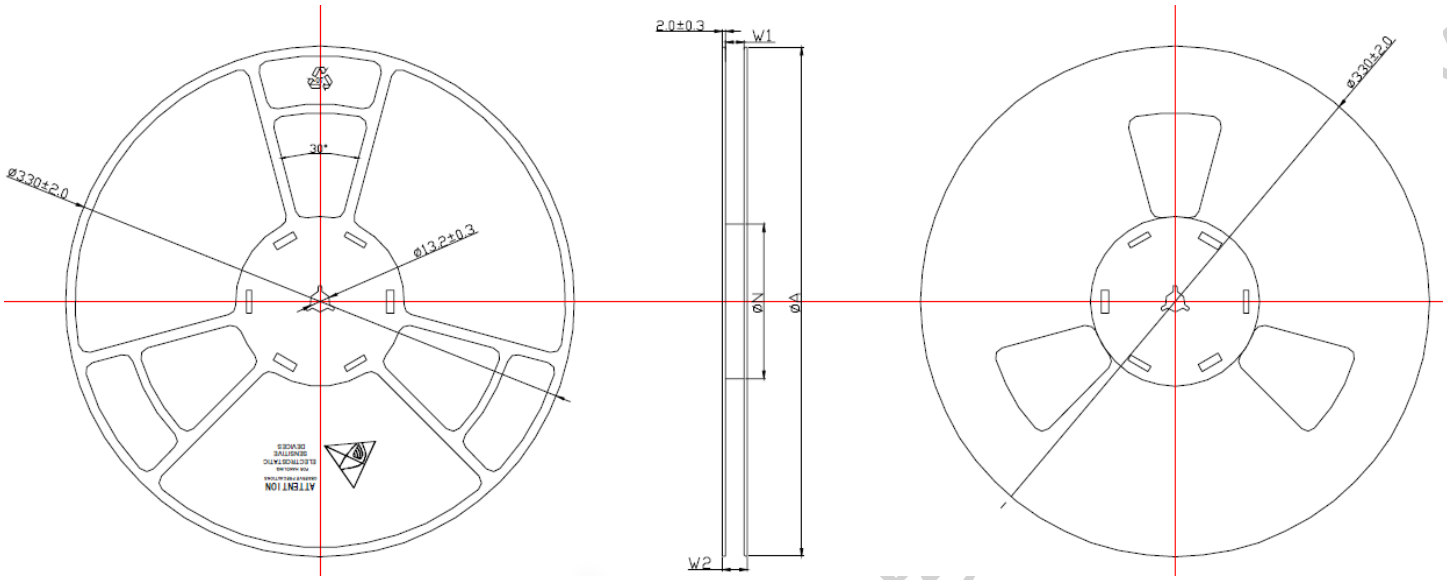
SIDE VIEW

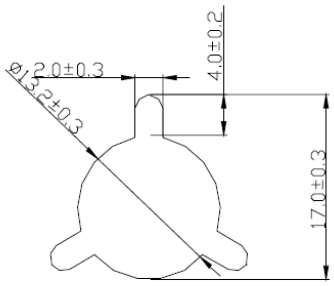
Notes

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

Tape and Reel Information

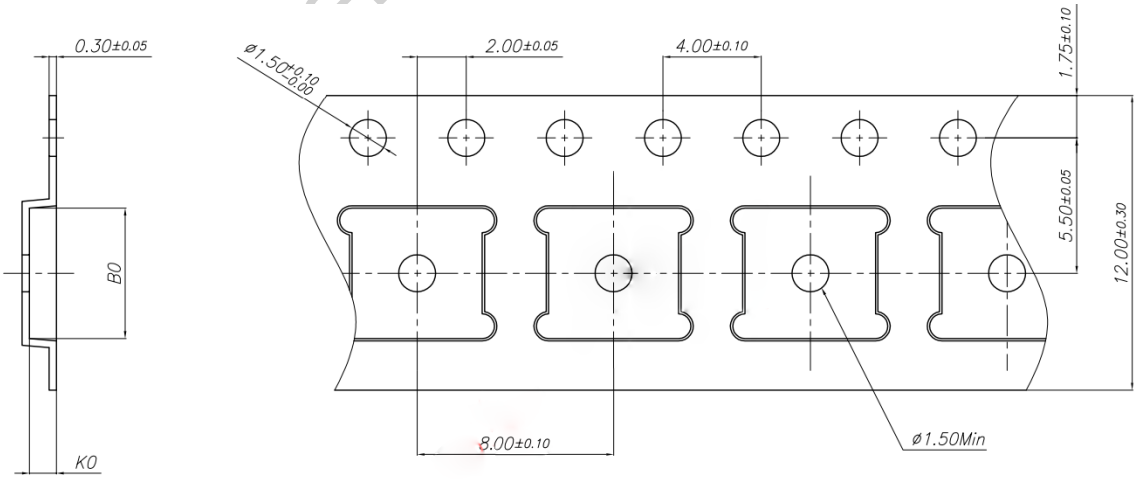
Reel Information

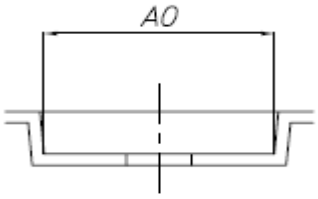




PRODUCT SPECIFICATIONS				
TYPE WIDTH	ØA	ØN	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4

Carrier Tape Information





Ao	5.30±0.10
Bo	5.30±0.10
Ko	1.10±0.10

Device	Package	SPQ	Reel Diameter (mm)	Tape Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)
HL6111RFNWP5	QFN-32	1000	330±2	12±0.3	5.30 ±0.1	5.30 ±0.1	1.10 ±0.1

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