

Upgrade Specification for FT6336GU

Upgrade Specific	eation for FT6336GU	
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Owner	ZhangXiaoyi	
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Approval		

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Revision History

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2014-12-10	0.1	Initial draft	Js Liao
2015-07-03	1.0	Chip named FT6336GU	ZhangXiaoyi
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Table of Contents

1	Intro	oduction		4
2	Con	nmunicat	tion	4
3	Basi	ic Flow		5
4	App	lication (data verification	5
	4.1	Fla	sh structure	6
		4.1.1	FW verification area	6
		4.1.2	FW configuration area	6
	4.2		p.bin file structure	
	4.3	Ap	plication verification flow	9
5	Con	nmunicat	ion protocol	9
	5.1	Co	mmunication steps	10
		5.1.1	Read ID	10
		5.1.2	Erase	10
		5.1	L.2.1 Erase application area	10
		5.1	1.2.2 Enable/Disable flash operation status INT	10
			L.2.3 Read Erase finished status	11
		5.1.3	Application F/W Data write	11
		5.1.3.1	Send data package	11
		5.1.3.2	Read Write Flash status	11
		5.1.4	Verification	12
		5.1.5	Read	
		5.1.6	Reset	
		5.1.7	Read Configuration	13
		5.1.8	Read bootloader version	
6	Imp	lementa	tion	14
	6.1	Ва	sic Flow	14
	6.2	Ва	sic Sequence	15
		6.2.1	Power on Sequence	15
		6.2.2	Reset Sequence	15
		6.2.3	I2C Sequence	16



1 Introduction

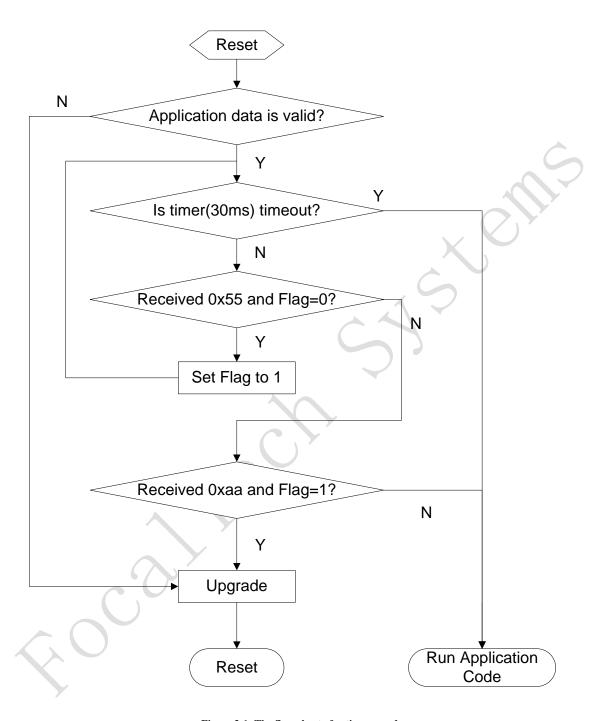
This document descripts the upgrade flow of FT6416/FT6426 IC series. The whole program of FT6416/FT6426 is divided into two parts, one is bootloader part and the other is application part. And both parts will be burned into flash when we run the download operation. When FT6416/FT6426 boot up, the bootloader part will run at first, then there will be a timer with 30ms time out started. The upgrade flow will be triggered if the bootloader received specific upgrade command within this timer, otherwise it will switch to application flow part.

2 Communication

The upgrade flow communication based on the standard IIC protocol. And the default IIC slave address is 0x70. The IIC slave address in bootloader and in application should be the same one. To ensure this, bootloader and application will both get the IIC slave address from a specific flash address (0x07B0).



3 Basic Flow



 $\label{eq:Figure 3-1:The flow chart of active upgrade } \textbf{Figure 3-1:The flow chart of active upgrade}$

4 Application data verification

Application data verification will be run before upgrade flow.



4.1 Flash structure

Below table shows the flash structure of FT6416/FT6426.(48k)

Delow table s	nows the	mash sh	acture or	110410/110420.(46K)						
	0	1	2		1022	1023				
$0\mathbf{K} = 0\mathbf{x}0$		Bootloader								
1k = 0x400		Bootloader FW configuration area(0x7b0~0x7ff)								
2k = 0x800		ipt vector a		FW verification area(0x900~0x91f)	Appli	cation				
				Application						
46k=0xb800		Application								
47k=0xbc00		P	arameter c	meter configuration(0xbc00~0xbff7) For tp tool						
					(0xbff	8~0xbfff: 8bytes)				

Table 4-1: The structure of flash

4.1.1 FW verification area

0x900	0x901	0x902	0x903	0x904	0x905	0x906	0x907
Code leng	th	Negation	of code	App Part1	Negation of	App Part2	Negation
		length		ECC	App part1	ECC	of App
					ECC		part2 ECC
0x908	0x909	0x90a	0x90b	0x90c	0x90d	0x90e	0x90f
Panel	Negation of	FW	Negation	Upgarde	Upgarde flag2	Upgarde	Negation
Vendor	Panel	Version	of FW	flag1		times	of Upgarde
ID	Vendor ID	\ \ \	Version				times
0x910	0x911	0x912	0x913	0x914			0x91f
the param	eter region	Negation o	of the	Reserved			Reserved
length		parameter region					
		length					

Address is at Flash struct.

Code length is App F/W length.

App Part1 ECC is ECC of App F/W first 256 bytes.

App Part2 ECC is ECC of App F/W of starting at address 0x120. (Address at Flash structure is 0x920)

4.1.2 FW configuration area

0x7b0	0x7b1	0x7b2	0x7b3	0x7b4	0x7b5		0x7cf
IIC	Negation of	iovoltage	Negation of	Panel Vendor ID	Negation of Panel	Reserved	Reserved



Slave_address	Slave_address	lovoltage		Vendor ID			
0x7d0							
	Project Code(ASCII)						
0x7f0	f0						
Customer code(ASCII)							

Project code and Customer code end with ASCII character '/0'.

4.1.3 Parameter configuration area

0xbc00-0xbc01	0xbc02-0xbc03	0xbc04-0xbc05	0xbc06-0xbc07	0xbc08-0xbc09	0xbc0a		0xbc0f
Parameter length	Negation of	Parameter data	Negation of	Start address of	xml	Rese	Reserve
	Parameter length	ECC	Parameter data	Parameter data	version	rved	d
			ECC				
0xbc10							0xbc1f
		Param	neter data or 0xff				
				1			
0xbff0	Oxbfff						
	Parameter data or 0xff (0xbff8~0xbfff: 8bytes)						

4.2 App.bin file structure

"app.bin" and "app.i" is the same thing with different file format. The "app.bin" is Binary data and "app.i" is Hex data.





Example for app.bin and app.i

Below table shows the structure of "app.bin" file.

	0	1	2				1022	1023
0k = 0x0	Interrupt vector address (0x000~0xff)			FW verification area(0x100~0x11f) Applicat			ation	
1k=0x400					Application			
		Application						
					Application or 0xff			
45k=0xb400			Application	on or 0	xff	FW configu	aration area	ı
	(address: ~ 0xb7f7)					(address: 0xb	7f8~0xb84	.7)
46k =0xb800	F	FW configuration area						
~0xb847	(address	address: 0xb7f8~0xb847, 80bytes)						

The data from 0x100 to 0x11f at app.bin is totally the same with the data from 0x900 to 0x91f at flash.

0x100	0x101	0x102	0x103	0x104	0x105	0x106	0x107
Code leng	th	Negation	of code	App Part1	Negation of	App Part2	Negation
		length		ECC	App part1	ECC	of App
					ECC		part2 ECC
0x108	0x109	0x10a	0x10b	0x10c	0x10d	0x10e	0x10f
Panel	Negation of	FW	Negation	Upgarde	Upgarde flag2	Upgarde	Negation
Vendor	Panel	Version	of FW	flag1		times	of Upgarde
ID	Vendor ID		Version				times
0x110	0x111	0x112	0x113	0x114			0x11f
the parameter region Negation of the		Reserved			Reserved		
length		parameter region					
		length					

The data from "APP_CODE_LEN+0x00" to "APP_CODE_LEN+0x4f" at app.bin is totally the same with the data from 0x7b0 to 0x7ff at flash.

 $APP_CODE_LEN = ((data@0x100) << 8) + (data@0x101).$

APP_CODE_	APP_CODE_	APP_CODE	APP_CODE_	APP_CODE	APP_CODE_		APP_CODE	
LEN+0x00	LEN+0x01	_LEN+0x02	LEN+0x03	_LEN+0x04	LEN+0x05		_LEN+0x1f	
IIC	Negation of	iovoltage	Negation of	Panel Vendor	Negation of	Reserved	Reserved	
Slave_address	Slave_address		lovoltage	ID	Panel Vendor ID			
APP_CODE_								
LEN+0x20							_LEN+0x3f	
			Project Code(ASCII)				
APP_CODE_								
LEN+0x40								
Customer code(ASCII)								



4.3 Application verification flow

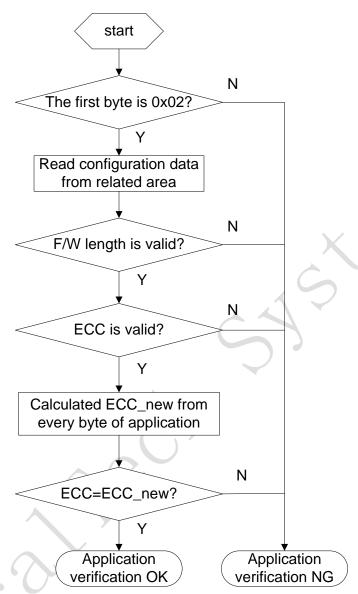


Figure 4-2: The flow chart of application verification

5 Communication protocol

Definition	:	
Slv_addr	IIC slave address	
R	Stand for value 1,	IIC read
W	Stand for value 0,	IIC write



5.1 Communication steps

5.1.1 Read ID

Read ID is a must be step before upgrade, upgrade can't start if the ID is not correct, the ID of FT6416/FT6426 is "0x79, 0x18"

Step 1: Send the command bytes

Start	Slv_addr +	0x90	0x00	0x00	0x00	Stop
	W					

Step 2: Read ID

Start Slv_addr + R	0x79	0x1c	Stop
--------------------	------	------	------

5.1.2 Erase

5.1.2.1 Erase application area

Start	Slv_addr + W	0x61	Stop
-------	--------------	------	------

It takes ****ms [****ms (erase time for 60 blocks) + ****ms (safe delay after last erase finished)] to erase application area (46K Bytes). addr:0x0800->0xbfff.

5.1.2.2 Erase parameter configuration area

Start	Slv_addr + W	0x62	Stop

It erase config only addr: 0x b400->0xb7ff.

5.1.2.3 Erase application area A

Start	Slv_addr + W	0x63	Stop
			l *

It erase app only addr:0x0800->0xbbff.

5.1.2.4 Enable/Disable flash operation status INT

art $Slv_addr + W = 0x6b$	0x00 0x00	0x00 EnINT	Stop
---------------------------	-----------	------------	------

EnINT: 0x01->Enabled INT signal for flash operation status query;

0x00->Disabled INT signal for flash operation status query;



5.1.2.5 Read Erase finished status

Step1:

If flash operation status INT had been enabled, wait for the INT signal or timeout.

Step2:

Start	Slv_addr + W	0x6a	0x00	0x00	0x00	Stop
						r

Step3:

Start	Slv_addr + R	Flash_Operation_Status	Flash_Operation_Status	Stop
		_High_Bytes	_Low_Bytes	

Flash_Operation_Status: 0xB002 means flash erase is finished. Other value means not yet finished and need to wait then query again.

5.1.3 Application F/W Data write

5.1.3.1 Send data package

Start	Slv_addr	0xBF	Add_H	Add_M	Add_L	Len_H	Len_L	Data1	 Data	Stop	
	+ W					,					

Parameter	r Description	
Add_H	The high byte of start address	1 Byte
Add_M	The middle byte of start address	1Byte
Add_L	The low byte of start address	1Byte
Len_H	The high byte of sending data length	1Byte
Len_L	The low byte of sending data length	1Byte

Table 5-1 Abbreviation

The length of sending data can NOT exceed 255 Bytes.

Host could divided whole application data into many data packages based on the total size of application.

5.1.3.2 Read Write Flash status

Step1:

If flash operation status INT had been enabled, wait for the INT signal or timeout.

Step2:

|--|

Step3:



Start	Slv_addr + R	Flash_Operation_Status	Flash_Operation_Status	Stop
		_High_Bytes	_Low_Bytes	

Flash_Operation_Status: (0xB002 + i) means flash write for the No. i package(128 bytes) is finished. $(1 \le i \le 0xFFD)$

5.1.4 Verification

Step 1:

Start	Slv_addr + W	0xcc	Stop	
				9

Step 2:

Start Slv_addr + R	Ecc	Stop
--------------------	-----	------

Ecc is the block check character of all the valid F/W bytes.

Host will also calculate ECC data by itself when sending data. It should compare the ECC data read from FT6416/FT6426 and the one which calculated by itself. If they are the same, it means that upgraded succeed, otherwise upgrade is failed and need to retry from chapter 5.1.2.

5.1.5 Read

Host could read data from FT6416/FT6426

Step 1:

Start	Slv_addr +	0x03	ADD_H	ADD_M	ADD_L	Stop
	W	\sim \sim				

Step 2:

Start Slv_addr + R Data1 Data2 DataN Stop

Parameter	Description	Default
Add_H	The high byte of start address	1 Byte
Add_M	The middle byte of start address	1Byte
Add_L	The low byte of start address	1 Byte
Data	Application data	

Table 5-2 Abbreviation

5.1.6 Reset

Send this command could make FT6416/FT6426 trigger software reset.

Start	Slv_addr + W	0x07	Stop
	· · · · · · · · · · · · · · · · · · ·		1



5.1.7 Read Configuration

Step 1:

- 1							
	Start	$Slv_addr + W$	0x4A	0x00	0x00	Offset	Stop

Step 2:

Start	Slv addr + R	Data1	Data2	Data3	 DataN	Stop
					 	1 ·- · · 1

Offset: Configuration Data Address offset (Max 0x4f).

Data: Configuration Data($(N + offset) \leq 0x50$).

5.1.8 Read bootloader version

Step 1:

Start	Slv addr + W	0xcd	Stop
Start	DIV_addi W	OACU	Stop

Step 2:

Stort Sly addr D Rootlander Version Stop					
Start Siv_addi + K Doodloader_Version Stop	Start	1 SIV auul + K	Bootloader Version	Stop	



6 Implementation

6.1 Basic Flow

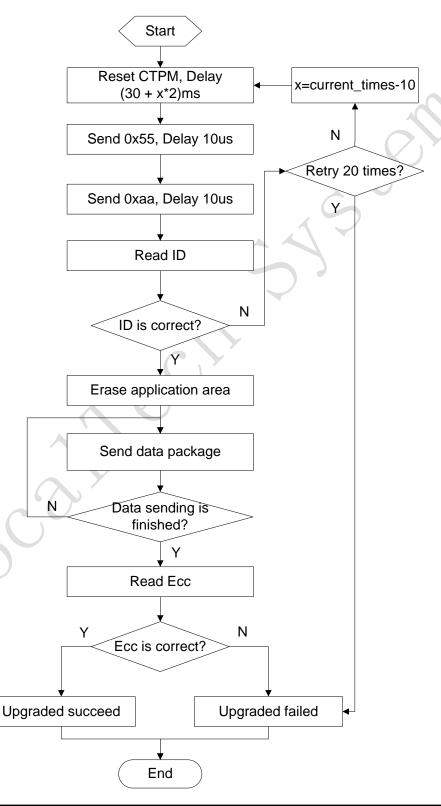




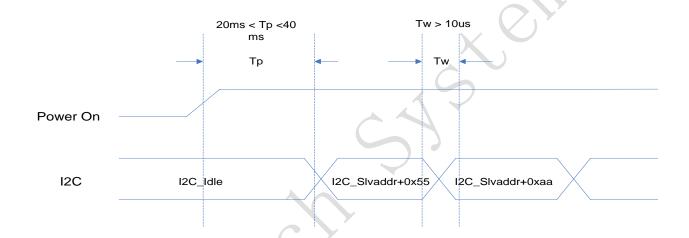
Figure 6-1: The flow chart of upgrade

- 注: 1、In "Erase application area" step, if Host have not received INT after 20s, Host Automate for the next step.
 - 2. In "Send data package" step, if Host have not received INT after 80ms, Host Automate for the next step.

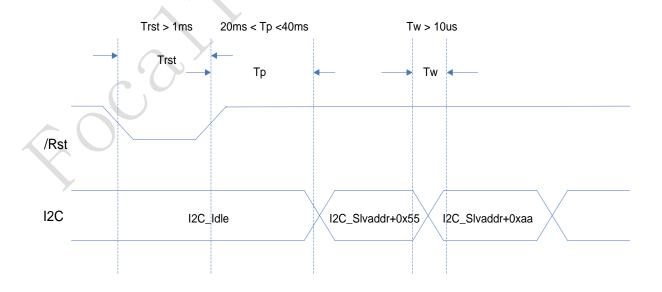
6.2 Basic Sequence

There are two methods to trigger upgrade, one is power on and the other is reset.

6.2.1 Power on Sequence



6.2.2 Reset Sequence





6.2.3 I2C Sequence

