CPU

ChipHD to Pine64		
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LPDDR3 32X1

ChipHD to Pine64

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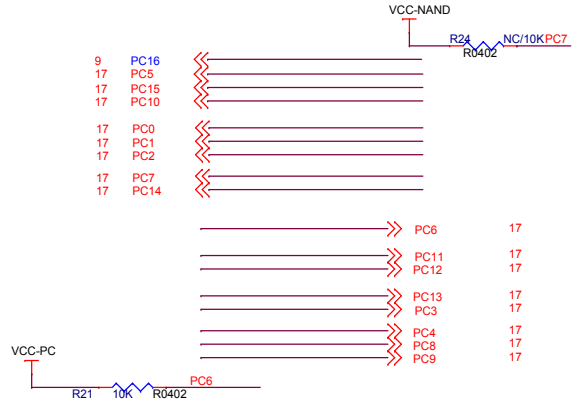

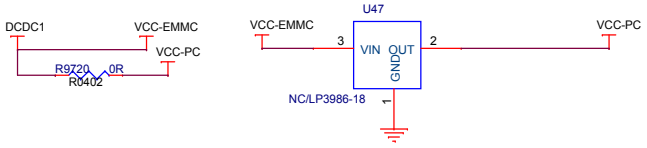

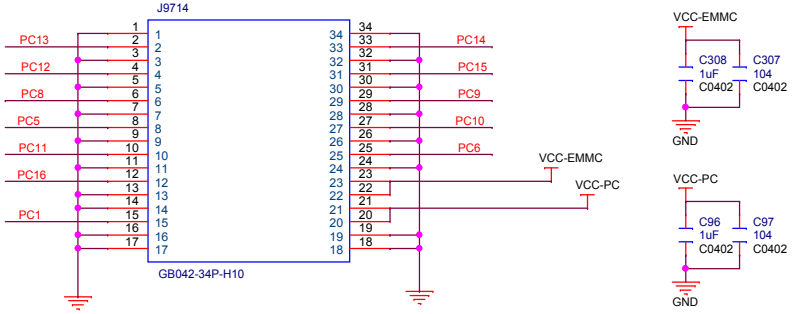

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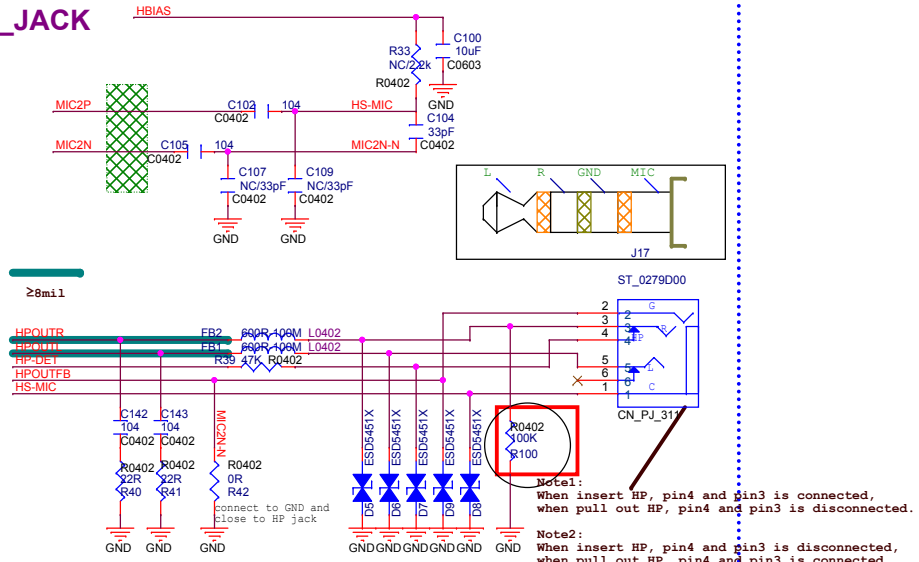
AUDIO

HP_JACK



5 HBIAS

5 HP-DET
5 HPOUTFB
5 HPOUTL
5 HPOUTR

5 MIC2N
5 MIC2P

5 HS-MIC

5 EAROUTP
5 EAROUTN

AVCC

VCC-5V

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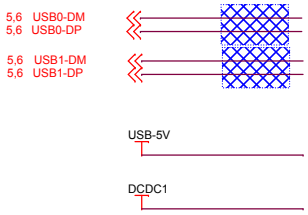

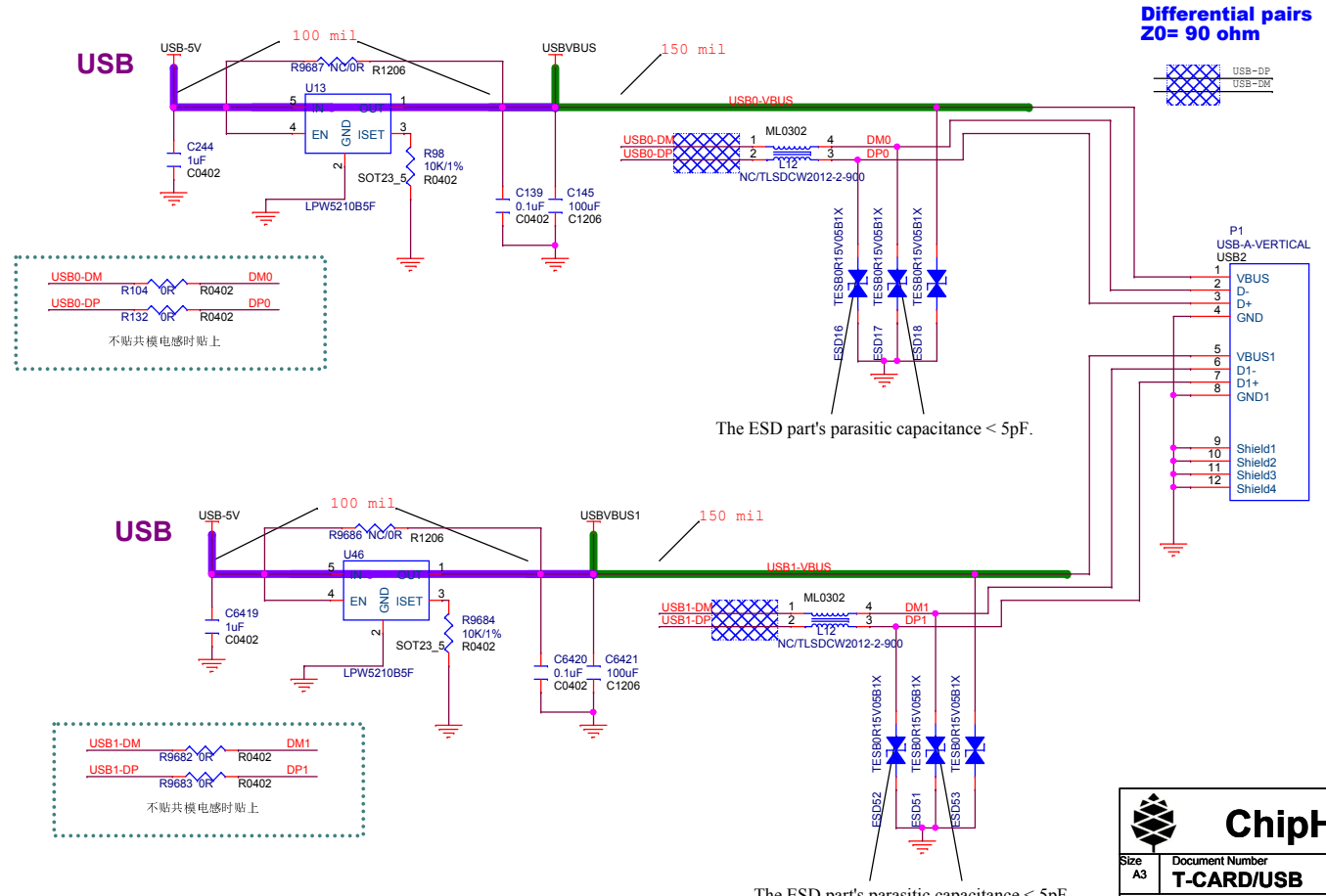

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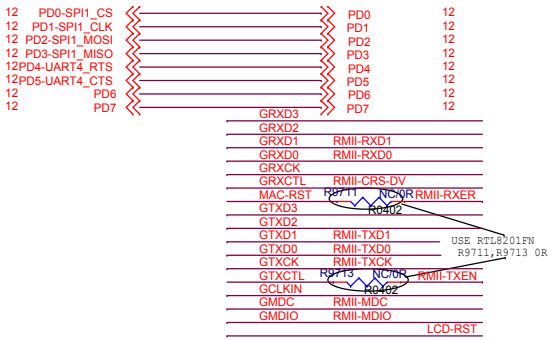
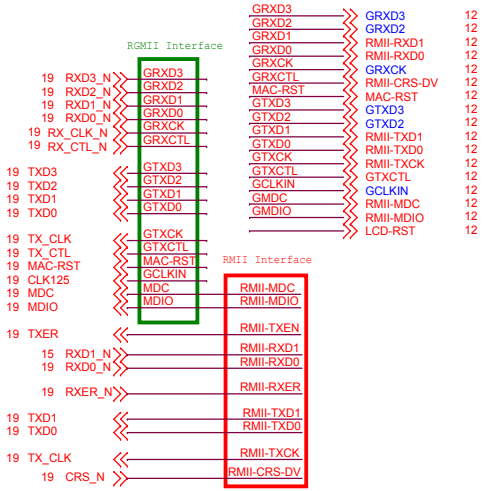
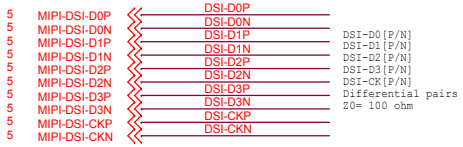
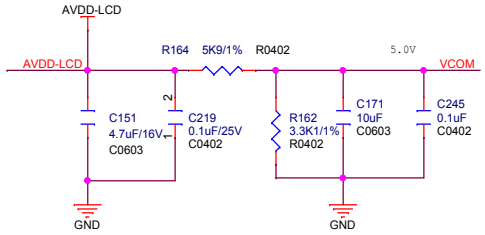
LCD

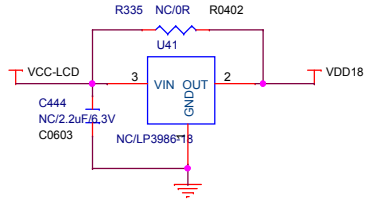


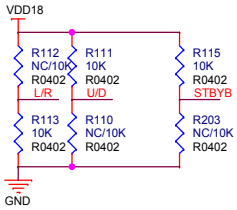


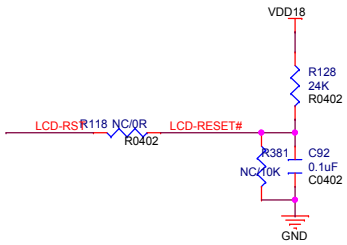


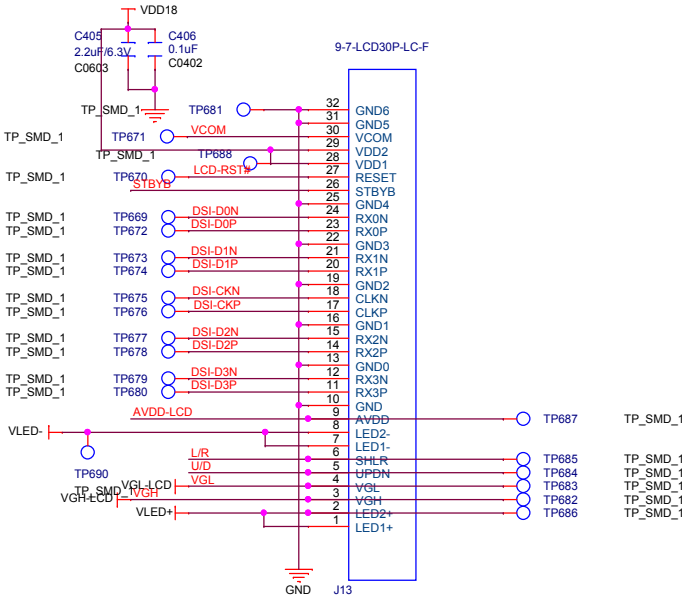
MIPI-LCD

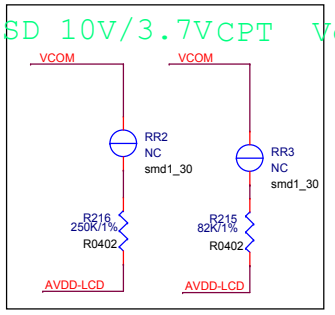












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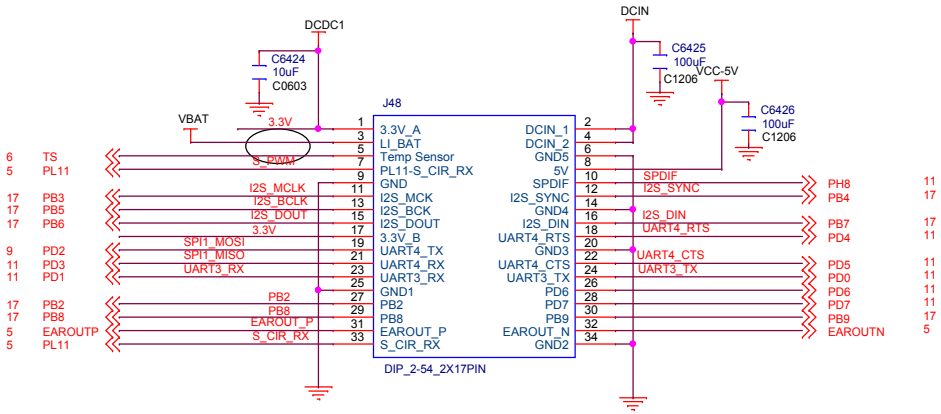
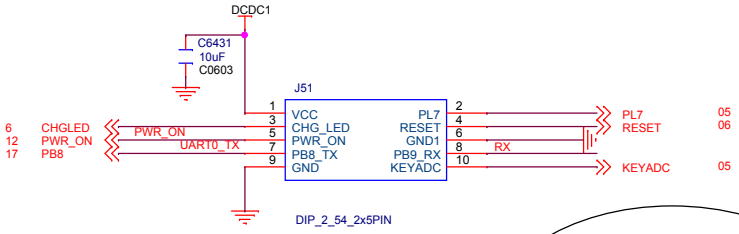
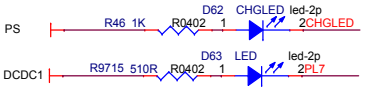
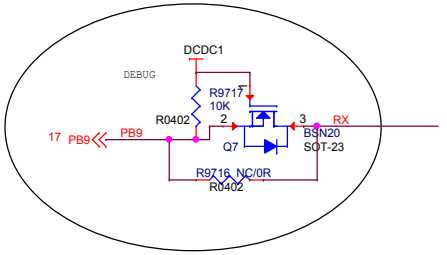
Euler bus









ChipHD to Pine64

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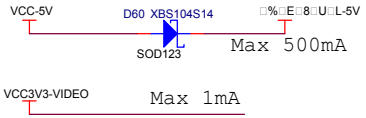
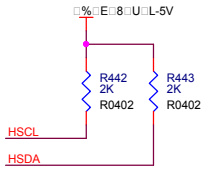
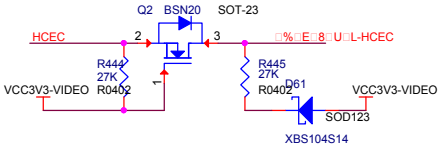
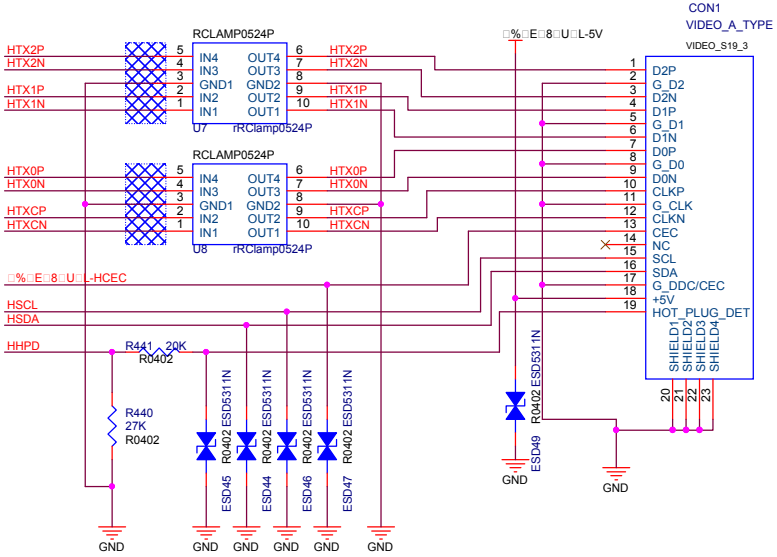


Differential pairs
Z0= 100 ohm







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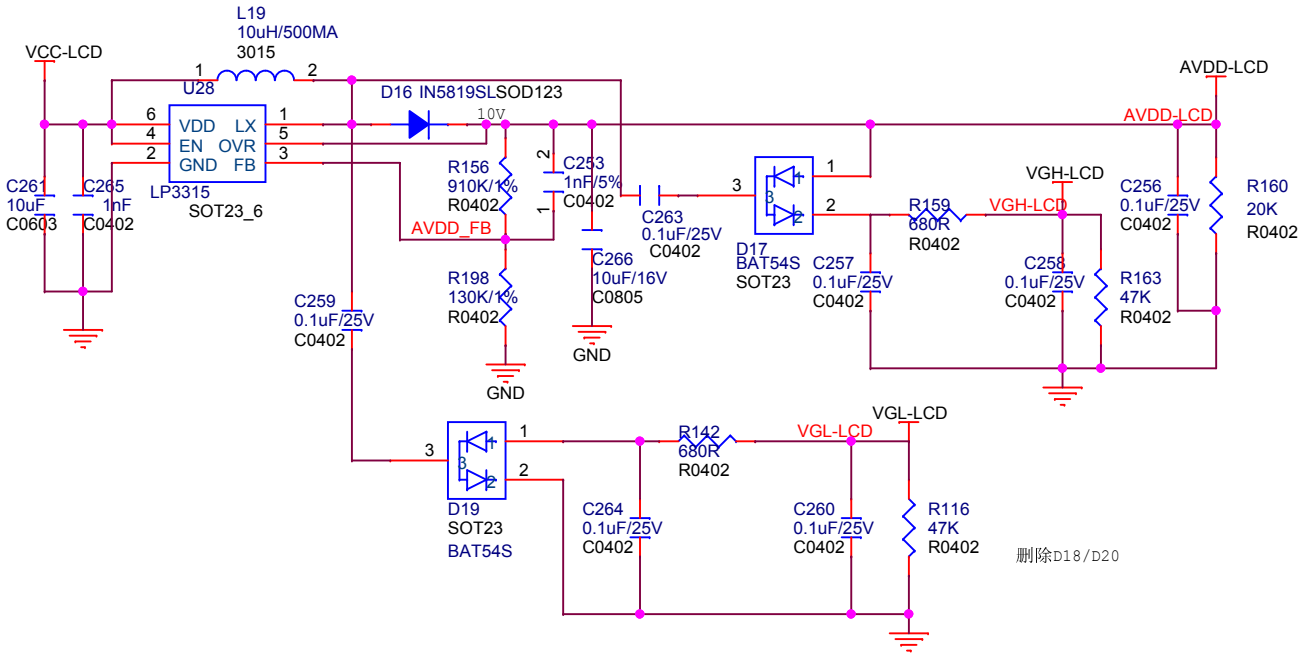
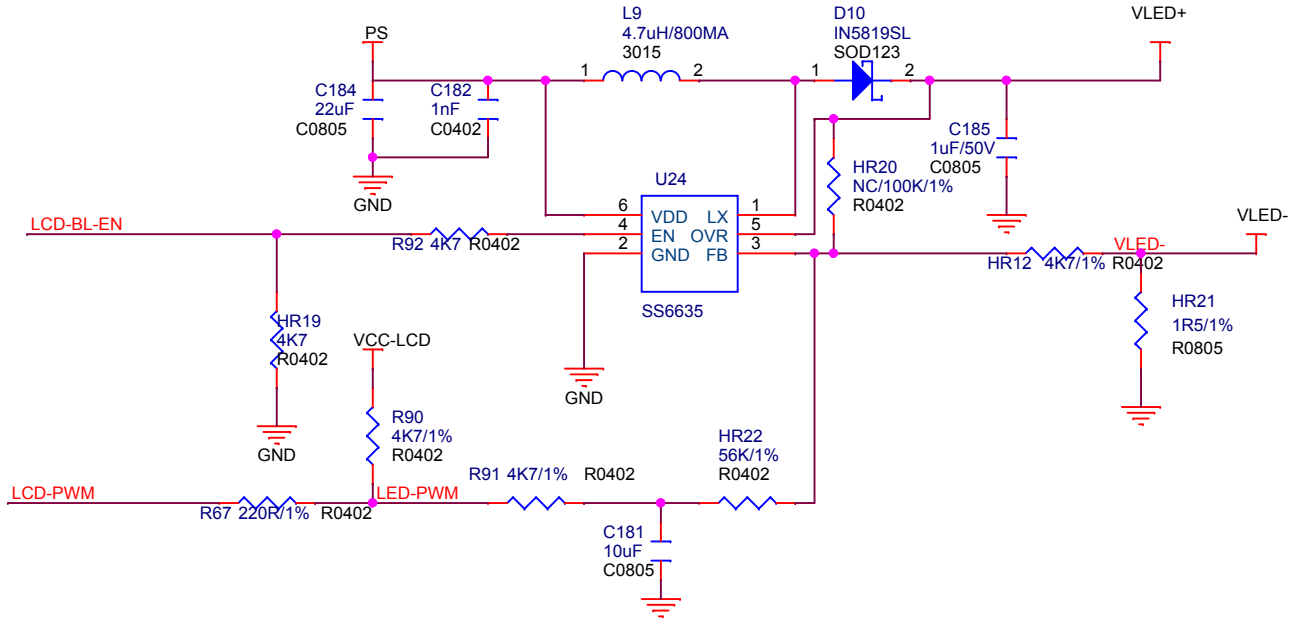
LCD POWER

6 LCD-PWM
6 LCD-BL-EN



Backlight



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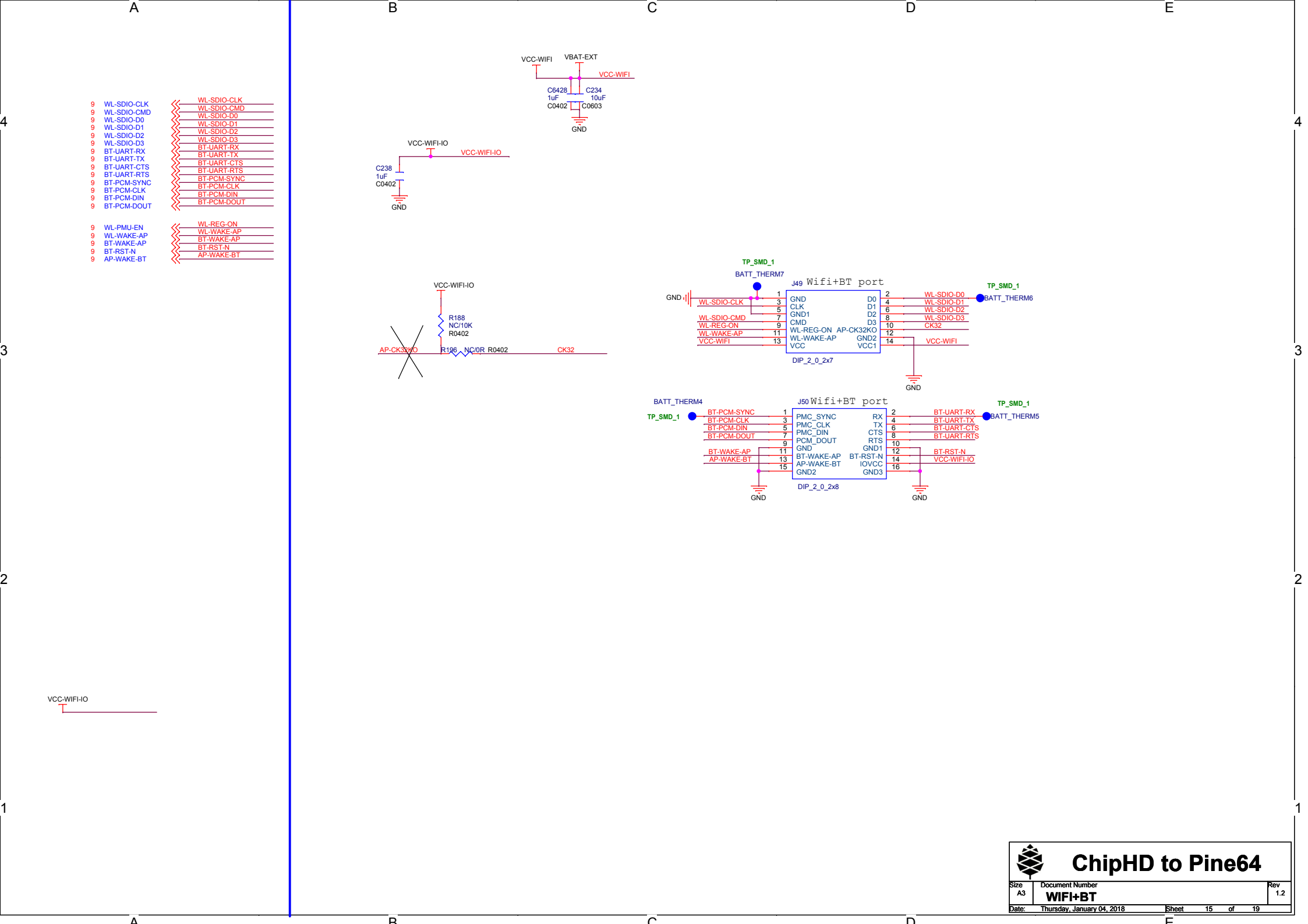
A
B
C
D
E
9 WL-SDIO-CLK
9 WL-SDIO-CMD
9 WL-SDIO-D0
9 WL-SDIO-D1
9 WL-SDIO-D2
9 WL-SDIO-D3
9 BT-UART-RX
9 BT-UART-TX
9 BT-UART-CTS
9 BT-UART-RTS
9 BT-PCM-SYNC
9 BT-PCM-CLK
9 BT-PCM-DIN
9 BT-PCM-DOUT
WL-SDIO-CLK
WL-SDIO-CMD
WL-SDIO-D0
WL-SDIO-D1
WL-SDIO-D2
WL-SDIO-D3
BT-UART-RX
BT-UART-TX
BT-UART-CTS
BT-UART-RTS
BT-PCM-SYNC
BT-PCM-CLK
BT-PCM-DIN
BT-PCM-DOUT
9 WL-PMU-EN
9 WL-WAKE-AP
9 BT-WAKE-AP
9 BT-RST-N
9 AP-WAKE-BT
WL-REG-ON
WL-WAKE-AP
BT-WAKE-AP
BT-RST-N
AP-WAKE-BT
VCC-WIFI-IO
VCC-WIFI
VBAT-EXT
C6428
1uF
C0402
C234
10uF
C0603
GND
VCC-WIFI-IO
C238
1uF
C0402
GND
VCC-WIFI-IO
R188
NC/10K
R0402
AP-CK32KO
R196 NC/0R R0402
CK32
TP_SMD_1
BATT_THERM7
J49 Wifi+BT port
GND
WL-SDIO-CLK
WL-SDIO-CMD
WL-REG-ON
WL-WAKE-AP
VCC-WIFI
GND
CLK
GND1
CMD
WL-REG-ON
WL-WAKE-AP
VCC
D0
D1
D2
D3
AP-CK32KO
GND2
VCC1
WL-SDIO-D0
WL-SDIO-D1
WL-SDIO-D2
WL-SDIO-D3
CK32
VCC-WIFI
TP_SMD_1
BATT_THERM6
DIP_2_0_2x7
GND
BATT_THERM4
TP_SMD_1
J50 Wifi+BT port
BT-PCM-SYNC
BT-PCM-CLK
BT-PCM-DIN
BT-PCM-DOUT
BT-WAKE-AP
AP-WAKE-BT
PMC_SYNC
PMC_CLK
PMC_DIN
PCM_DOUT
GND
BT-WAKE-AP
AP-WAKE-BT
GND2
RX
TX
CTS
RTS
GND1
BT-RST-N
IOVCC
GND3
BT-UART-RX
BT-UART-TX
BT-UART-CTS
BT-UART-RTS
BT-RST-N
VCC-WIFI-IO
TP_SMD_1
BATT_THERM5
DIP_2_0_2x8
GND
GND
VCC-WIFI-IO
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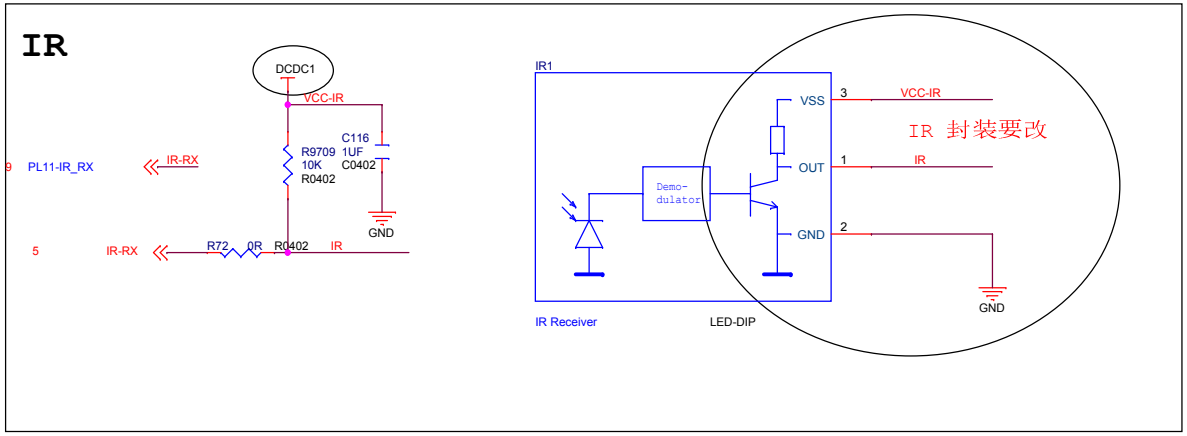
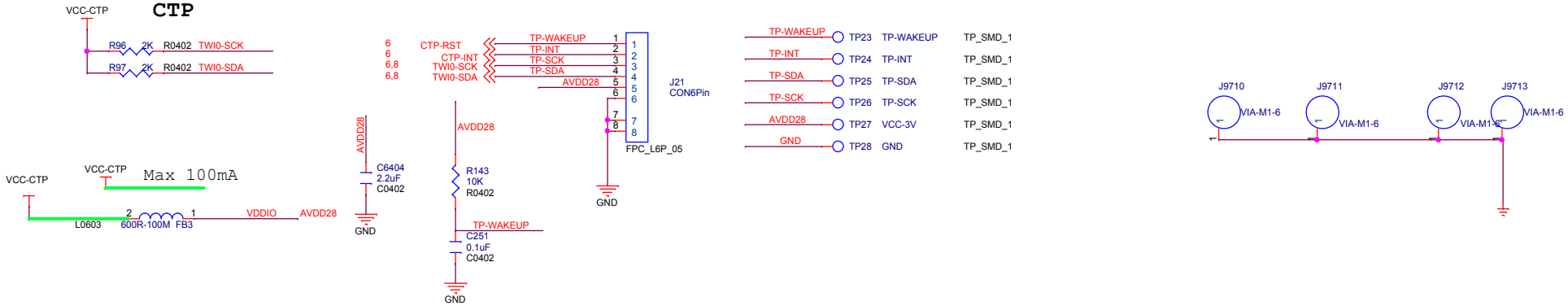
CTP

IR



CTP



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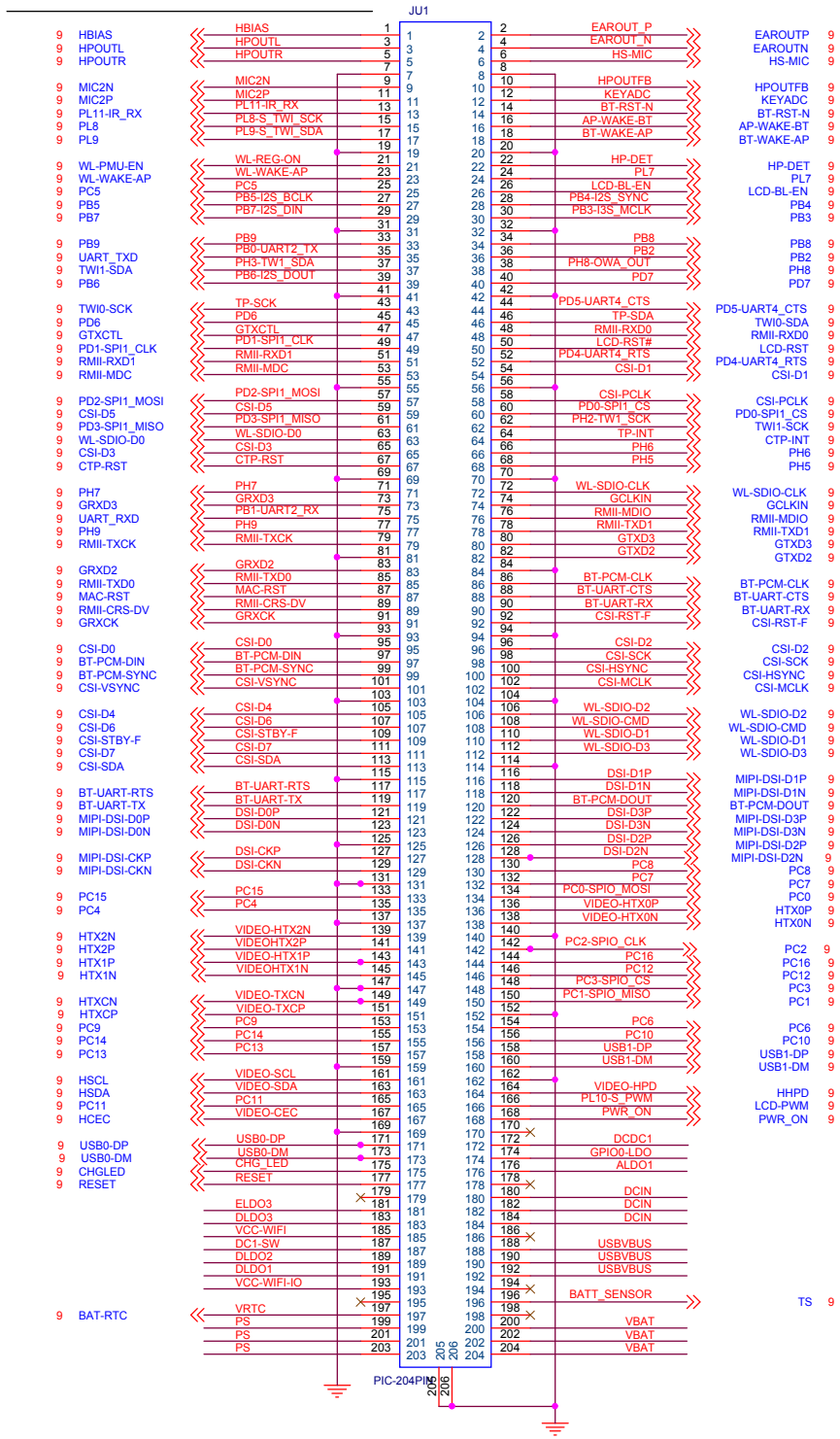
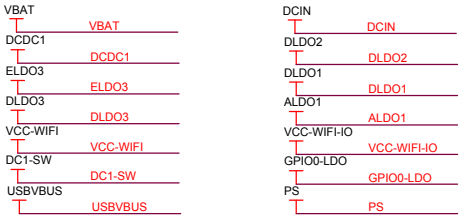
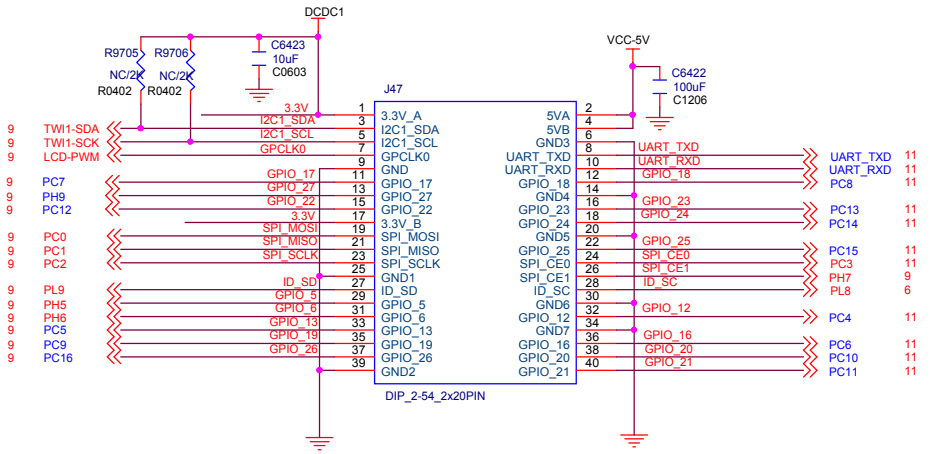
PI-2 bus







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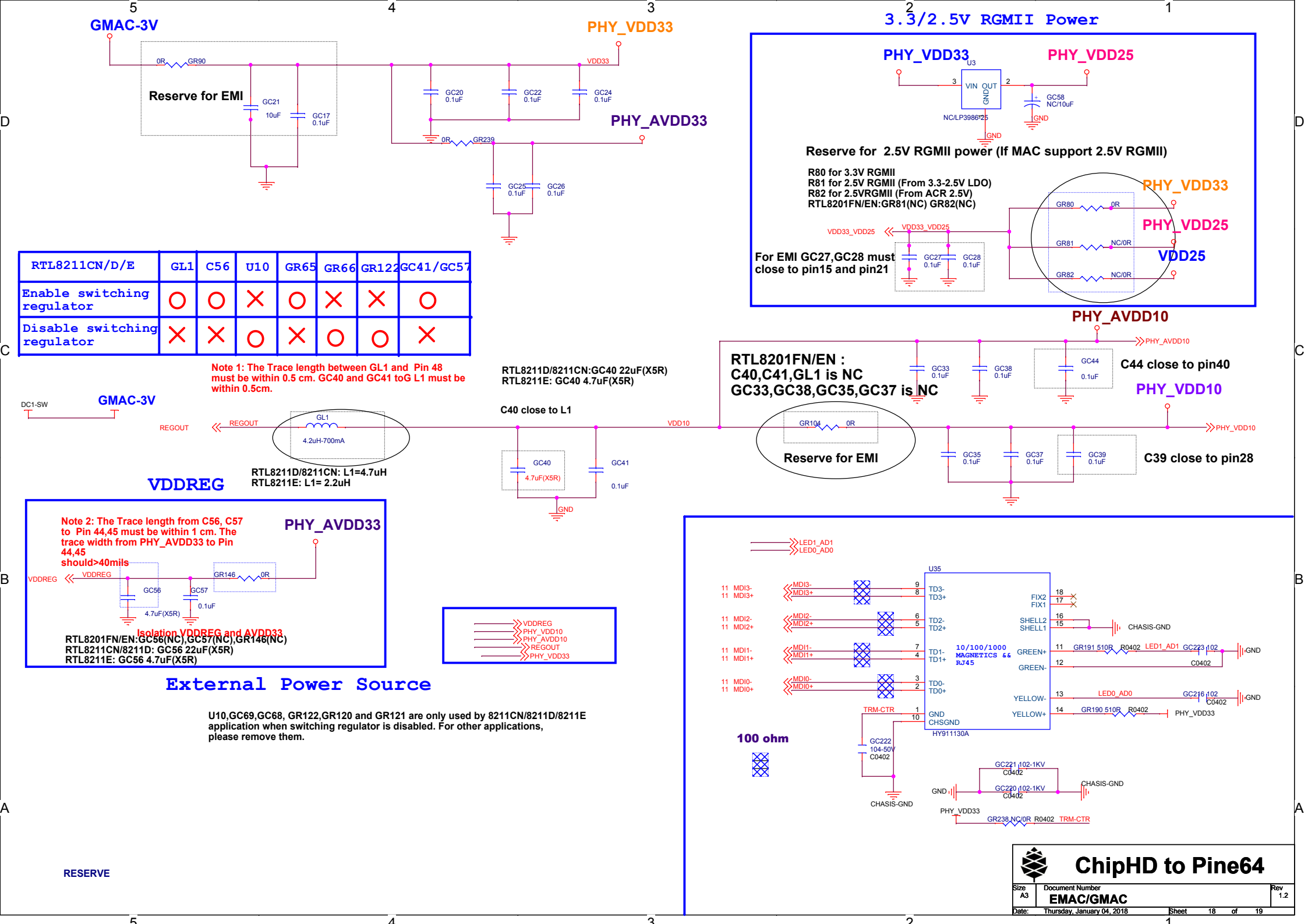
GMAC-3V
PHY_VDD33
0R GR90
Reserve for EMI
GC21 10uF
GC17 0.1uF
VDD33
GC20 0.1uF
GC22 0.1uF
GC24 0.1uF
PHY_AVDD33
0R GR239
GC25 0.1uF
GC26 0.1uF
3.3/2.5V RGMII Power
PHY_VDD33
PHY_VDD25
U3
VIN OUT GND
NC/LP3986-25
GC58 NC/10uF
GND
Reserve for 2.5V RGMII power (If MAC support 2.5V RGMII)
R80 for 3.3V RGMII
R81 for 2.5V RGMII (From 3.3-2.5V LDO)
R82 for 2.5VRGMII (From ACR 2.5V)
RTL8201FN/EN:GR81(NC) GR82(NC)
VDD33_VDD25
For EMI GC27,GC28 must close to pin15 and pin21
GC27 0.1uF
GC28 0.1uF
GR80 0R
GR81 NC/0R
GR82 NC/0R
PHY_VDD33
PHY_VDD25
VDD25
PHY_AVDD10
PHY_AVDD10
C44 close to pin40
GC33 0.1uF
GC38 0.1uF
GC44 0.1uF
RTL8201FN/EN :
C40,C41,GL1 is NC
GC33,GC38,GC35,GC37 is NC
PHY_VDD10
PHY_VDD10
C39 close to pin28
GC35 0.1uF
GC37 0.1uF
GC39 0.1uF
GR104 0R
Reserve for EMI
RTL8211CN/D/E | GL1 | C56 | U10 | GR65 | GR66 | GR122 | GC41/GC57
Enable switching regulator | O | O | X | O | X | X | O
Disable switching regulator | X | X | O | X | O | O | X
Note 1: The Trace length between GL1 and Pin 48 must be within 0.5 cm. GC40 and GC41 toG L1 must be within 0.5cm.
RTL8211D/8211CN:GC40 22uF(X5R)
RTL8211E: GC40 4.7uF(X5R)
C40 close to L1
DC1-SW
GMAC-3V
REGOUT
REGOUT
GL1
4.2uH-700mA
VDD10
GC40 4.7uF(X5R)
GC41 0.1uF
GND
RTL8211D/8211CN: L1=4.7uH
RTL8211E: L1= 2.2uH
VDDREG
Note 2: The Trace length from C56, C57 to Pin 44,45 must be within 1 cm. The trace width from PHY_AVDD33 to Pin 44,45 should>40mils
PHY_AVDD33
VDDREG
VDDREG
GR146 0R
GC56 4.7uF(X5R)
GC57 0.1uF
Isolation VDDREG and AVDD33
RTL8201FN/EN:GC56(NC),GC57(NC),GR146(NC)
RTL8211CN/8211D: GC56 22uF(X5R)
RTL8211E: GC56 4.7uF(X5R)
VDDREG
PHY_VDD10
PHY_AVDD10
REGOUT
PHY_VDD33
External Power Source
U10,GC69,GC68, GR122,GR120 and GR121 are only used by 8211CN/8211D/8211E application when switching regulator is disabled. For other applications, please remove them.
RESERVE
LED1_AD1
LED0_AD0
U35
11 MDI3-
11 MDI3+
MDI3-
MDI3+
TD3-
TD3+
11 MDI2-
11 MDI2+
MDI2-
MDI2+
TD2-
TD2+
11 MDI1-
11 MDI1+
MDI1-
MDI1+
TD1-
TD1+
10/100/1000 MAGNETICS && RJ45
11 MDI0-
11 MDI0+
MDI0-
MDI0+
TD0-
TD0+
TRM-CTR
GND
CHSGND
HY911130A
FIX2
FIX1
SHELL2
SHELL1
CHASIS-GND
GREEN+
GREEN-
GR191 510R R0402
LED1_AD1
GC223 102 C0402
GND
YELLOW-
YELLOW+
LED0_AD0
GC216 102 C0402
GR190 510R R0402
PHY_VDD33
100 ohm
GC222 104-50V C0402
CHASIS-GND
GC221 102-1KV C0402
GC220 102-1KV C0402
CHASIS-GND
GND
PHY_VDD33
GR238 NC/0R R0402 TRM-CTR
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RTL8211CN/8211D/8211E/8201FN/8201EN

PME

PHY_VDD33

Note: PME Function
RTL8211D/8211E/ 8201FN only
RTL8201EN/8211CN Pin33 is NC

GR109 4.7K

PME → PME

Interrupt

PHY_VDD33

GR127 for RTL8201EN INT function

CLK125/LED2_RXDLY — GR127 NC/0R — GR106 4.7K — INT → INT

MDC/MDIO

PHY_VDD33

VDD33_VDD25

GR125 0R

GR128 0R

MDIO — GR38 1.5K

MDIO → MDIO
MDC → MDC

RTL8201FN/EN/8211CN/8211D: GR128(NC)
RTL8211E:GR125(NC)

External clock and Crystal

External clock source from OSC or Chipset.

XTAL1 — X5 — XTAL2
4 GND2 XIN 1
3 XOUT GND 2
GC1 27pF
25M-10PPM CRY-TSX3225
GC2 27pF

Use external clock:
RTL8201FN/RTL8201EN/8211CN/8211D/8211E: GR105(0 ohm)

Enable/Disable SWREG

PHY_AVDD33

ENSWREG — GR65 0R — GR66 NC/0R

Connect ENSWREG to PHY_AVDD33 to enable Switching regulator or connect ENSWREG to GND to disable Switching regulator.

RTL8201FN /EN:
GR65 is Fiber Mode
GR66 is UTP Mode(default)

PHY Reset

GR57 NC0R/VDD33_VDD25 → VDD33_VDD25
GR58 0R PHY_VDD33 → PHY_VDD33
GR55 4.7K
PHYRSTB — GR56 NC/0R PCIRST → MAC-RST
GC54 0.01uF

RTL8211CN: GR58 (NC)
RTL8211D/8211E: GR57 (NC)
RTL8201FN /EN: GR58(NC)

For wake on LAN function, please mount GR55 GC54 and remove GR56

Configuration Setting

MII/RMII Setting only for RTL8201FN & RTL8201EN PHYAD2
Setting only for RTL8211E

PHY_VDD33

RTL8201FN USE RMII mode
GR46 4.7K — RX_CTL_PHYAD2 — GR47 NC/4.7K

RTL8201FN/RTL8201EN: RMII Signals:
Pull High for RMII mode
Pull Low for MII mode

REF_CLK - Pin 22
CRS_DV - Pin 36
RXD[1:0] - Pin 16, 14
TX_EN - Pin 27
TXD[1:0] - Pin 24, 23
RX_ER - Pin 39

PHY_VDD33

GR54 NC/4.7K — MDI3- — GR59 NC/4.7K

RTL8201FN: Pull High for LDO Enable
Pull Low for LDO disable

PHY_VDD33

LED1_AD1
LED0_AD0

GR88 NC/4.7K LED2_RXDLY_ENREG GR87 NC/4.7K
GR69 4.7K LED2_RXDLY GR70 NC/4.7K
GR71 4.7K LED1_AD1 GR72 NC/4.7K
GR73 NC/4.7K LED0_AD0 GR74 4.7K

RTL8211D/E: If use 2.5V RGMII please pull down (GR123)RXD0/SELRGV
RTL8211CN/8201EN:GR123,GR124 NC

GR123 NC/4.7K RXD0/SELRGV GR124 4.7K
GR75 NC/4.7K RXD2/AN0 GR76 4.7K
GR77 NC/4.7K RXD3/AN1 GR78 4.7K
VDD33_VDD25 → VDD33_VDD25
GR85 NC/4.7K RXD1/TXDLY GR86 4.7K
GND

RTL8211CN/8211D/8211E:
GR76,GR78: Config for all capability
GR71,GR74: PHY Address=01 (8211D/8211CN)
GR46,GR71,R74: PHY Address=001 (8211E)
GR69,GR85: Without TX/RX Delay

RTL8201EN:
GR88:MII Interface
GR87:SNI Interface
GR71,GR74: PHY Address=01
Other resistors are NC

RTL8201FN:
R78 : REF_CLK Input
R77: REF_CLK Output
R69,R71,R74: PHY Address=001
Other resistors are NC

PHY_VDD33

VDD33

RSET/ENSWREG/CLK125 Co-layout

ENREG/RSET — GR112 NC/0R — ENSWREG
GR113 0R RSET
GR126 NC/4.7K

RTL8211D/E Pin39 is RSET (GR112,GR126 NC)
RTL8211CN Pin39 is ENSWREG (GR113,GR126 NC)
RTL8201FN/EN Pin39 is RXER (GR113 NC)

CLK125/LED2_RXDLY — GC74 22pF
GR114 NC/0R CLK125 → CLK125
GR115 0R LED2_RXDLY

RTL8211D/E / RTL8201FN Pin32 is LED2_RXDLY (GR114 NC)
RTL8211CN Pin32 is CLK125 (GR115 NC)
RTL8201EN Pin32 is interrupt(GR114,GR115 NC)

Reserve for EMI.

LED2_RXDLY_ENREG — GR118 0R ENSWREG
GR119 NC/0R LED2_RXDLY

RTL8211CN Pin38 is LED2_RXDLY (GR118 NC)
RTL8211D/E Pin38 is ENSWREG (GR119 NC)
RTL8201FN/EN Pin 38 is Collision Pin(GR118 & GR119 NC)

RSET/CLK125 — GC73 22pF
GR116 0R CLK125 → CLK125
GR117 NC/0R RSET

RTL8211D/E Pin46 is CLK125 (GR117 NC)
RTL8211CN Pin46 is RSET (GR116 NC)
RTL8201FN/EN Pin46 is RSET(GR116 NC)

Reserve for EMI.

PHY_AVDD33

PHY_VDD33

RTL8211D/E:GC45(NC)
RTL8211CN:GC45(NC)

GC45 NC/0.1uF

AVDD33_CEN — GR83 0 R
GC47 0.1uF
GR83 Close to Pin41

U17

RTL8201EN:GR79(NC)
RTL8201FN: GR79,GR84(NC)
RTL8211CN/8211D/8211E:GR84(NC)

PHY_VDD10

GR79 0R
GR84 NC/4.7K

RTL8211CN
RTL8211D/E
RTL8201EN/FN

MDI0+ 1 MDI[0]+
MDI0- 2 MDI[0]-
PHY_AVDD10 3 AVDD10
MDI1+ 4 MDI[1]+
MDI1- 5 MDI[1]-
PHY_AVDD33 6 AVDD33
MDI2+ 7 MDI[2]+
MDI2- 8 MDI[2]-
PHY_AVDD10 9 AVDD10-0
MDI3+ 10 MDI[3]+
MDI3- 11 MDI[3]-
TXER 12 NC

PGND 49
REGOUT 48
GND 47
RSET/CLK125 46
VDDREG 45
VDDREG 44
CKXTAL2 43
CKXTAL1 42
AVDD33-1 41
AVDD10-1 40
ENREG/RSET 39
DVDD33-1 37
REGOUT
RSET/CLK125
VDDREG
VDDREG
XTAL2
XTAL1
AVDD33_CEN
PHY_AVDD10
ENREG/RSET
LED2_RXDLY_ENREG

DVDD10-0 36 PHY_VDD10_CRS
LED1/PHYAD1 35 LED1_AD1
LED0/PHYAD0 34 LED0_AD0
PME 33 PME
CLK125/LED2_RXDLY 32 CLK125/LED2_RXDLY
MDIO 31 MDIO
MDC 30 MDC
PHYRSTB 29 PHYRSTB
DVDD10 28 PHY_VDD10
TXCTL 27 TX_CTL
TXD3 26 TXD3
TXD2 25 TXD2
LED2RXDLY/INTBENREG

RXCTL/PHYAD2 13
RXD0/SELRGV 14
DVDD33 15
RXD1/TXDLY 16
RXD2/AN0 17
RXD3/AN1 18
RXC 19
INT 20
DVDD33-0 21
TXC 22
TXD0 23
TXD1 24

RX_CTL_PHYAD2 13
RXD0/SELRGV 14
VDD33_VDD25 15
RXD1/TXDLY 16
RXD2/AN0 17
RXD3/AN1 18
RX_CLK 19
INT 20
VDD33_VDD25 21
TX_CLK 22
TXD0 23
TXD1 24

RGMII/RMII

11 MDI3- MDI3-
11 MDI3+ MDI3+
11 MDI2- MDI2-
11 MDI2+ MDI2+
11 MDI1- MDI1-
11 MDI1+ MDI1+
11 MDI0- MDI0-
11 MDI0+ MDI0+

R35,36,37 Only for RTL8201FN/EN

PHY_VDD10_CRS — GR35 NC/0R — CRS_N → CRS_N
LED2_RXDLY_ENREG — GR36 NC/0R — COL_N → COL_N
ENSWREG — GR37 0R — RXER_N → RXER_N

Place filter network close to RX_CLK.
Reserved for EMI

RX_CLK — GR49 22R — RX_CLK_N
GC46 18pF

RX_CTL_PHYAD2 — GR48 22R — RX_CTL_N
RXD0/SELRGV — GR50 22R — RXD0_N
RXD1/TXDLY — GR51 22R — RXD1_N
RXD2/AN0 — GR52 22R — RXD2_N
RXD3/AN1 — GR53 22R — RXD3_N

RX_CTL_N → RX_CTL_N
RXD0_N → RXD0_N
RXD1_N → RXD1_N
RXD2_N → RXD2_N
RXD3_N → RXD3_N

TX_CLK
TX_CTL
TXER
TXD0
TXD1
TXD2
TXD3

Close to PHY
Reserve for EMI

RSET

RSET — GR6 2.49K(1%)

Others

VDDREG
PHY_VDD10
PHY_AVDD10
REGOUT
PHY_VDD33

ChipHD to Pine64

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