VERSION HISTORY

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Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Release version	2015-04-22			
Ver 1.2		2018-01-26			

ChipHD to Pine64

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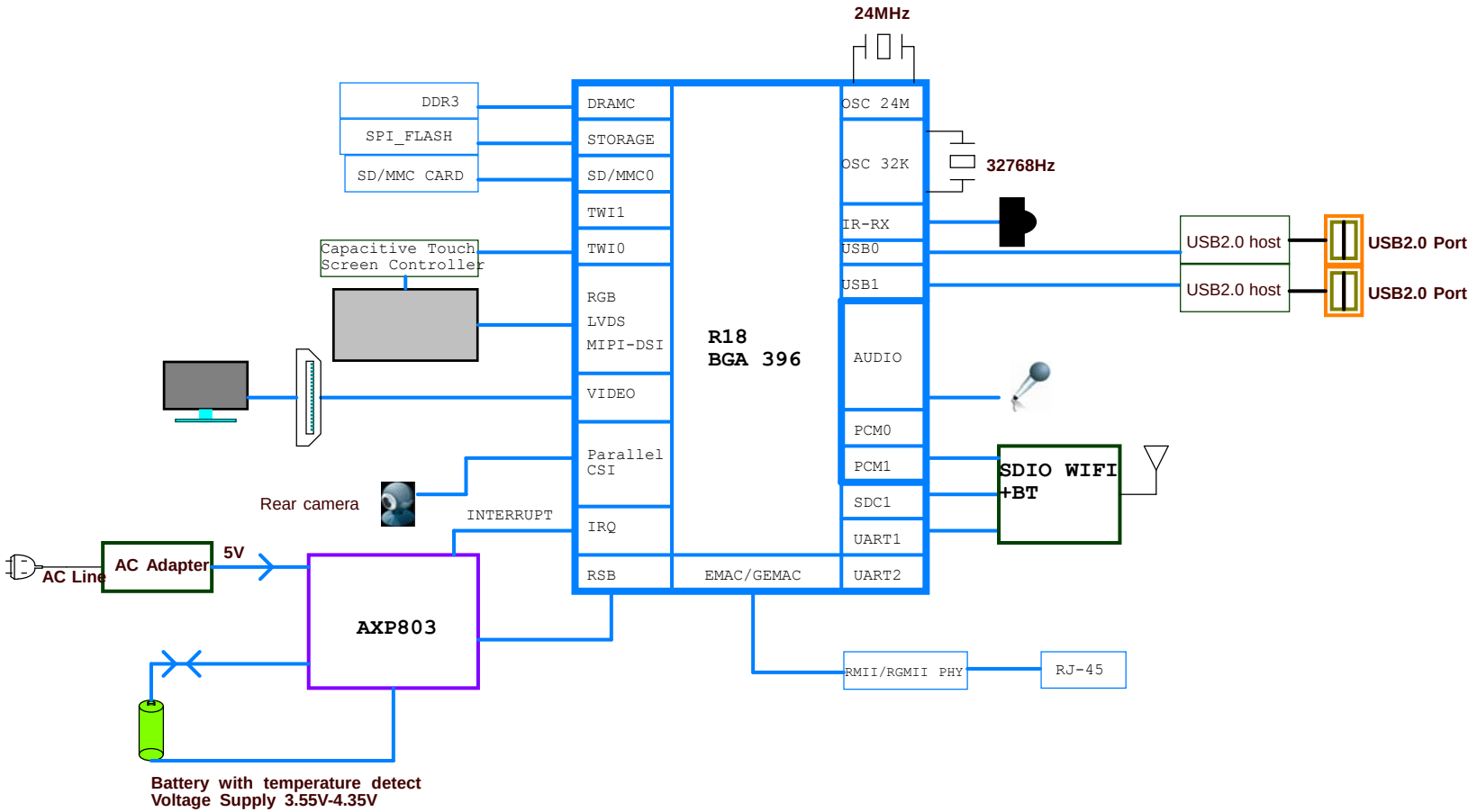
BLOCK DIAGRAM



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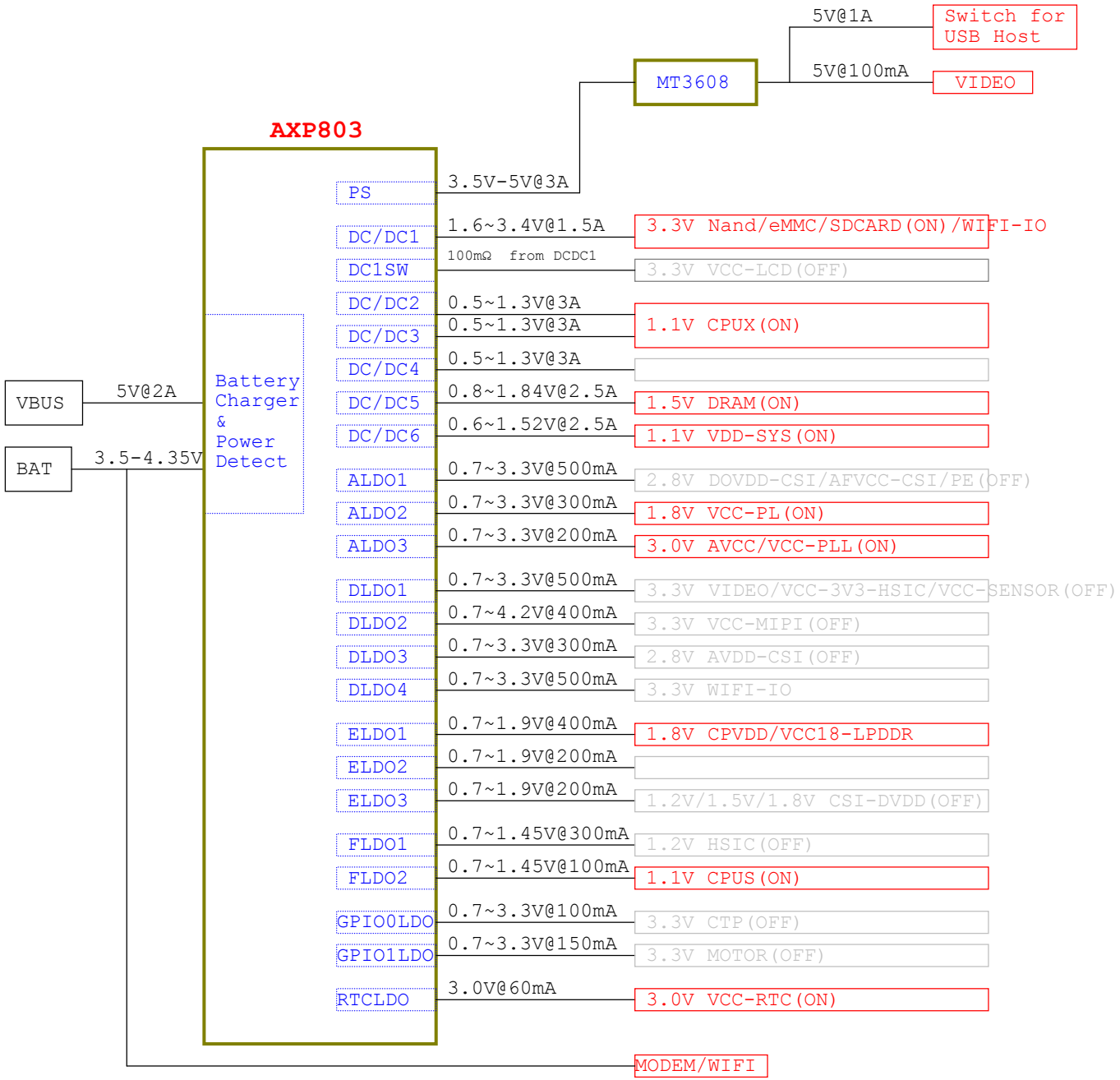
POWER TREE



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A3	POWER TREE	V1.2

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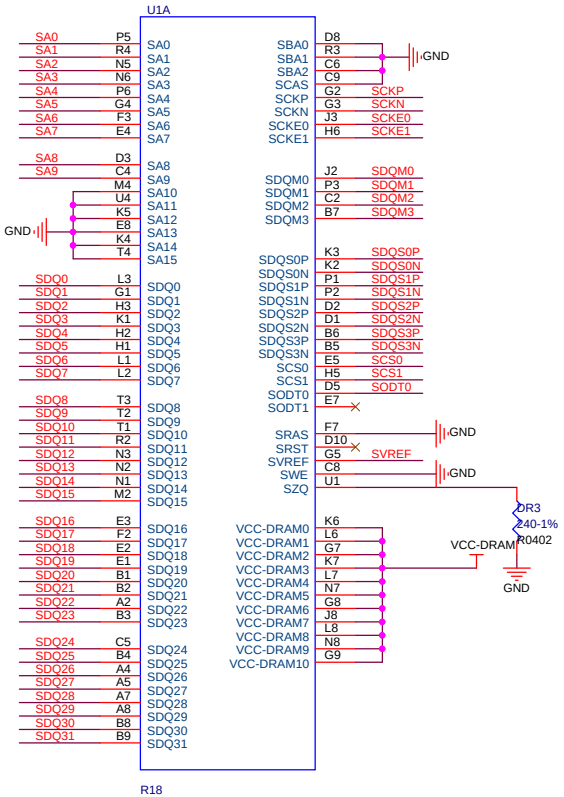
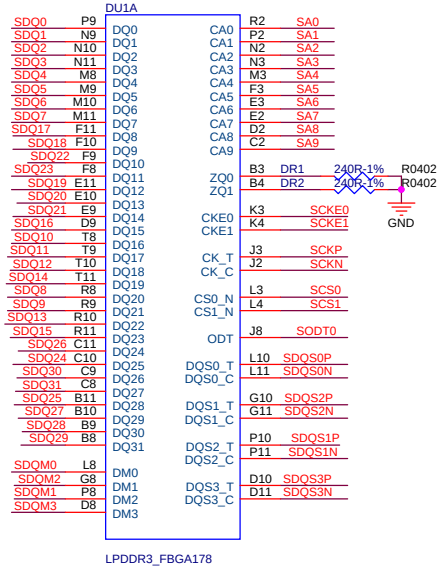
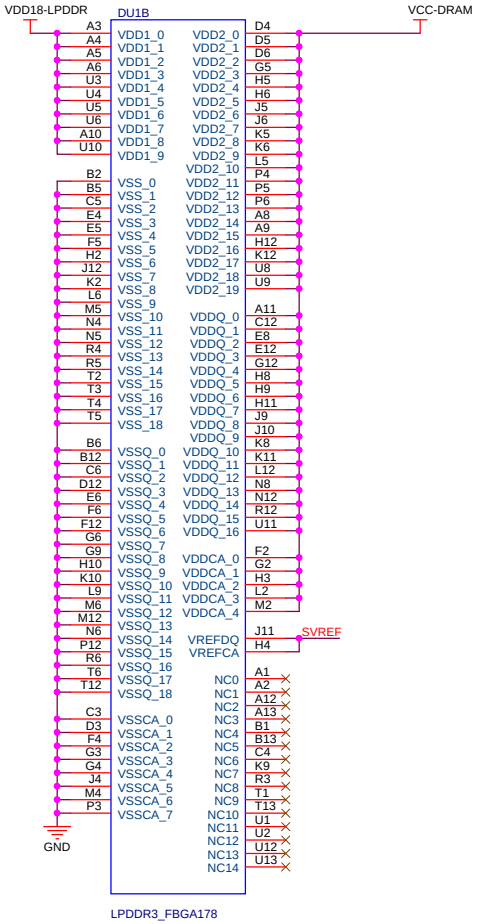
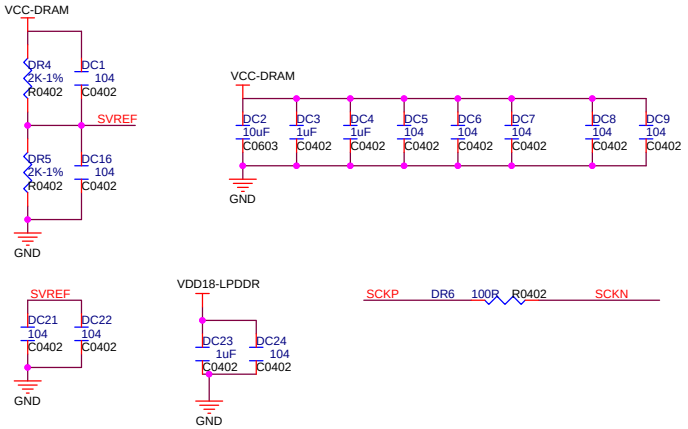
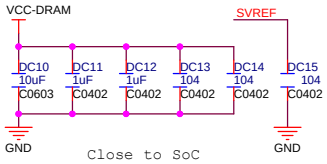
LPDDR3 32X1











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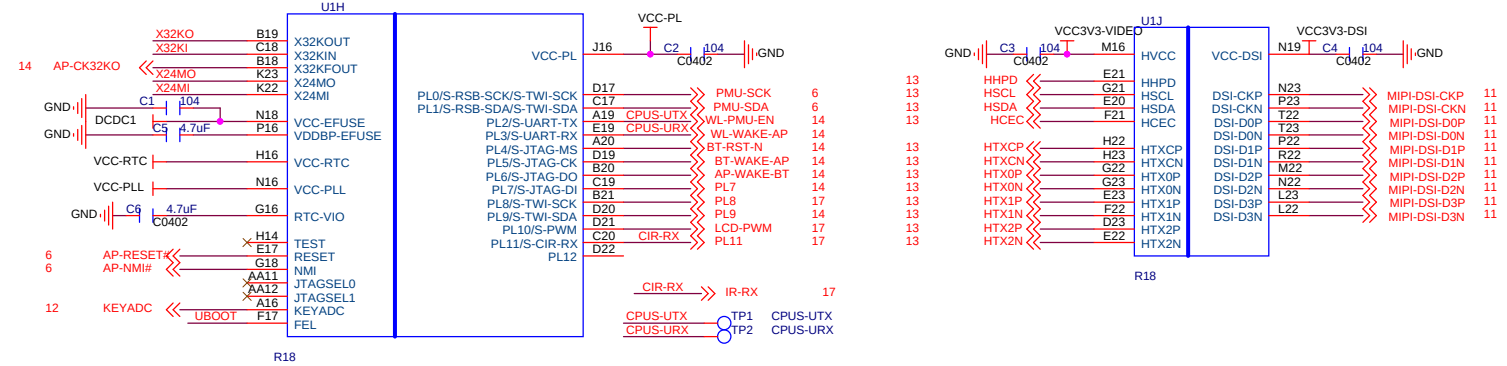
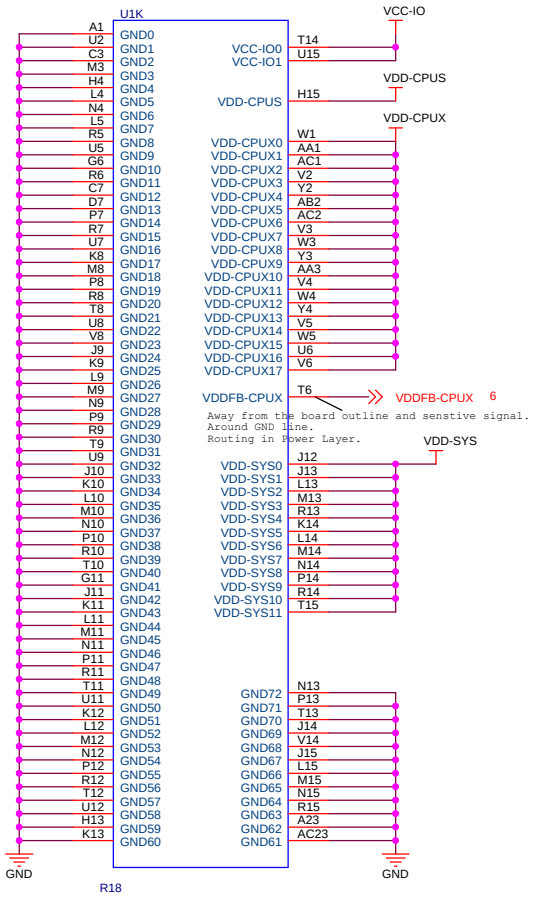
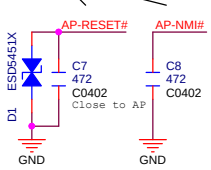
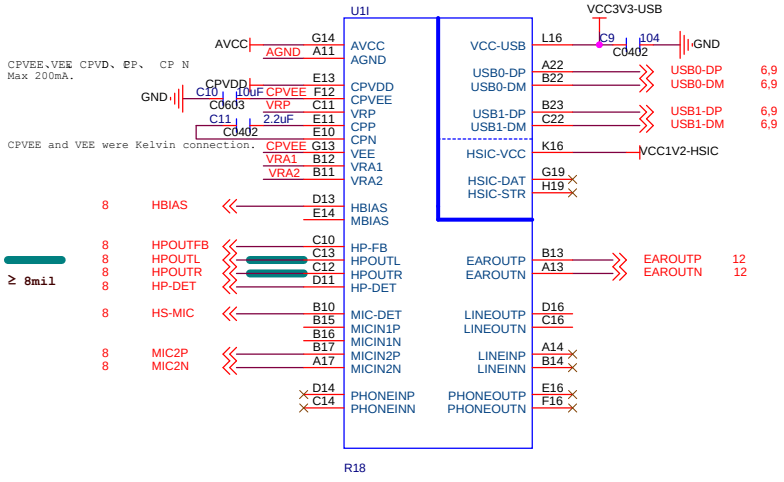
CPU

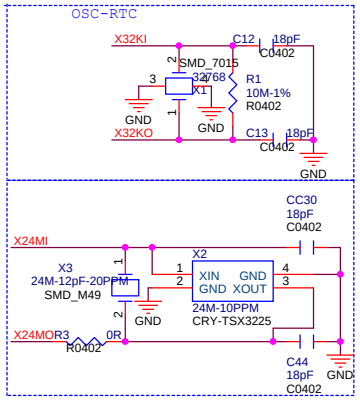


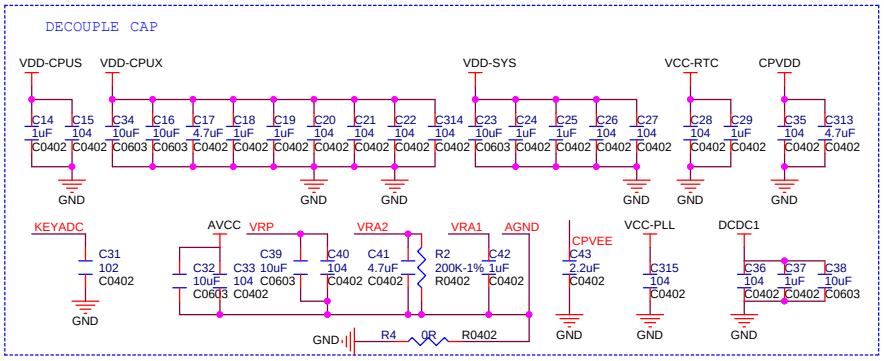


Away from the board outline and senstive signal.
Around GND line.









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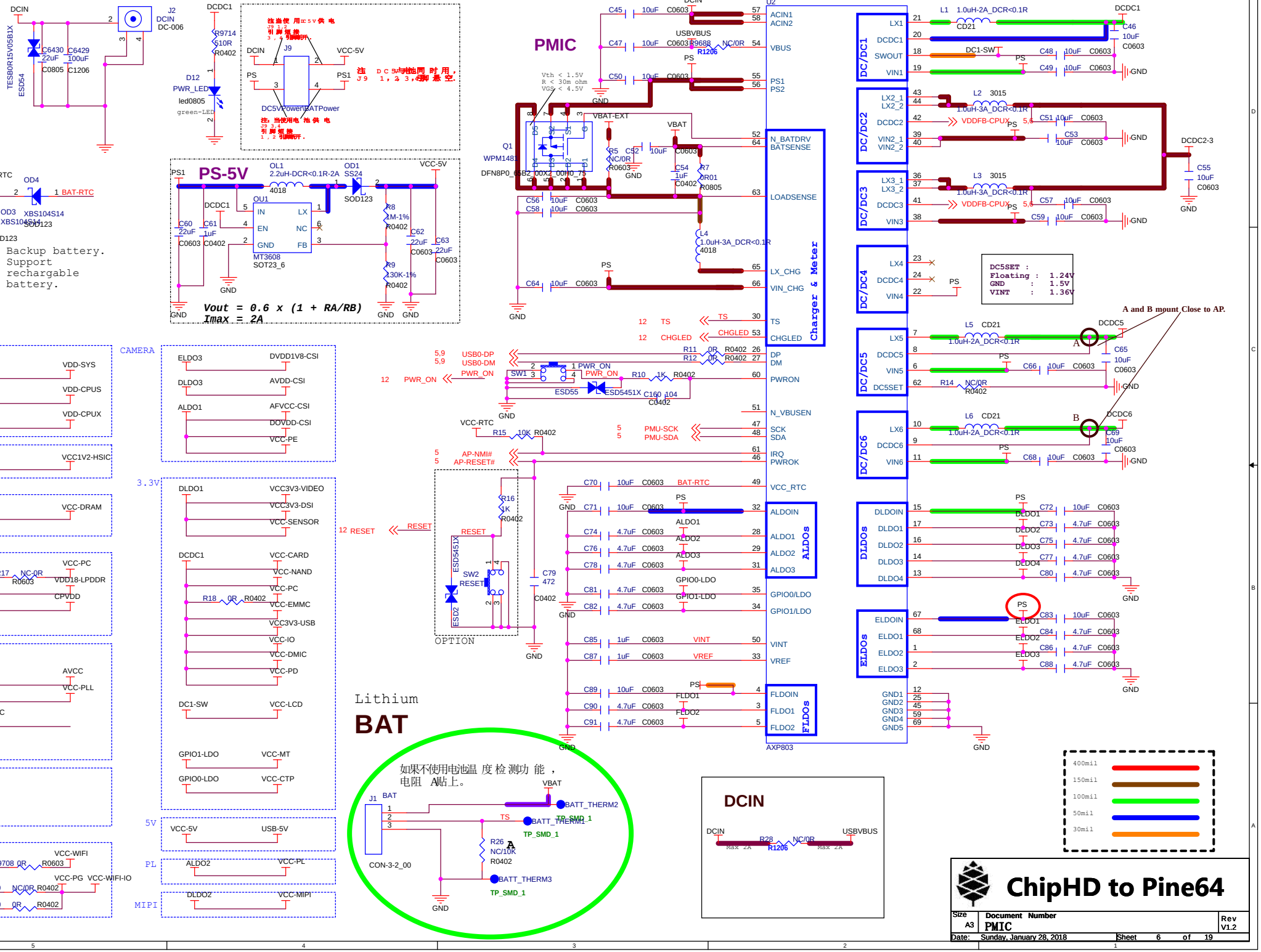
Power


DCIN
J2
DCIN
DC-006
TESB0R15V05B1X
ESD54
C6430
22uF
C0805
C6429
100uF
C1206
DCDC1
R9714
510R
R0402
D12
PWR_LED
led0805
green-LED
J9
VCC-5V
PS
PS1
DC5V/PowerBATPower
PS-5V
OL1
2.2uH-DCR<0.1R-2A
4018
OD1
SS24
SOD123
OU1
MT3608
SOT23_6
IN
LX
EN
NC
GND
FB
C60
22uF
C0603
C61
1uF
C0402
R8
1M-1%
R0402
R9
130K-1%
C62
22uF
C0603
C63
22uF
C0603
Vout = 0.6 x (1 + RA/RB)
Imax = 2A
VCC-RTC
OD4
BAT-RTC
OD3
XBS104S14
SOD123
BT1
CR2032
CON-2-2_00
Backup battery.
Support
rechargable
battery.
PMIC
Vth < 1.5V
R < 30m ohm
VGS < 4.5V
Q1
WPM1481
DFN8P0_6SB2_00X2_00H0_75
VBAT-EXT
VBAT
R5
NC/0R
R0603
C52
10uF
C0603
C54
1uF
C0402
R7
0R01
R0805
L4
1.0uH-3A_DCR<0.1R
4018
C56
10uF
C0603
C58
10uF
C0603
C64
10uF
C0603
C45
10uF
C0603
C47
10uF
C0603
R9688
NC/0R
R1206
C50
10uF
C0603
U2
ACIN1
ACIN2
VBUS
PS1
PS2
N_BATDRV
BATSENSE
LOADSENSE
LX_CHG
VIN_CHG
Charger & Meter
TS
CHGLED
DP
DM
PWRON
N_VBUSEN
SCK
SDA
IRQ
PWROK
VCC_RTC
ALDOIN
ALDO1
ALDO2
ALDO3
ALDOs
GPIO0-LDO
GPIO1-LDO
VINT
VREF
FLDOIN
FLDO1
FLDO2
FLDOs
AXP803
USB0-DP
USB0-DM
PWR_ON
SW1
ESD55
ESD5451X
C160
104
C0402
PMU-SCK
PMU-SDA
AP-NMI#
AP-RESET#
R15
10K
R0402
R16
1K
R0402
RESET
SW2
ESD5451X
ESD2
C79
472
C0402
OPTION
DC/DC1
DC/DC2
DC/DC3
DC/DC4
DC/DC5
DC/DC6
DLDOs
ELDOs
L1
1.0uH-2A_DCR<0.1R
CD21
DCDC1
C46
10uF
C0603
DC1-SW
C48
10uF
C0603
C49
10uF
C0603
L2
3015
1.0uH-3A_DCR<0.1R
VDDFB-CPUX
C51
10uF
C0603
C53
10uF
C0603
DCDC2-3
C55
10uF
C0603
L3
3015
1.0uH-3A_DCR<0.1R
VDDFB-CPUX
C57
10uF
C0603
C59
10uF
C0603
DC5SET :
Floating : 1.24V
GND : 1.5V
VINT : 1.36V
A and B mount Close to AP.
L5
CD21
1.0uH-2A_DCR<0.1R
DCDC5
C65
10uF
C0603
C66
10uF
C0603
R14
NC/0R
R0402
L6
CD21
1.0uH-2A_DCR<0.1R
DCDC6
C69
10uF
C0603
C68
10uF
C0603
C72
10uF
C0603
C73
4.7uF
C0603
C75
4.7uF
C0603
C77
4.7uF
C0603
C80
4.7uF
C0603
C83
10uF
C0603
C84
4.7uF
C0603
C86
4.7uF
C0603
C88
4.7uF
C0603
GND1
GND2
GND3
GND4
GND5
1.1V
DCDC6
VDD-SYS
FLDO2
VDD-CPUS
DCDC2-3
VDD-CPUX
1.2V
FLDO1
VCC1V2-HSIC
1.2V/
1.35V/
1.5V
DCDC5
VCC-DRAM
1.8V
ELDO1
R17
NC/0R
R0603
VCC-PC
VDD18-LPDDR
CPVDD
3V
ALDO3
AVCC
VCC-PLL
VCC-RTC
BB
WIFI
DLDO4
R9708 0R
R0603
VCC-WIFI
DLDO4
VCC-PG
VCC-WIFI-IO
ELDO1
R19
NC/0R
R0402
R20
0R
R0402
CAMERA
ELDO3
DVDD1V8-CSI
DLDO3
AVDD-CSI
ALDO1
AFVCC-CSI
DOVDD-CSI
VCC-PE
3.3V
DLDO1
VCC3V3-VIDEO
VCC3V3-DSI
VCC-SENSOR
DCDC1
VCC-CARD
VCC-NAND
VCC-PC
R18
0R
R0402
VCC-EMMC
VCC3V3-USB
VCC-IO
VCC-DMIC
VCC-PD
DC1-SW
VCC-LCD
GPIO1-LDO
VCC-MT
GPIO0-LDO
VCC-CTP
5V
VCC-5V
USB-5V
PL
ALDO2
VCC-PL
MIPI
DLDO2
VCC-MIPI
Lithium
BAT
如果不使用电池温 度检测功 能 ，
电阻 A贴上。
J1
BAT
CON-3-2_00
VBAT
BATT_THERM2
TS
BATT_THERM1
TP_SMD_1
R26
NC/10K
R0402
A
BATT_THERM3
TP_SMD_1
DCIN
R28
NC/0R
R1206
USBVBUS
Max 2A
Max 2A
400mil
150mil
100mil
50mil
30mil
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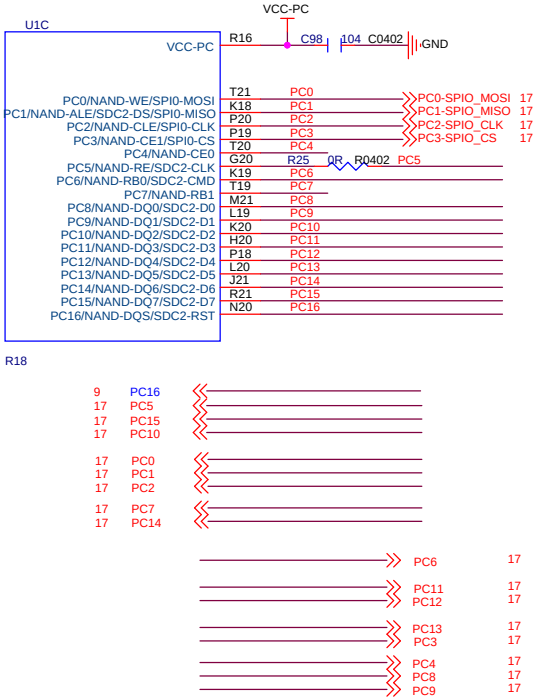
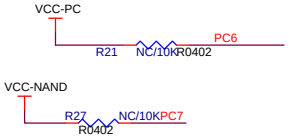
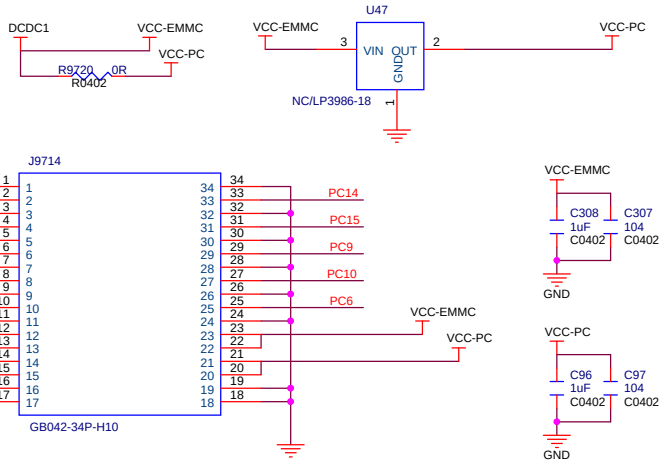
eMMC/SPI_FLASH

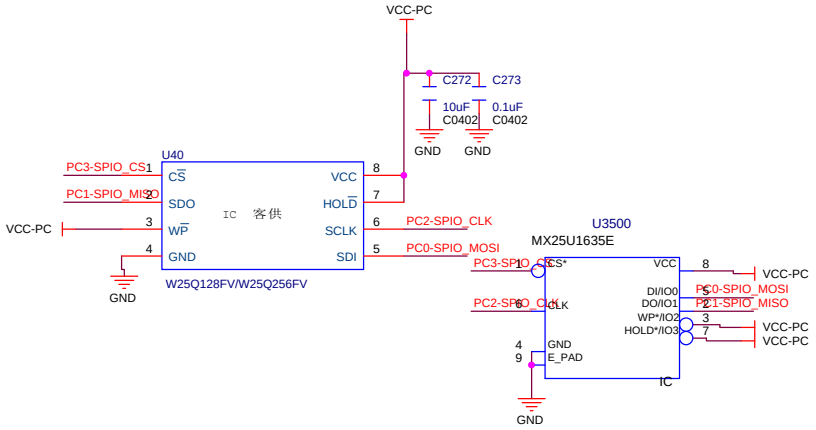




eMMC socket



SPI_FLASH



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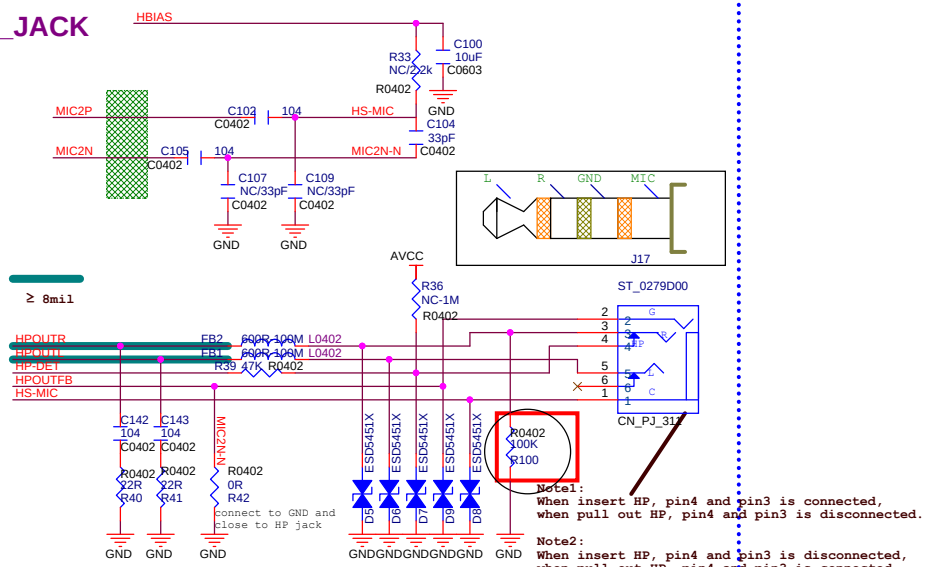
AUDIO

HP_JACK



Note1:
When insert HP, pin4 and pin3 is connected,
when pull out HP, pin4 and pin3 is disconnected.

Note2:
When insert HP, pin4 and pin3 is disconnected,
when pull out HP, pin4 and pin3 is connected.
Mount R100 3.3K.

5 HBIAS

5 HP-DET
5 HPOUTFB
5 HPOUTL
5 HPOUTR

5 MIC2N
5 MIC2P

5 HS-MIC

5 EAROUTP
5 EAROUTN

AVCC

VCC-5V

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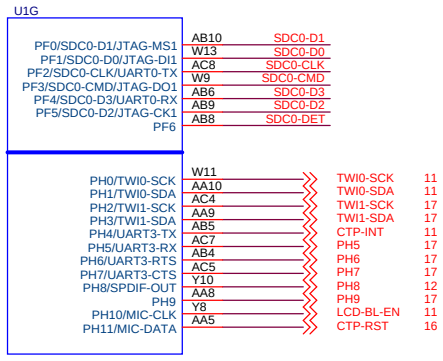
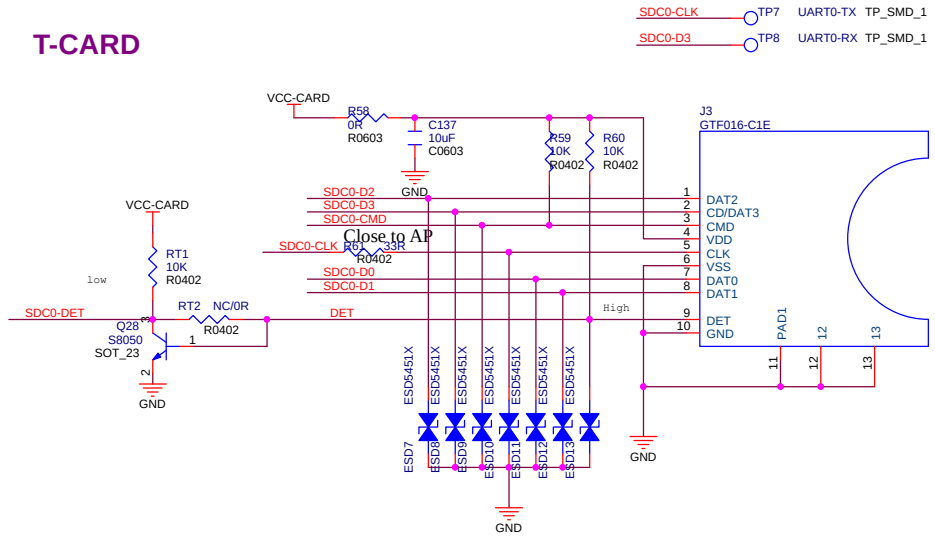
USB/T-CARD

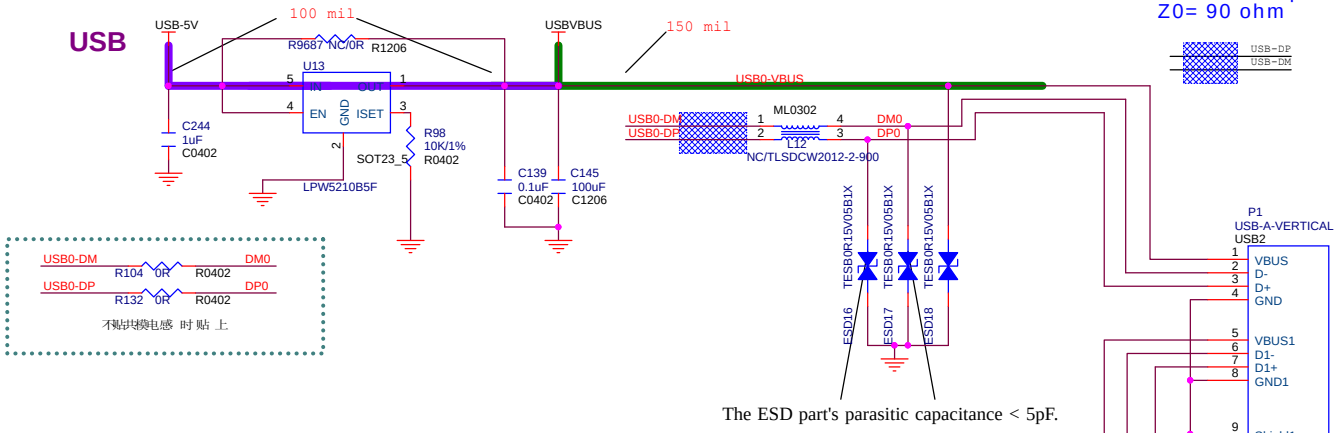
T-CARD



VCC-CARD



USB

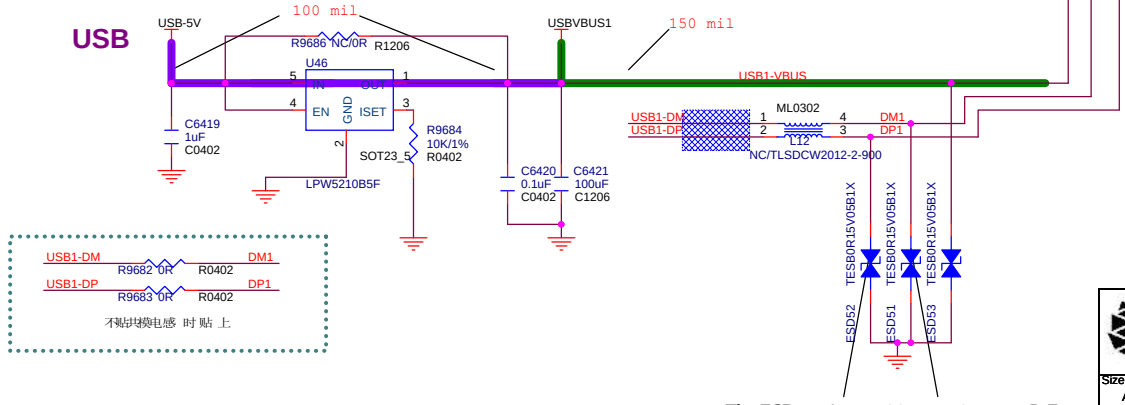


5,6 USB0-DM
5,6 USB0-DP
5,6 USB1-DM
5,6 USB1-DP

USB-5V

DCDC1

USB



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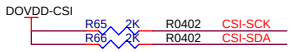
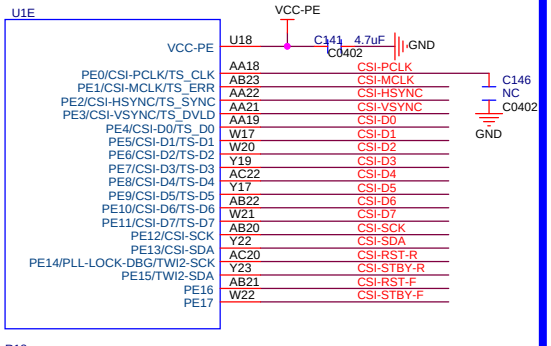
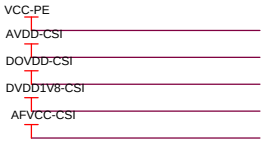
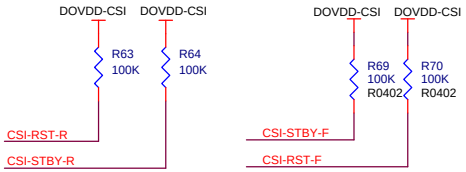
CAMERA

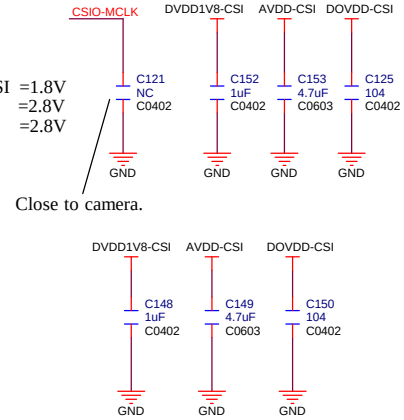


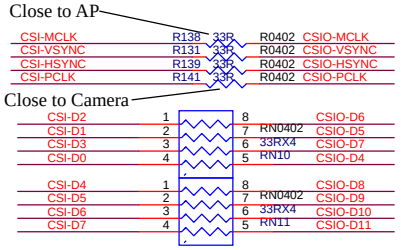


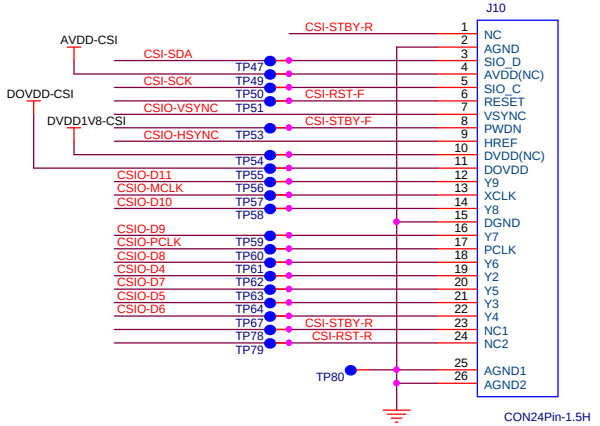




DVDD1V8-CSI =1.8V
DOVDD-CSI =2.8V
AVDD-CSI =2.8V







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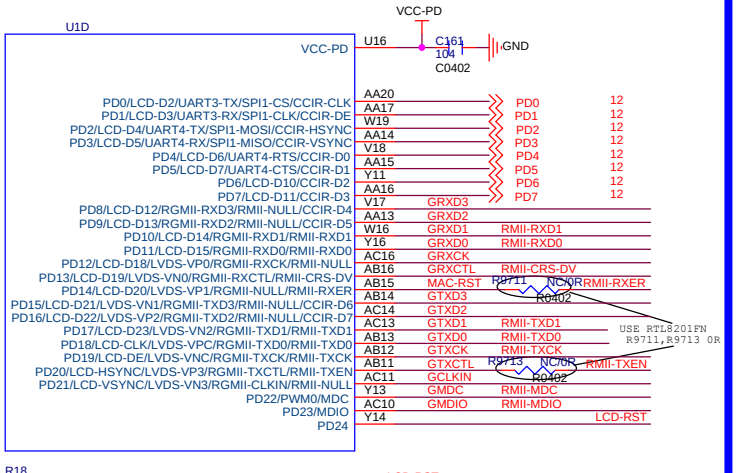
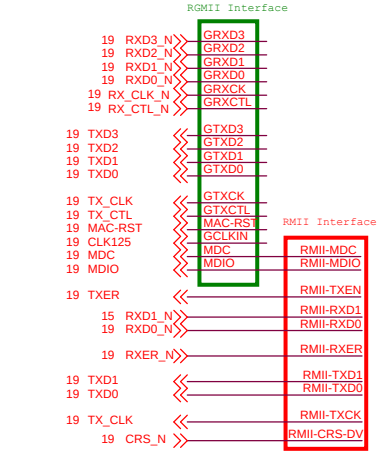
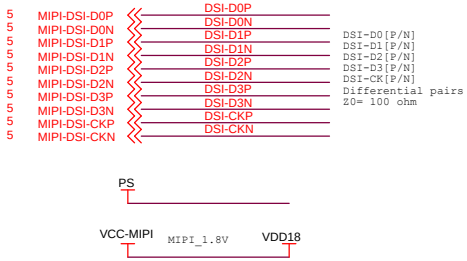
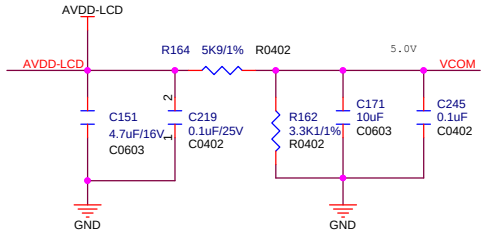
LCD

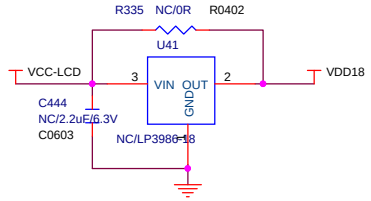


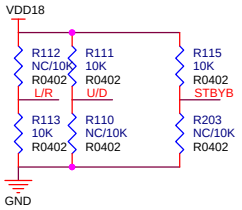


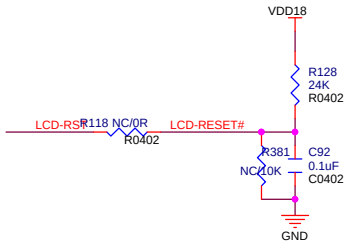


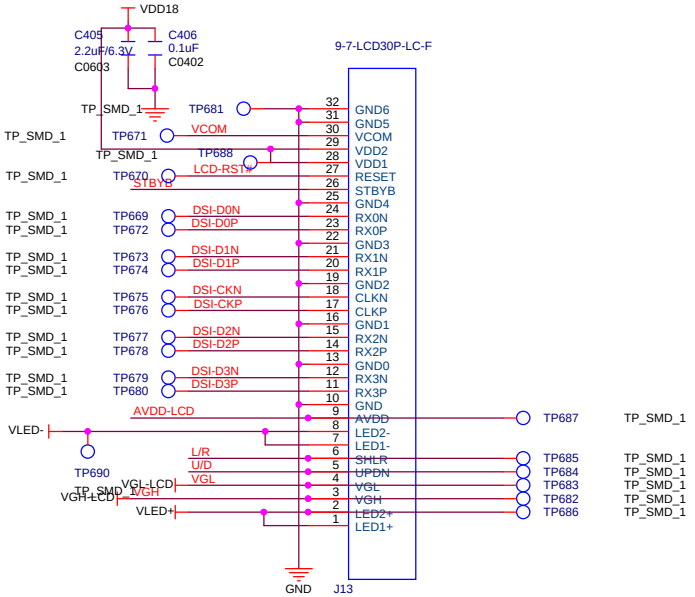
MIPI-LCD

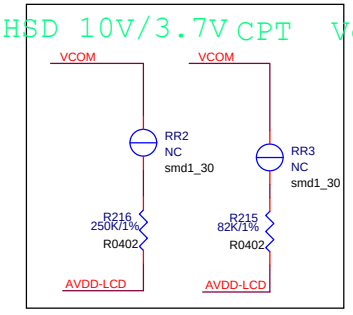












ChipHD to Pine64

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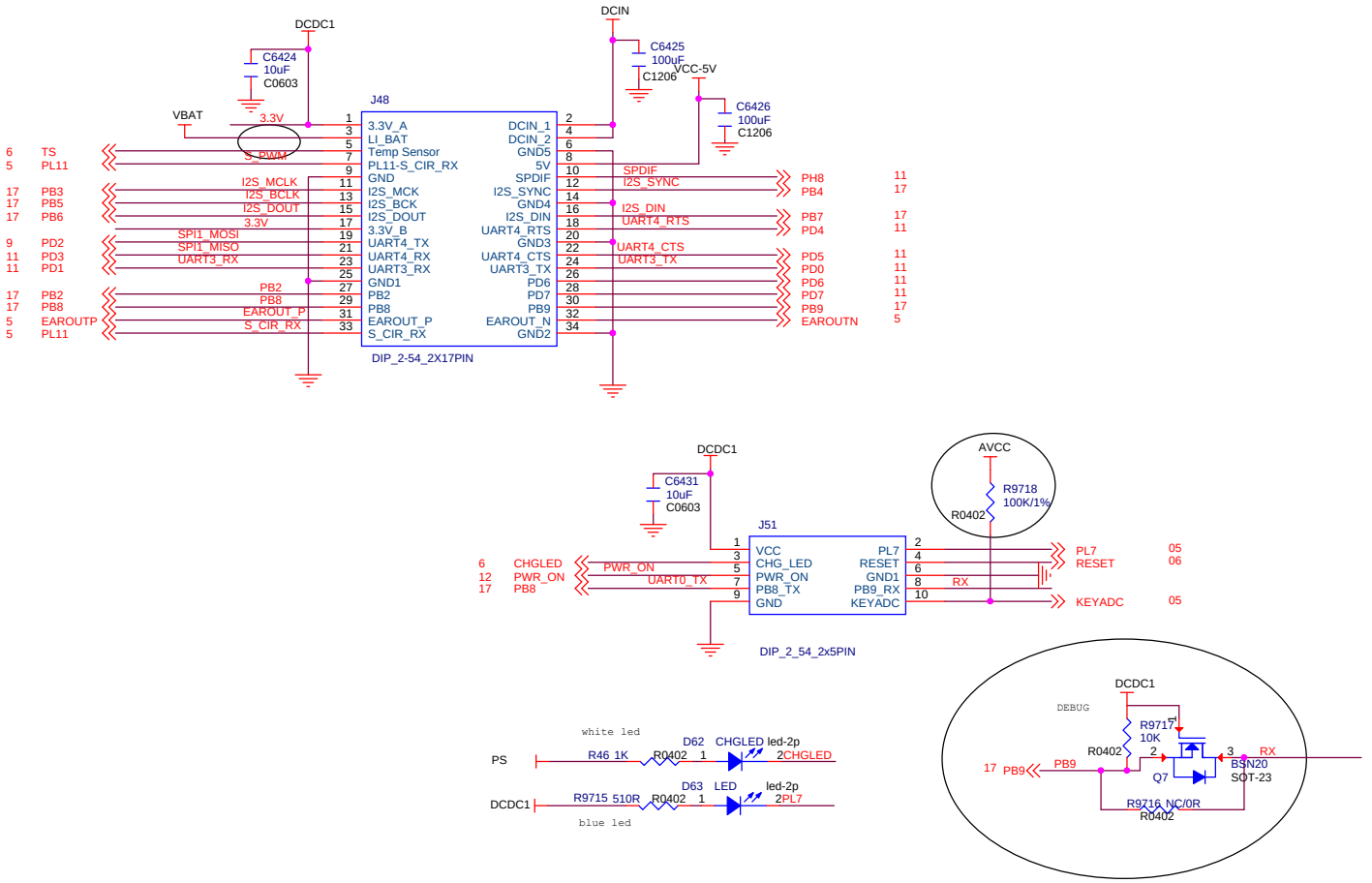
Euler e Connector



ChipHD to Pine64

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A3	Euler e Connector	V1.2

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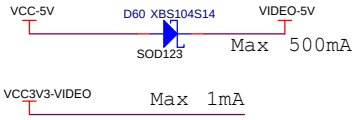
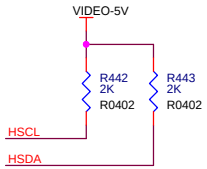
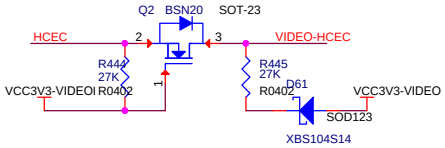
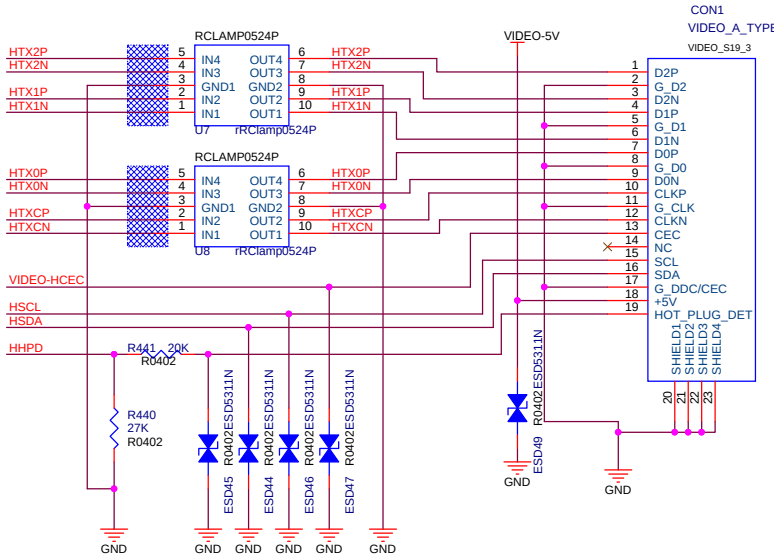
VIDEO



Differential pairs
Z0= 100 ohm







ChipHD to Pine64

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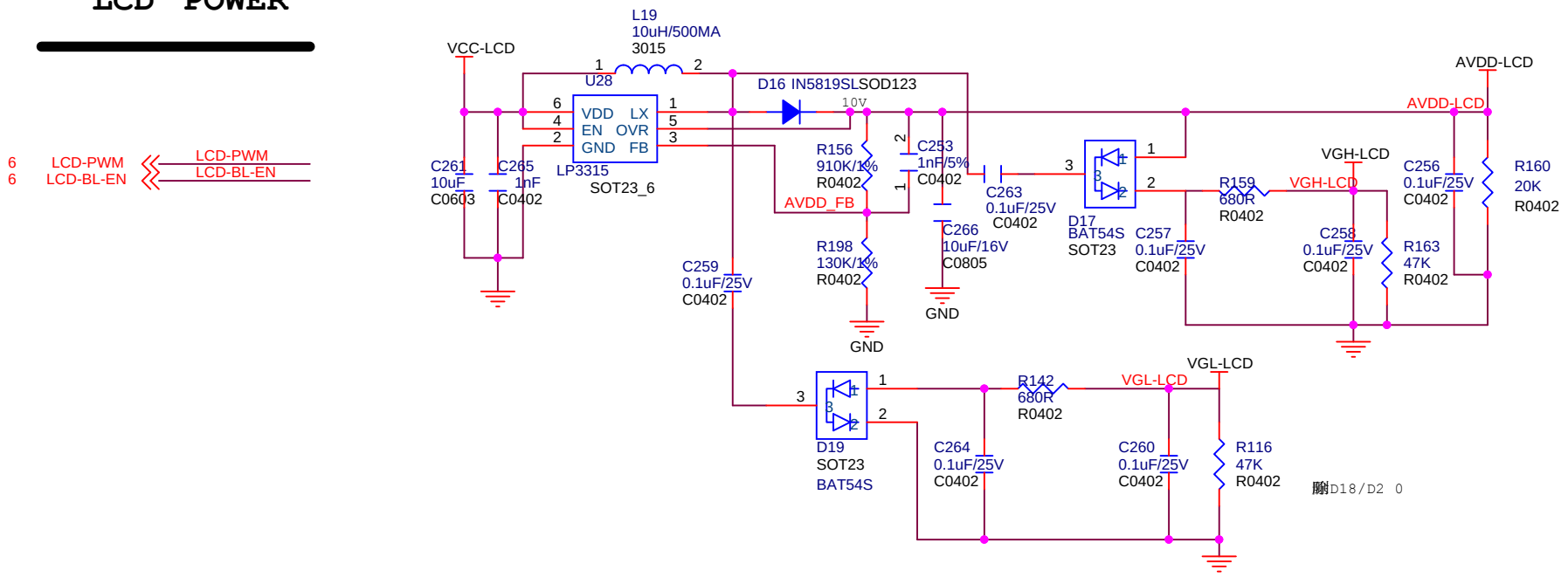
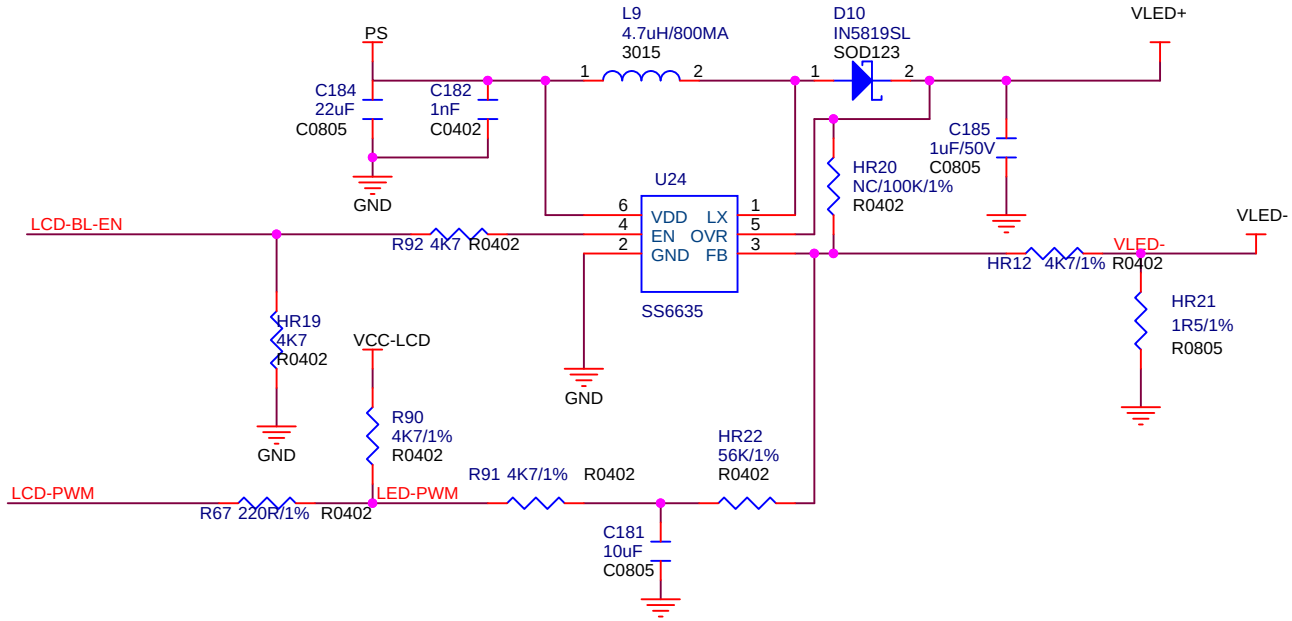
LCD POWER



Backlight



Size A4	Document Number LED POWER		Rev V1.2
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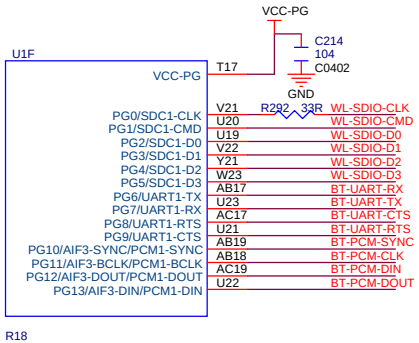
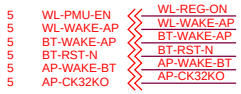
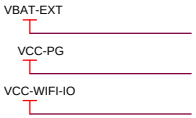
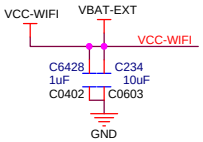
ChipHD to Pine64

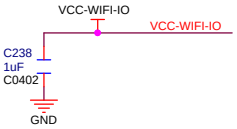
WIFI+BT

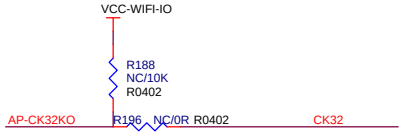


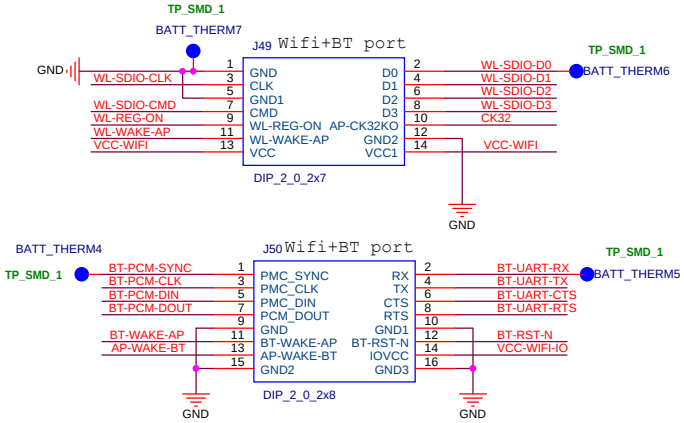












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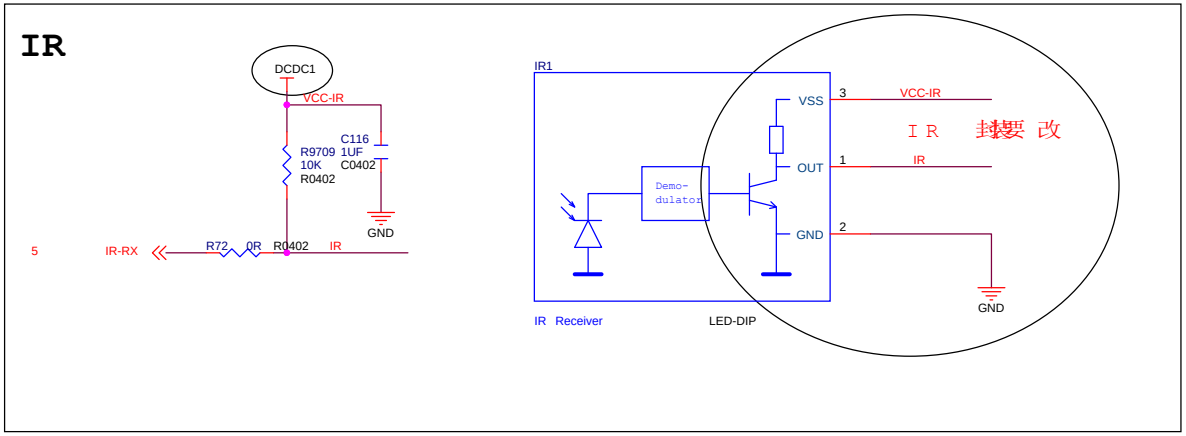
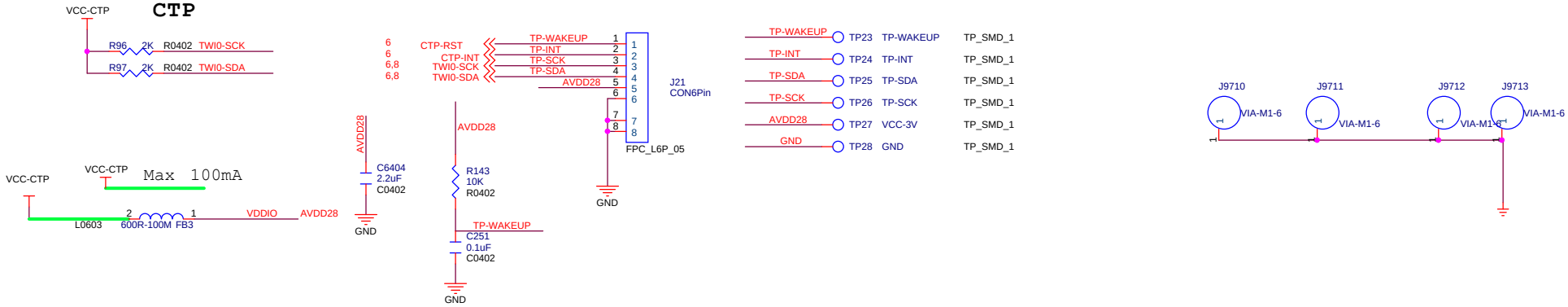
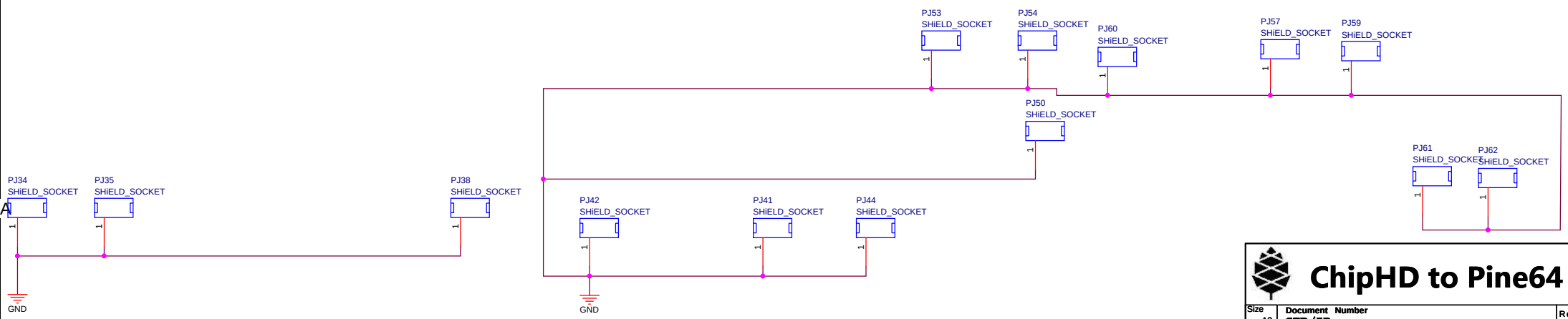
CTP/IR

IR



CTP





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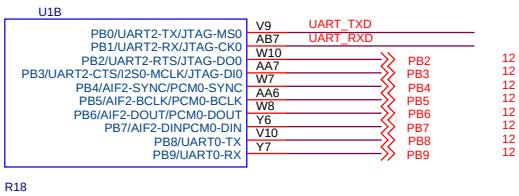
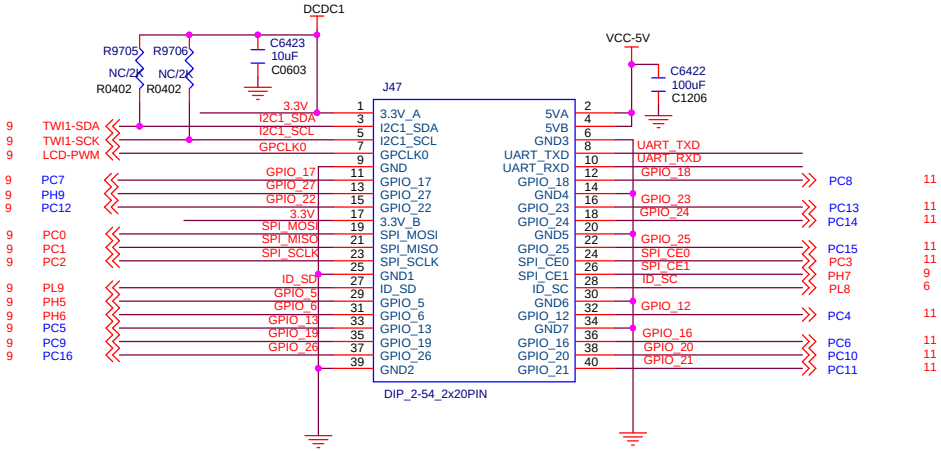
Pi-2 Connector





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A3	Pi-2 Connector	V1.2

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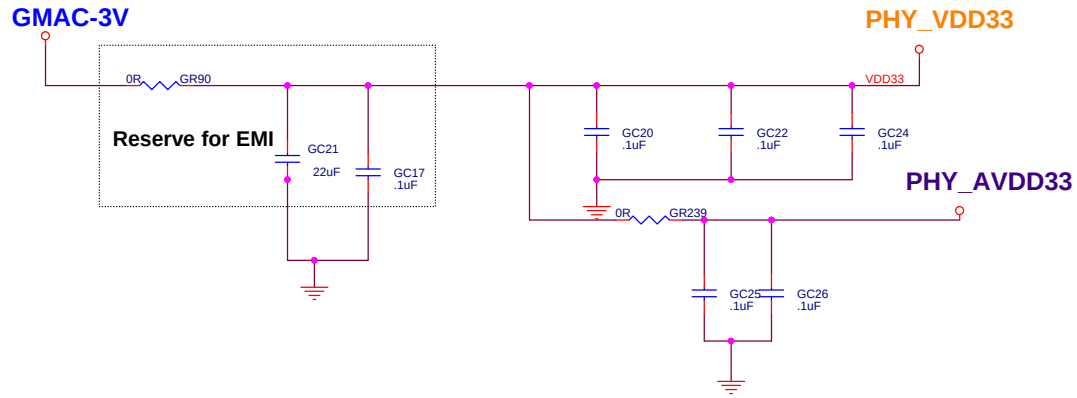
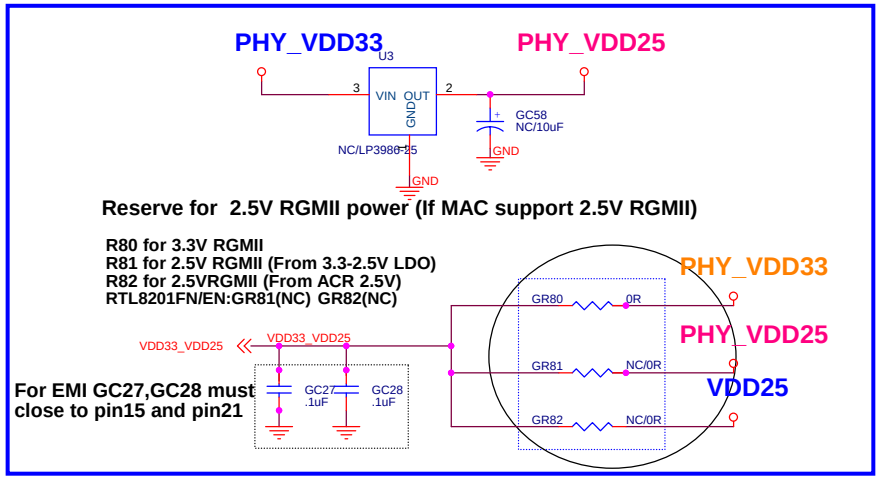
GMAC-3V



3.3/2.5V RGMII Power



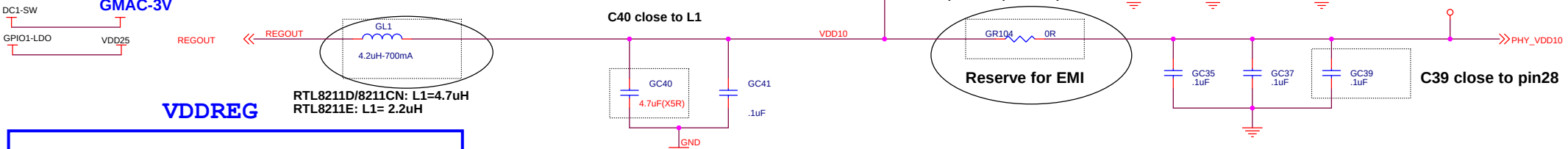
RTL8211CN/D/E	GL1	C56	U10	GR65	GR66	GR122	GC41/GC57
Enable switching regulator	O	O	X	O	X	X	O
Disable switching regulator	X	X	O	X	O	O	X

Note 1: The Trace length between GL1 and Pin 48 must be within 0.5 cm. GC40 and GC41 toG L1 must be within 0.5cm.

RTL8211D/8211CN:GC40 22uF(X5R)
RTL8211E: GC40 4.7uF(X5R)

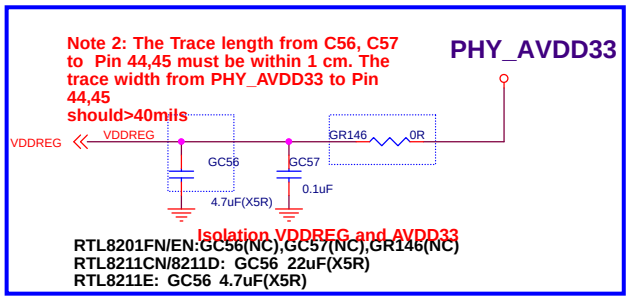
C40 close to L1

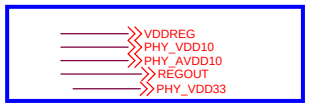
GMAC-3V



RTL8211D/8211CN: L1=4.7uH
RTL8211E: L1= 2.2uH

VDDREG



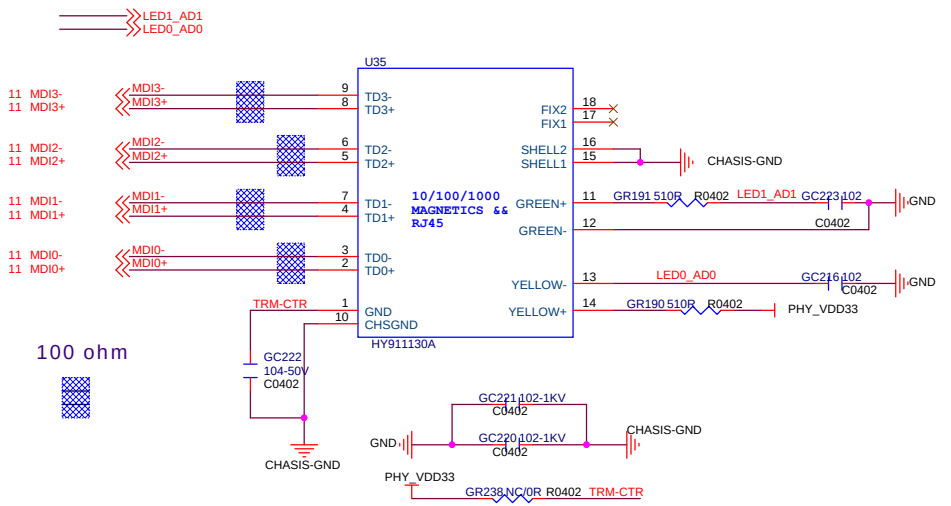


External Power Source

U10,GC69,GC68, GR122,GR120 and GR121 are only used by 8211CN/8211D/8211E application when switching regulator is disabled. For other applications, please remove them.

RESERVE

PHY_AVDD10



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RTL8211CN/8211D/8211E/8201FN/8201EN

PME

PHY_VDD33

Note: PME Function
RTL8211D/8211E/ 8201FN only
RTL8201EN/8211CN Pin33 is NC

GR109 4.7K

PME → PME

Interrupt

PHY_VDD33

GR127 for RTL8201EN INT function

CLK125/LED2_RXDLY — GR127 0 — INT → INT

GR106 4.7K

MDC/MDIO

PHY_VDD33

MDIO — GR38 1.5K — GR125 NC/0 — GR128 0 — VDD33_VDD25

MDIO → MDIO
MDC → MDC

RTL8201FN/EN/8211CN/8211D: GR128(NC)
RTL8211E:GR125(NC)

Configuration Setting

MII/RMII Setting only for RTL8201FN & RTL8201EN PHYAD2
Setting only for RTL8211E

PHY_VDD33

RTL8201FN USE RMII mode
GR46 4.7K — RX_CTL_PHYAD2 — GR47 NC/4.7K

RTL8201FN/RTL8201EN: RMII Signals:
Pull High for RMII mode — REF_CLK - Pin 22
Pull Low for MII mode — CRS_DV - Pin 36
RXD[1:0] - Pin 16, 14
TX_EN - Pin 27
TXD[1:0] - Pin 24, 23
RX_ER - Pin 39

PHY_VDD33

VDD33

PHY_VDD33

GR54 NC/4.7K — MDI3- — GR59 NC/4.7K

RTL8201FN: Pull High for LDO Enable
Pull Low for LDO disable

PHY_VDD33

LED1_AD1
LED0_AD0

GR88	NC/4.7K	LED2_RXDLY_ENREG	GR87	NC/4.7K	
GR69	NC/4.7K	LED2_RXDLY	GR70	4.7K	
GR71	4.7K	LED1_AD1	GR72	NC/4.7K	
GR73	NC/4.7K	LED0_AD0	GR74	4.7K	

RTL8211D/E: If use 2.5V RGMII please pull down (GR123)RXD0/SELRGV
RTL8211CN/8201EN:GR123,GR124 NC

GR123	NC/4.7K	RXD0/SELRGV	GR124	4.7K	
GR75	NC/4.7K	RXD2/AN0	GR76	4.7K	VDD33_VDD25
GR77	NC/4.7K	RXD3/AN1	GR78	4.7K	
GR85	NC/4.7K	RXD1/TXDLY	GR86	4.7K	

GND

RTL8211CN/8211D/8211E:
GR76,GR78: Config for all capability
GR71,GR74: PHY Address=01 (8211D/8211CN)
GR46,GR71,R74: PHY Address=001 (8211E)
GR69,GR85: Without TX/RX Delay

RTL8201EN:
GR88:MII Interface
GR87:SNI Interface
GR71,GR74: PHY Address=01
Other resistors are NC

RTL8201FN:
R78 : REF_CLK Input
R77: REF_CLK Output
R69,R71,R74: PHY Address=001
Other resistors are NC

External clock and Crystal

External clock source from OSC or Chipset.

XTAL1 — X5 (GND XIN / XOUT GND) — XTAL2
GC1 27pF — 25M-10PPM CRY-TSX3225 — GC2 27pF

Use external clock:
RTL8201FN/RTL8201EN/8211CN/8211D/8211E: GR105(0 ohm)

Enable/Disable SWREG

PHY_AVDD33

ENSWREG — GR65 0R — GR66 NC/0R

Connect ENSWREG to PHY_AVDD33 to enable Switching regulator or connect ENSWREG to GND to disable Switching regulator.

RTL8201FN /EN:
GR65 is Fiber Mode
GR66 is UTP Mode(default)

PHY Reset

GR57 NC/0R/VDD33_VDD25 → VDD33_VDD25
GR58 0R PHY_VDD33 → PHY_VDD33
GR55 4.7K
PHYRSTB — GR56 NC/0R PCIRST → MAC-RST
GC54 0.01uF

RTL8211CN: GR58 (NC)
RTL8211D/8211E: GR57 (NC)
RTL8201FN /EN: GR58(NC)

For wake on LAN function, please mount GR55 GC54 and remove GR56

RSET/ENSWREG/CLK125 Co-layout

ENREG/RSET — GR112 NC/0R — ENSWREG
GR113 0R — RSET
GR126 NC/4.7K

RTL8211D/E Pin39 is RSET (GR112,GR126 NC)
RTL8211CN Pin39 is ENSWREG (GR113,GR126 NC)
RTL8201FN/EN Pin39 is RXER (GR113 NC)

CLK125/LED2_RXDLY — GC74 22pF — GR114 NC/0R — CLK125
GR115 0R — LED2_RXDLY

RTL8211D/E / RTL8201FN Pin32 is LED2_RXDLY (GR114 NC)
RTL8211CN Pin32 is CLK125 (GR115 NC)
RTL8201EN Pin32 is interrupt(GR114,GR115 NC)

Reserve for EMI.

LED2_RXDLY_ENREG — GR118 0R — ENSWREG
GR119 NC/0R — LED2_RXDLY

RTL8211CN Pin38 is LED2_RXDLY (GR118 NC)
RTL8211D/E Pin38 is ENSWREG (GR119 NC)
RTL8201FN/EN Pin 38 is Collision Pin(GR118 & GR119 NC)

RSET/CLK125 — GC73 22pF — GR116 0R — CLK125
GR117 NC/0R — RSET

RTL8211D/E Pin46 is CLK125 (GR117 NC)
RTL8211CN Pin46 is RSET (GR116 NC)
RTL8201FN/EN Pin46 is RSET(GR116 NC)

Reserve for EMI.

PHY_AVDD33 / PHY_VDD33

RTL8211D/E:GC45(NC)
RTL8211CN:GC45(NC)

GC45 1uF

AVDD33_CEN — GR83 0 — GC47 1uF

GR83 Close to Pin41

U17

RTL8201EN:GR79(NC)
RTL8201FN: GR79,GR84(NC)
RTL8211CN/8211D/8211E:GR84(NC)

PHY_VDD10

GR79 0 (NC)
GR84 4.7K

RTL8211CN
RTL8211D/E
RTL8201EN/FN

MDI0+	1	MDI[0]+	
MDI0-	2	MDI[0]-	
PHY_AVDD10	3	AVDD10	
MDI1+	4	MDI[1]+	
MDI1-	5	MDI[1]-	
PHY_AVDD33	6	AVDD33	
MDI2+	7	MDI[2]+	
MDI2-	8	MDI[2]-	
PHY_AVDD10	9	AVDD10-0	
MDI3+	10	MDI[3]+	
MDI3-	11	MDI[3]-	
TXER	12	NC	

36	PHY_VDD10_CRS	DVDD10-0	
35	LED1_AD1	LED1/PHYAD1	
34	LED0_AD0	LED0/PHYAD0	
33	PME	PME	
32	CLK125/LED2_RXDLY	CLK125/LED2_RXDLY	
31	MDIO	MDIO	
30	MDC	MDC	
29	PHYRSTB	PHYRSTB	
28	PHY_VDD10	DVDD10	
27	TX_CTL	TXCTL	
26	TXD3	TXD3	
25	TXD2	TXD2	

49		PGND	
48	REGOUT	REGOUT	
47	RSET/CLK125	GND	
46	VDDREG	RSET/CLK125	
45	VDDREG	VDDREG	
44	VDDREG	VDDREG	
43	XTAL2	CKXTAL2	
42	XTAL1	CKXTAL1	
41	AVDD33_CEN	AVDD33-1	
40	PHY_AVDD10	AVDD10-1	
39	ENREGRSET	ENREG/RSET	
38	LED2_RXDLY	DVDD33-1	
37	ENREG		

14	RX_CTL_PHYAD2	RXCTL/PHYAD2	
15	RXD0/SELRGV	RXD0/SELRGV	
16	VDD33_VDD25	DVDD33	
17	RXD1/TXDLY	RXD1/TXDLY	
18	RXD2/AN0	RXD2/AN0	
19	RXD3/AN1	RXD3/AN1	
20	RX_CLK	RXC	
21	INT	INT	
22	VDD33_VDD25	DVDD33-0	
23	TX_CLK	TXC	
24	TXD0	TXD0	
	TXD1	TXD1	

RX_CTL_PHYAD2 RXD0/SELRGV VDD33_VDD25 RXD1/TXDLY RXD2/AN0 RXD3/AN1 RX_CLK INT VDD33_VDD25 TX_CLK TXD0 TXD1

RGMII/RMII

11 MDI3- / 11 MDI3+ ↔ MDI3- / MDI3+
11 MDI2- / 11 MDI2+ ↔ MDI2- / MDI2+
11 MDI1- / 11 MDI1+ ↔ MDI1- / MDI1+
11 MDI0- / 11 MDI0+ ↔ MDI0- / MDI0+

R35,36,37 Only for RTL8201FN/EN

PHY_VDD10_CRS	GR35	0R	CRS_N	CRS_N
LED2_RXDLY_ENREG	GR36	NC/0R	COL_N	COL_N
ENSWREG	GR37	0R	RXER_N	RXER_N

Place filter network close to RX_CLK.
Reserved for EMI

RX_CLK — GR49 22R RX_CLK_N — GC46 NC

RX_CTL_N
RX_CLK_N

RXD0_N
RXD1_N
RXD2_N
RXD3_N

RX_CTL_PHYAD2	GR48	22R	RX_CTL_N
RXD0/SELRGV	GR50	22R	RXD0_N
RXD1/TXDLY	GR51	22R	RXD1_N
RXD2/AN0	GR52	22R	RXD2_N
RXD3/AN1	GR53	22R	RXD3_N

TX_CLK
TX_CTL
TXER
TXD0
TXD1
TXD2
TXD3

Close to PHY
Reserve for EMI

RSET

RSET — GR6 2.49K(1%)

Others

VDDREG
PHY_VDD10
PHY_AVDD10
REGOUT
PHY_VDD33

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