Index

Note

NOTE 1:
Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted
3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

NOTE 2:
Please use our recommended components to avoid too many changes.For more informations about the second source,please refer to our AVL.

Note

Option

Description

Remind

Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

PINE64	PINE64		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**01.Index**		
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Version	Date	Author	Change List	Approved
V1.0	*20181025*		*First edition for RK1808 ddr4*	*RZF*
V2.0	20190919		SOEdge Schematic Released	

PINE64	**PINE64**
Project:	SOEdge Schematic 20190919 ver 2.0
File:	**02.Revision History**
Date:	Thursday, September 19, 2019
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I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	I2C0_SCL/GPIO0_B0_u I2C0_SDA/GPIO0_B1_u	PMUIO2	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC_3V3	Rockchip RK809	0x20	PMIC	100kHz,400kHz
					SY837		BUCK	100kHz,400kHz
I2C1	I2C1_SCL/GPIO0_C0_u I2C1_SDA/GPIO0_C1_u	PMUIO2	I2C1_SCL I2C1_SDA	VCC_3V3	GSL1680		Touch IC	100kHz,400kHz
								100kHz,400kHz
I2C2	I2C1_SCL/GPIO1_B4_U I2C1_SDA/GPIO1_B5_U	VCCIO_3V3			NC			100kHz,400kHz
I2C3	GPIO2_D0/I2C3_SCL_U GPIO2_D1/I2C3_SDA_U	VCCA_1V8		VCCA_1V8	MIPI CAMERA			
					CIF CAMERA			
					BT1120			
I2C4	GPIO3_C2/I2C4_SCL_U GPIO3_C3/I2C4_SDA_U	VCCIO_3V3		VCCIO_3V3	DIGITAL MIC			
					RGB LCD			
					PCIEX4			
					SENSOR			

	PINE64
Project:	SOEdge Schematic 20190919 ver 2.0
File:	**04.I2C MAP**
Date:	Thursday, September 19, 2019
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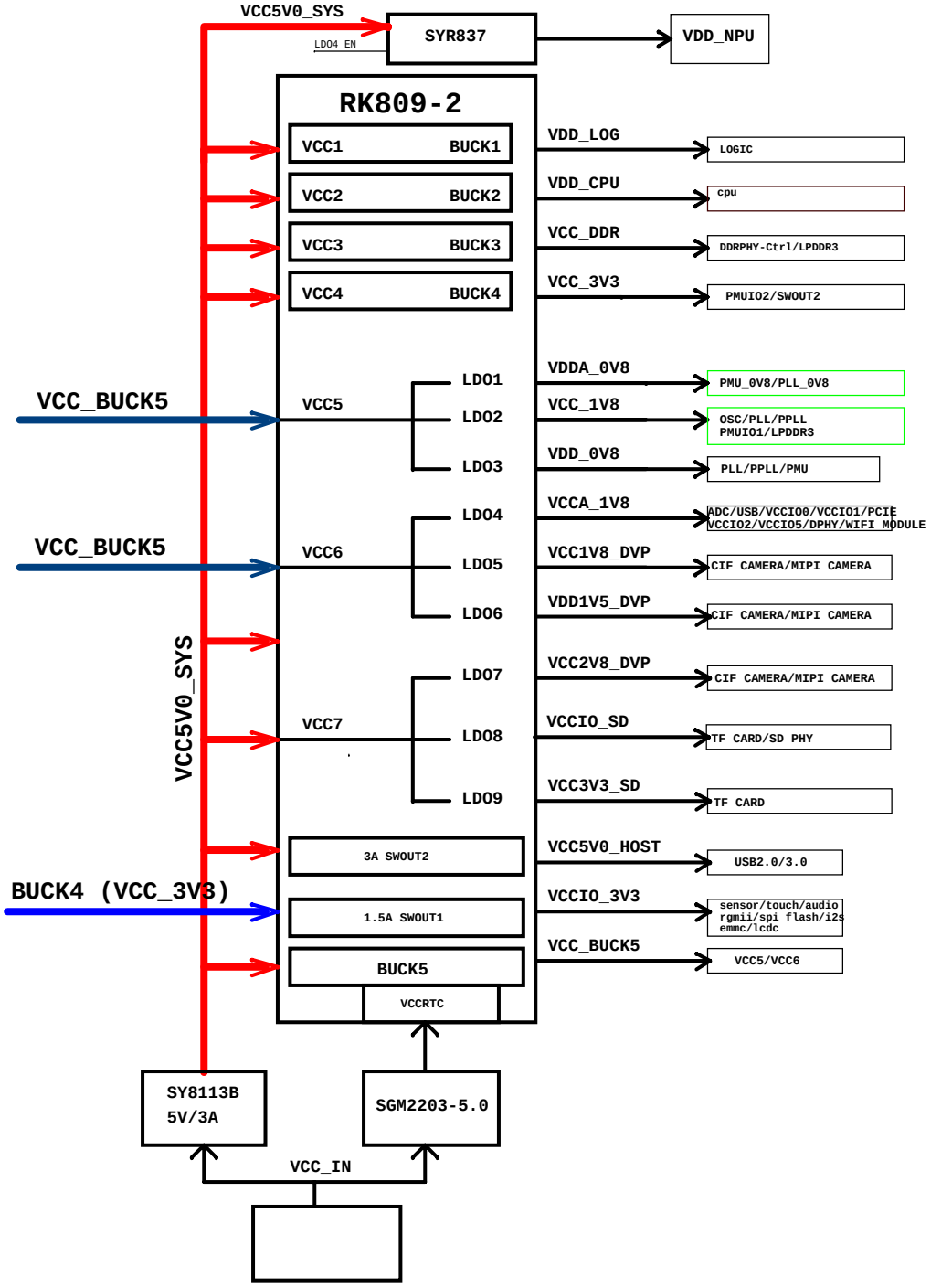
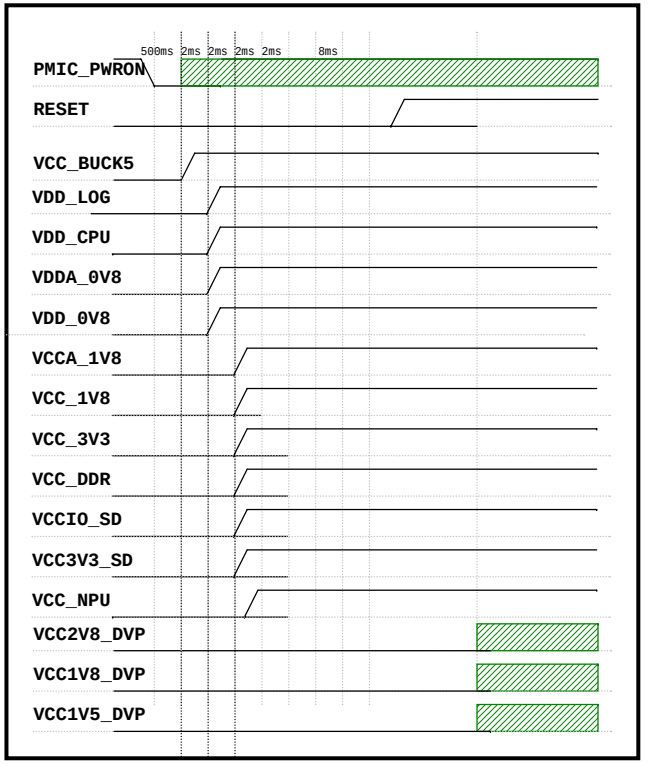
POWER DIAGRAM



RK809-2 Power-on Sequence

PowerName	PMIC Channel	Time Slot (step 2mS)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current
VDD_NPU	EXTERNAL(SY837)	Slot:3A	1V	6A	ON	OFF	4A
VDD_LOG	BUCK1	Slot:2	0.85V	2.5A	ON	OFF	1.25A
VDD_CPU	BUCK2	Slot:2	0.85V	2.5A	ON	OFF	750mA
VCC_DDR	BUCK3	Slot:3	FB=0.6V	1.5A	ON	ON	
VCC_3V3	BUCK4	Slot:4	3.3V	1.5A	ON	ON	
VCC_BUCK5	BUCK5	Slot:1	2.5V	2.5A	ON	ON	
VDDA_0V8	LDO1	Slot:2	0.8V	400mA	ON	OFF	
VCC_1V8	LDO2	Slot:3	1.8V	400mA	ON	ON	
VDD_0V8	LDO3	Slot:2	0.8V	100mA	ON	ON	
VCCA_1V8	LDO4	Slot:3	1.8V	400mA	ON	OFF	
VCC1V8_DVP	LDO5		1.8V	400mA	OFF	OFF	
VDD1V5_DVP	LDO6		1.5V	400mA	OFF	OFF	
VCC2V8_DVP	LDO7		2.8V	400mA	OFF	OFF	
VCCIO_SD	LDO8	Slot:4	3.3V	400mA	ON	OFF	
VCC3V3_SD	LDO9	Slot:4	3.3V	400mA	ON	OFF	
VCCIO_3V3	SWOUT2	Slot:4	3.3V	3A	ON	OFF	
VCC5V0_HOST	SWOUT1		5V	1.5A	OFF	OFF	
RESET	RESETB	Slot:10	OD				



PINE64	PINE64
Project:	SOEdge Schematic 20190919 ver 2.0
File:	05.Power diagram and Sequence
Date:	Thursday, September 19, 2019
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Designed by:	Rzf
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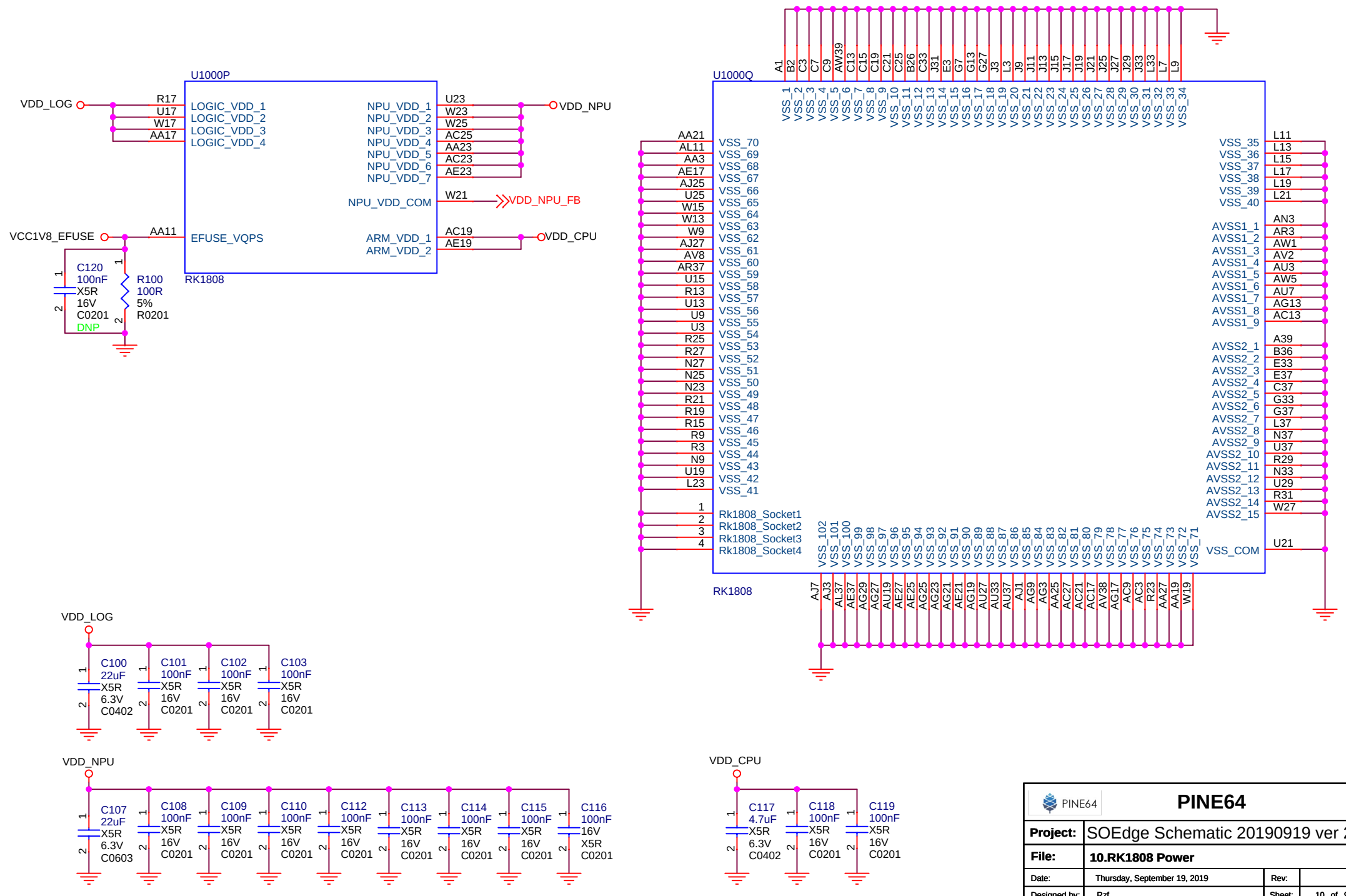
RK1808 Power



PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**10.RK1808 Power**		
Date:	Thursday, September 19, 2019	Rev:	
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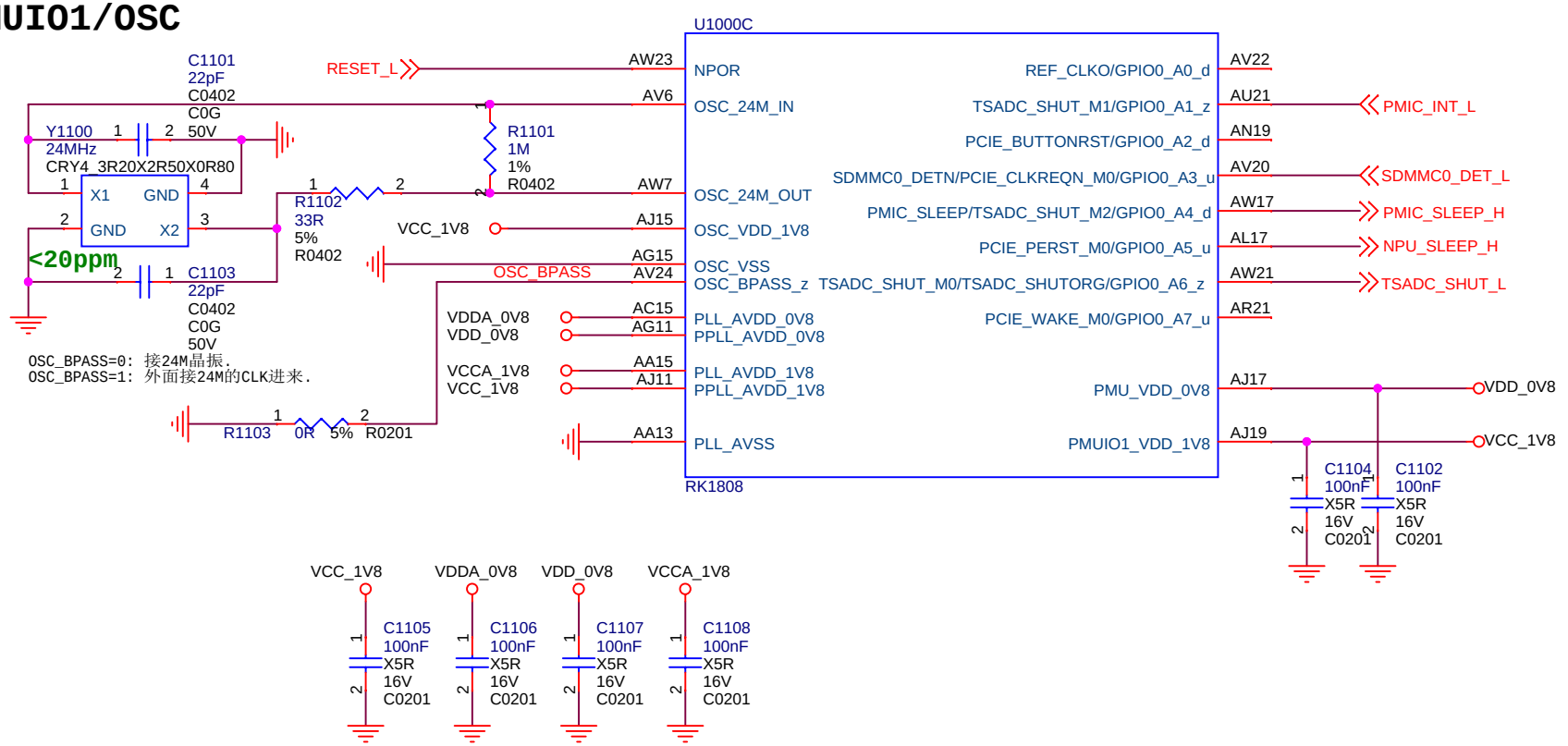
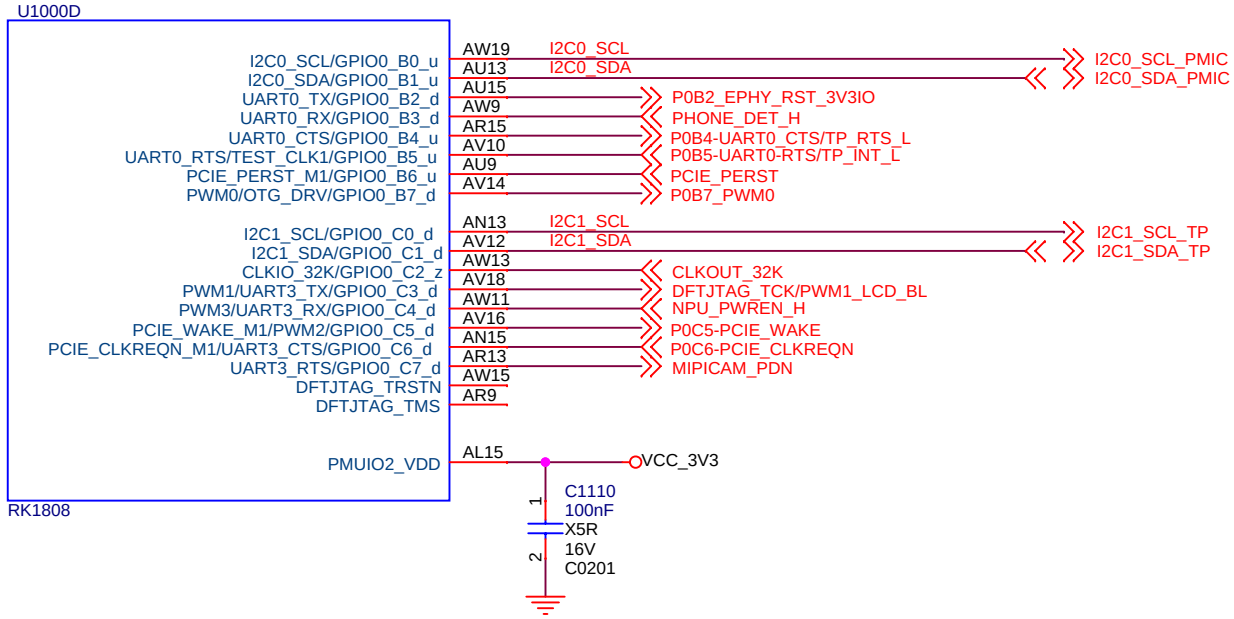
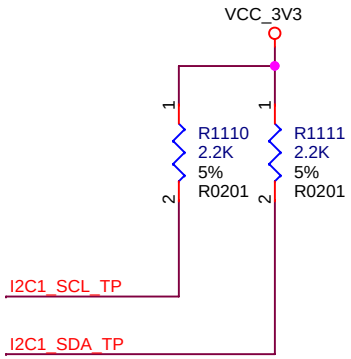
PMUIO1/OSC



PMUIO2





PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**11.RK1808 OSC/PMUIO1/PMUIO2**		
Date:	Thursday, September 19, 2019	Rev:	
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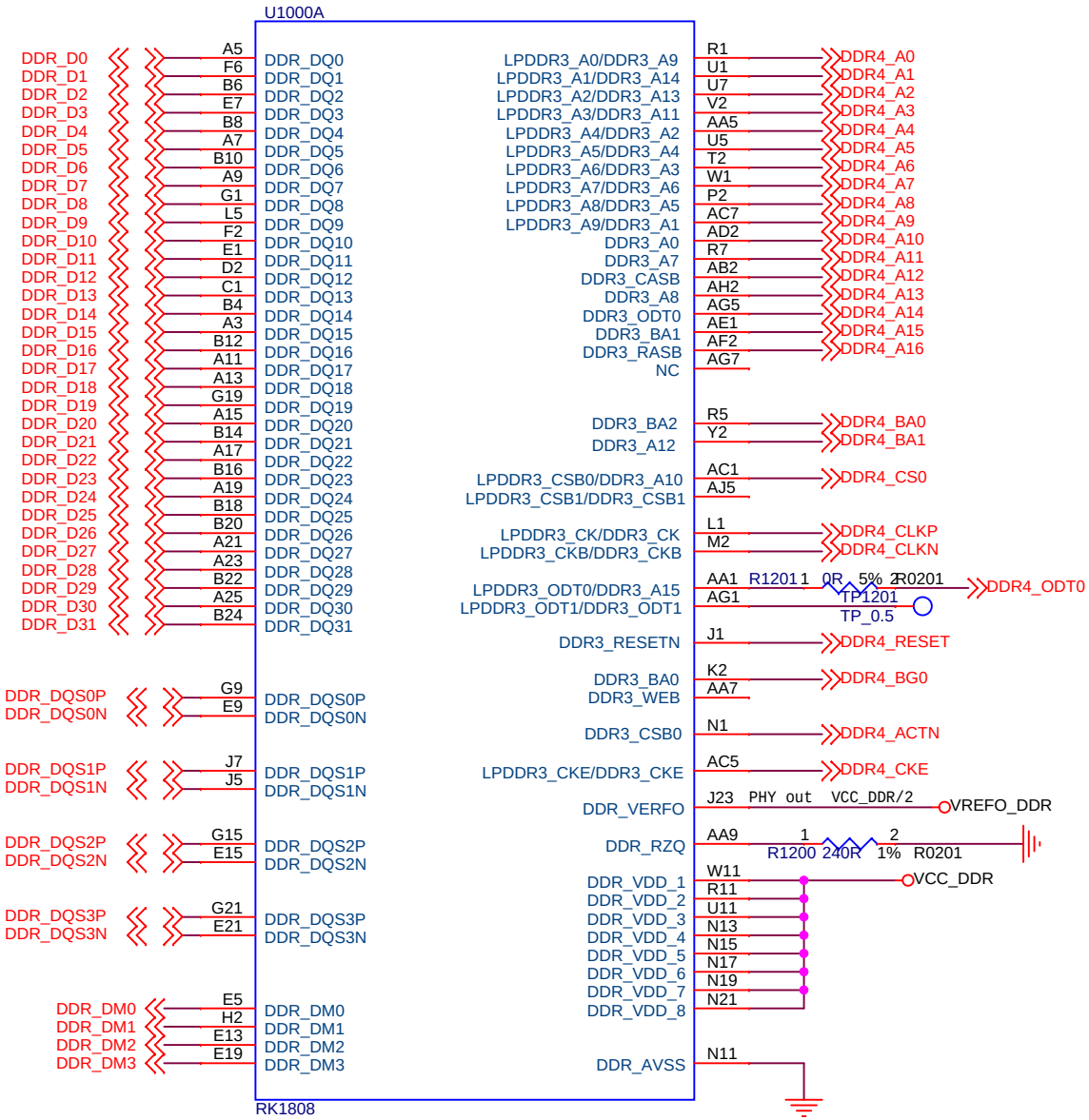
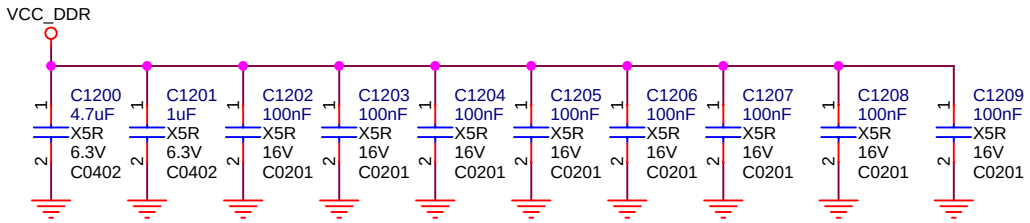
DDR Controller



LPDDR3/LPDDR2	DDR3
A0	A9
A1	A14
A2	A13
A3	A11
A4	A2
A5	A4
A6	A3
A7	A6
A8	A5
A9	A1
	A0
	A7
	CASB
	A8
	ODT0
	BA1
	RASB
	CSB0
	BA2
	A12
	BA0
	WEB
CK	CK
CKB	CKB
CKE	CKE
CSB0	A10
CSB1	CSB1
ODT0	A15
ODT1	ODT1
	RESETN



PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**12.RK1808 DDR Controller**		
Date:	Thursday, September 19, 2019	Rev:	
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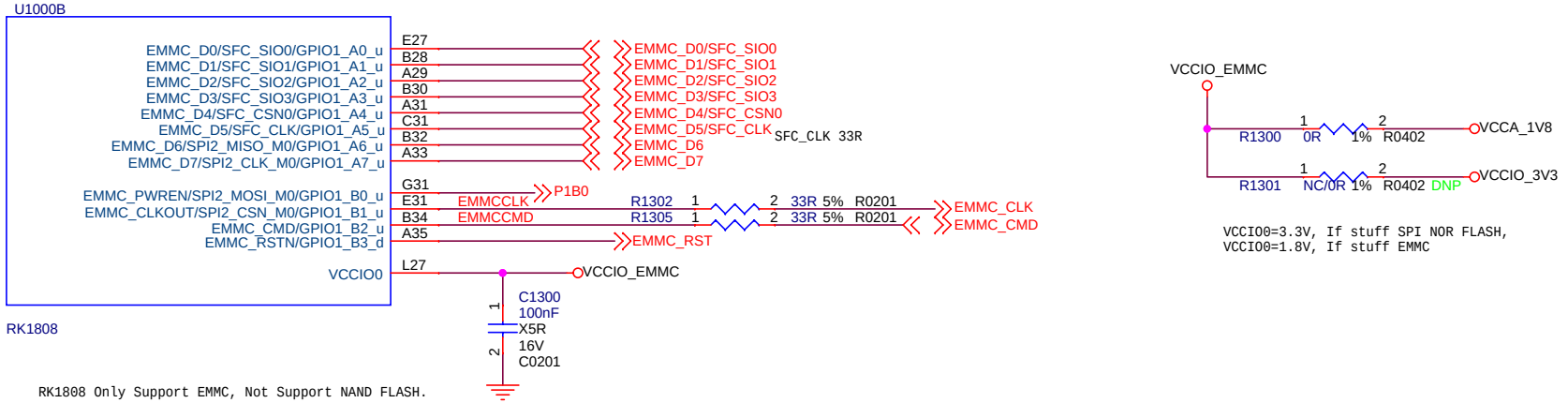
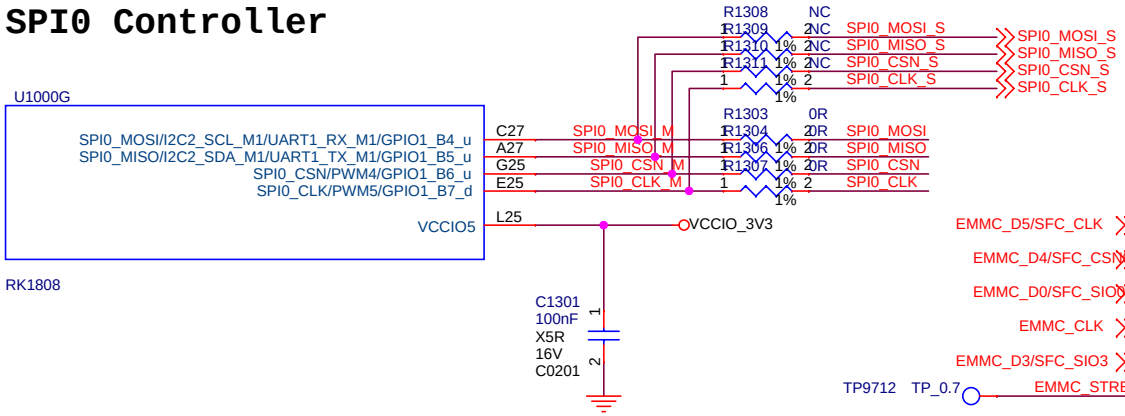
EMMC/SFC Controller

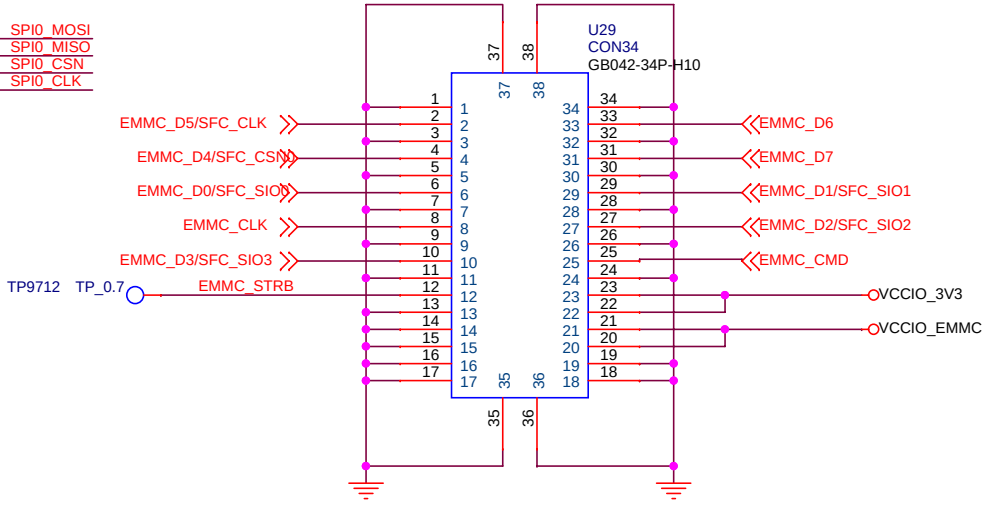


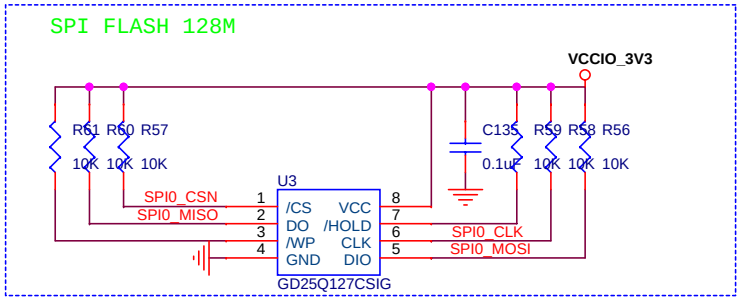
RK1808 Only Support EMMC, Not Support NAND FLASH.

VCCIO0=3.3V, If stuff SPI NOR FLASH,
VCCIO0=1.8V, If stuff EMMC

SPI0 Controller

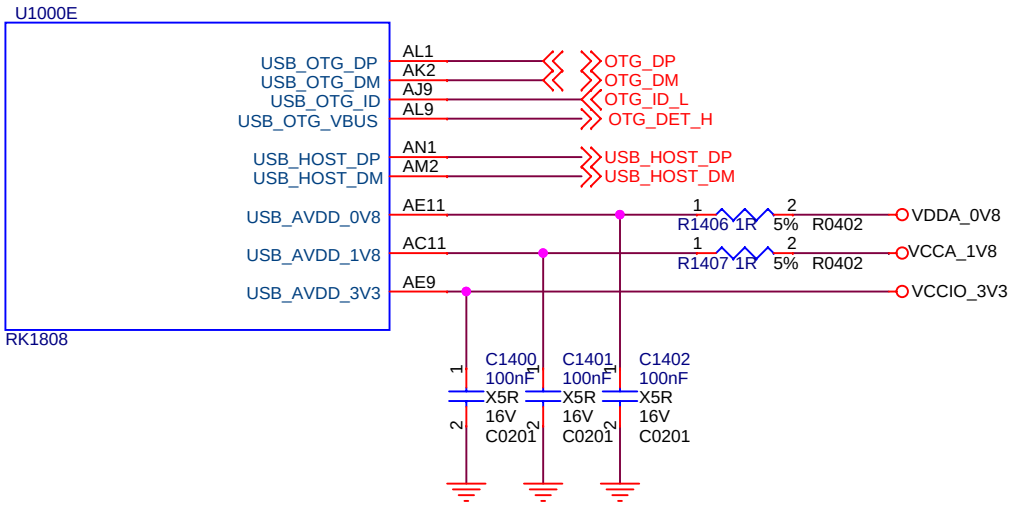




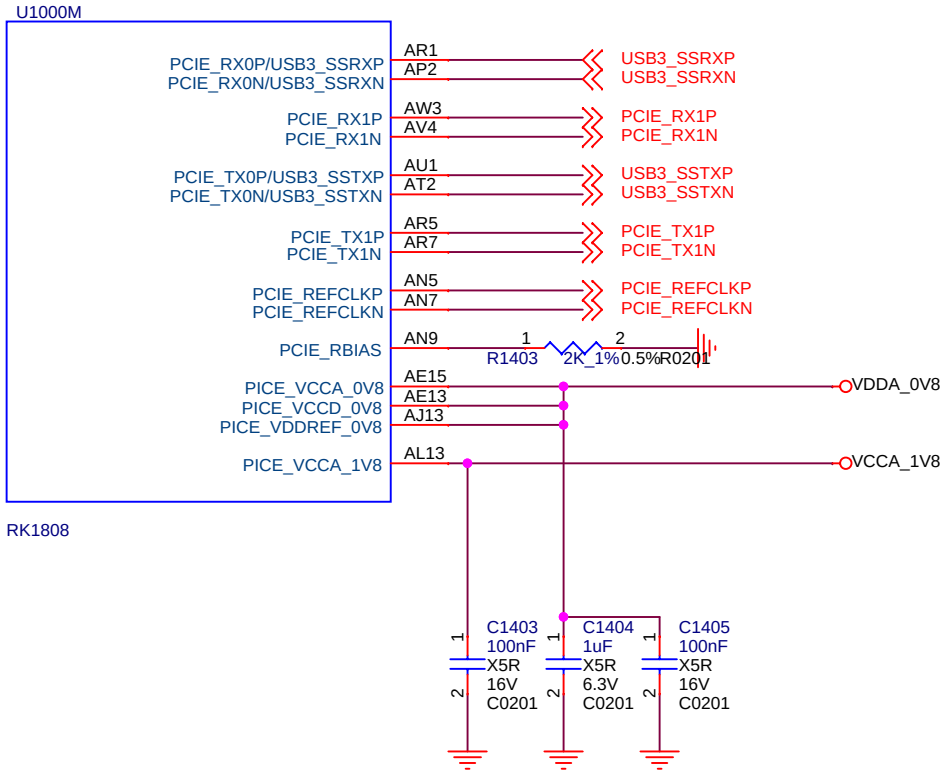


PINE64	PINE64		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	13.RK1808 EMMC /SPI Controller		
Date:	Thursday, September 19, 2019	Rev:	
Designed by:	Rzf	Sheet:	13 of 99

USB Controller



PCIE Controller



PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**14.RK1808 USB/PCIE Controller**		
Date:	Thursday, September 19, 2019	Rev:	
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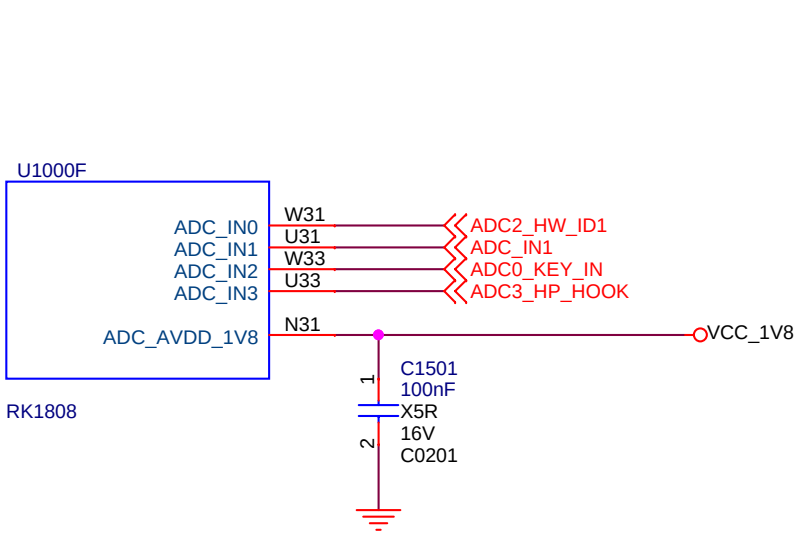
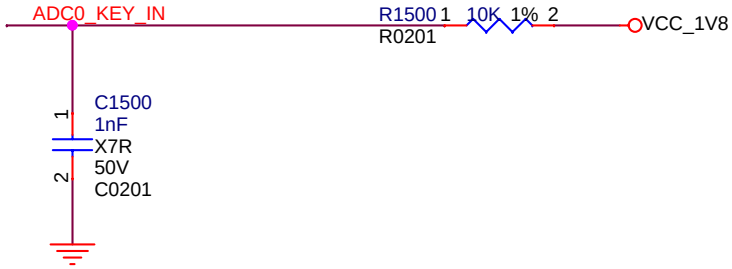
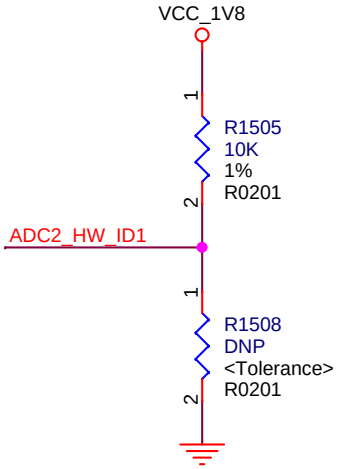
SARADC/KEY



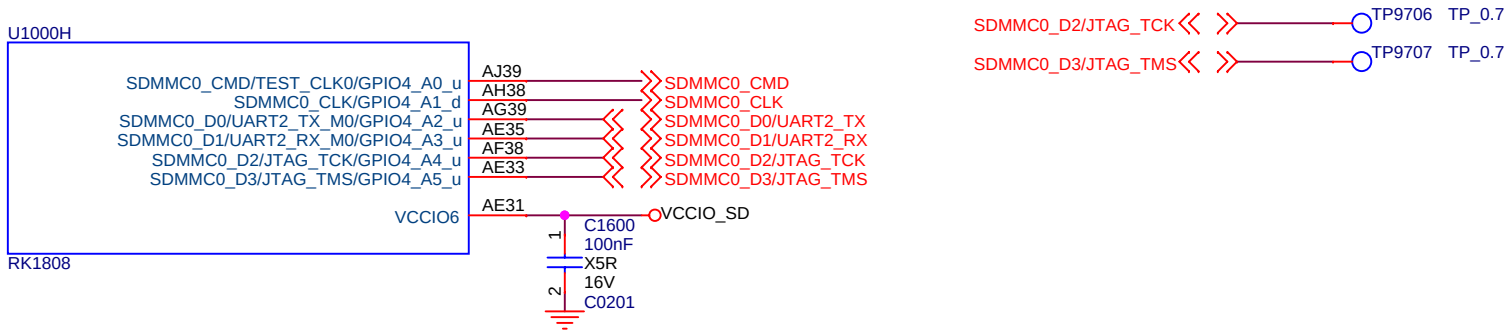


Key Name	SARADC
VOL+/RECOVERY	10
VOL-	170

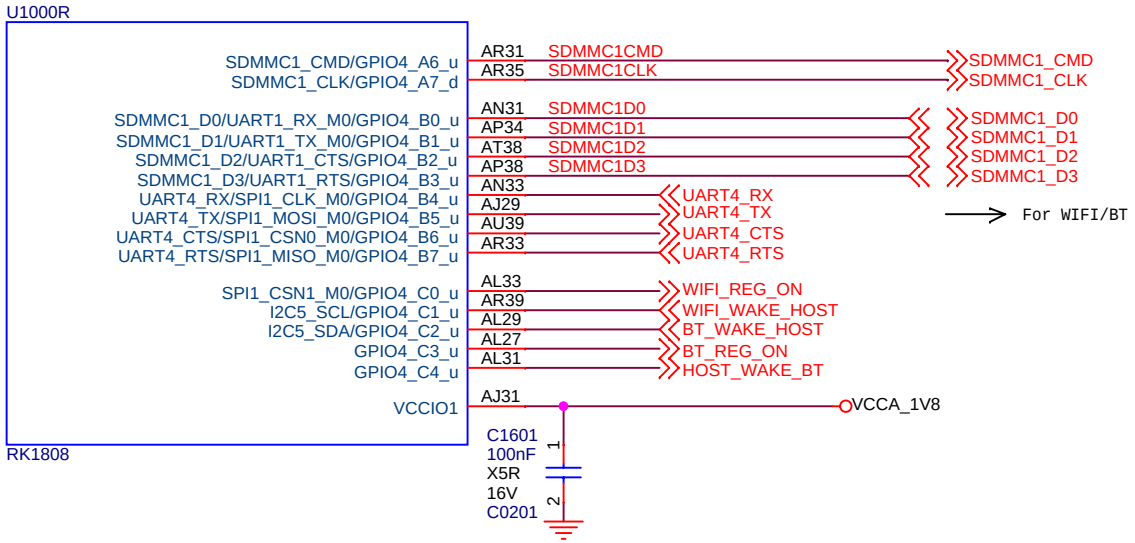


PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**15.RK1808 SARADC/KEY**		
Date:	Thursday, September 19, 2019	Rev:	
Designed by:	Rzf	Sheet:	15 of 99

SDMMC0 Controller



SDMMC1 Controller



PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**16.RK1808 SDMMC0/SDMMC1**		
Date:	Thursday, September 19, 2019	Rev:	
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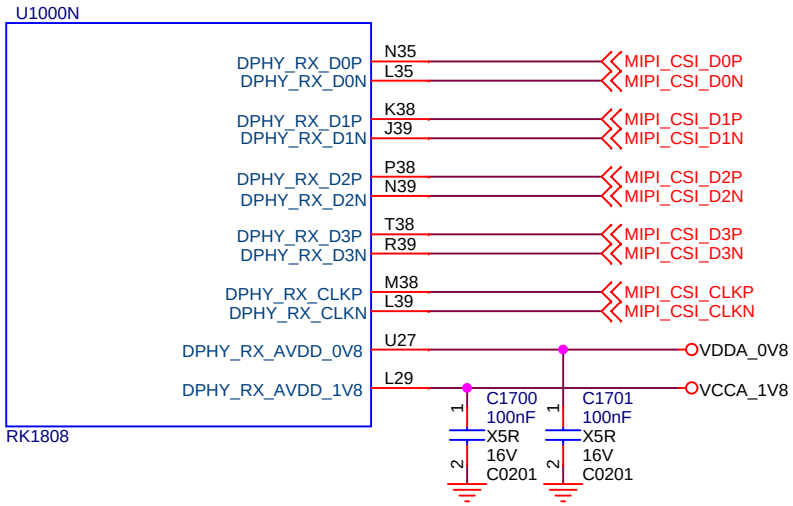
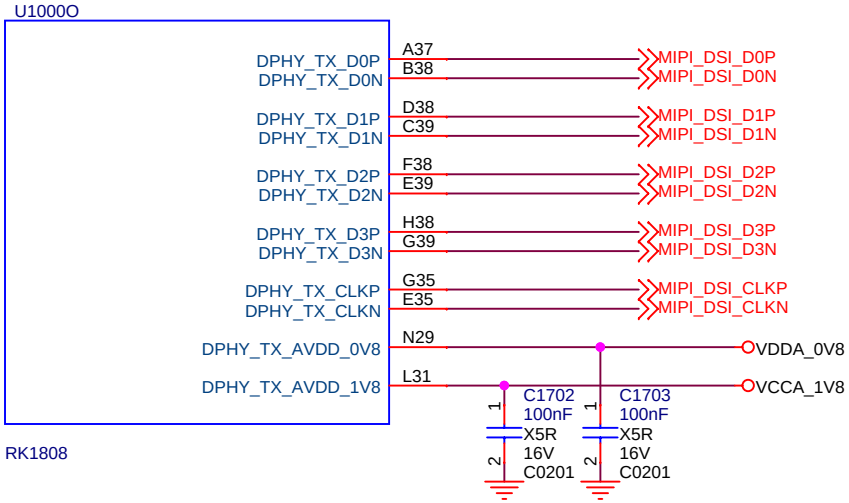
MIPI CSI Controller



MIPI DSI Controller



PINE64	PINE64		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**17.RK1808 MIPI DSI/CSI**		
Date:	Thursday, September 19, 2019	Rev:	
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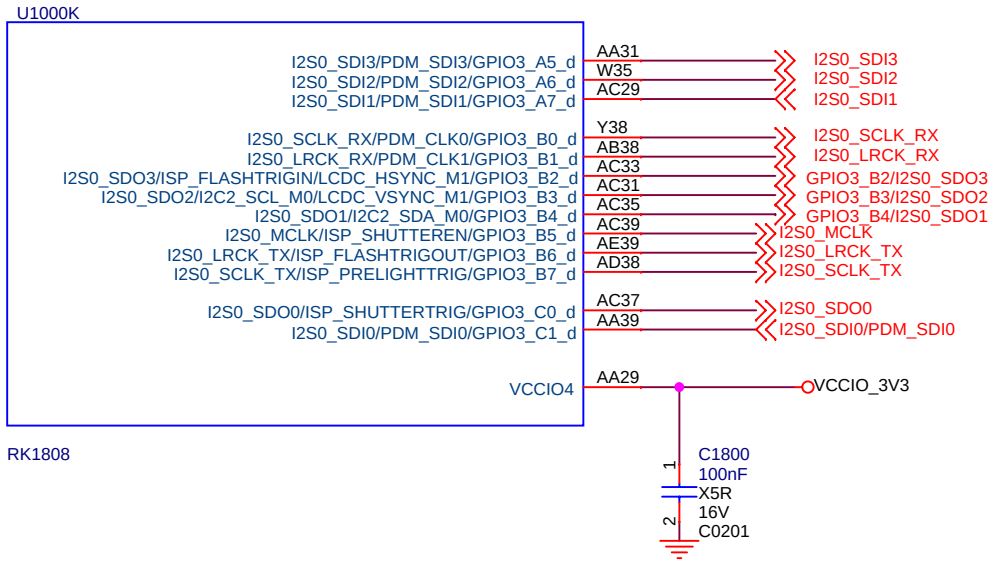
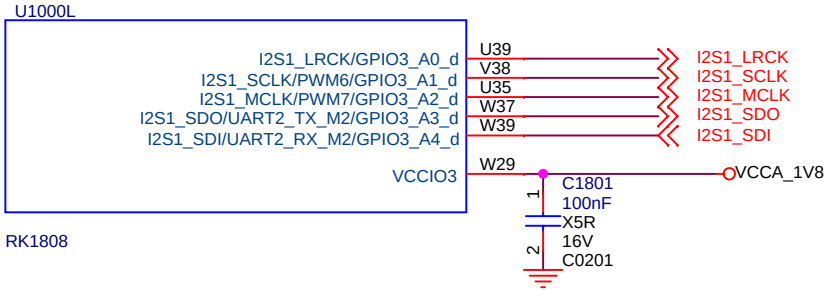
I2S0 Controller



I2S1 Controller



For Codec

PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**18.RK1808 I2S0/I2S1**		
Date:	Thursday, September 19, 2019	Rev:	
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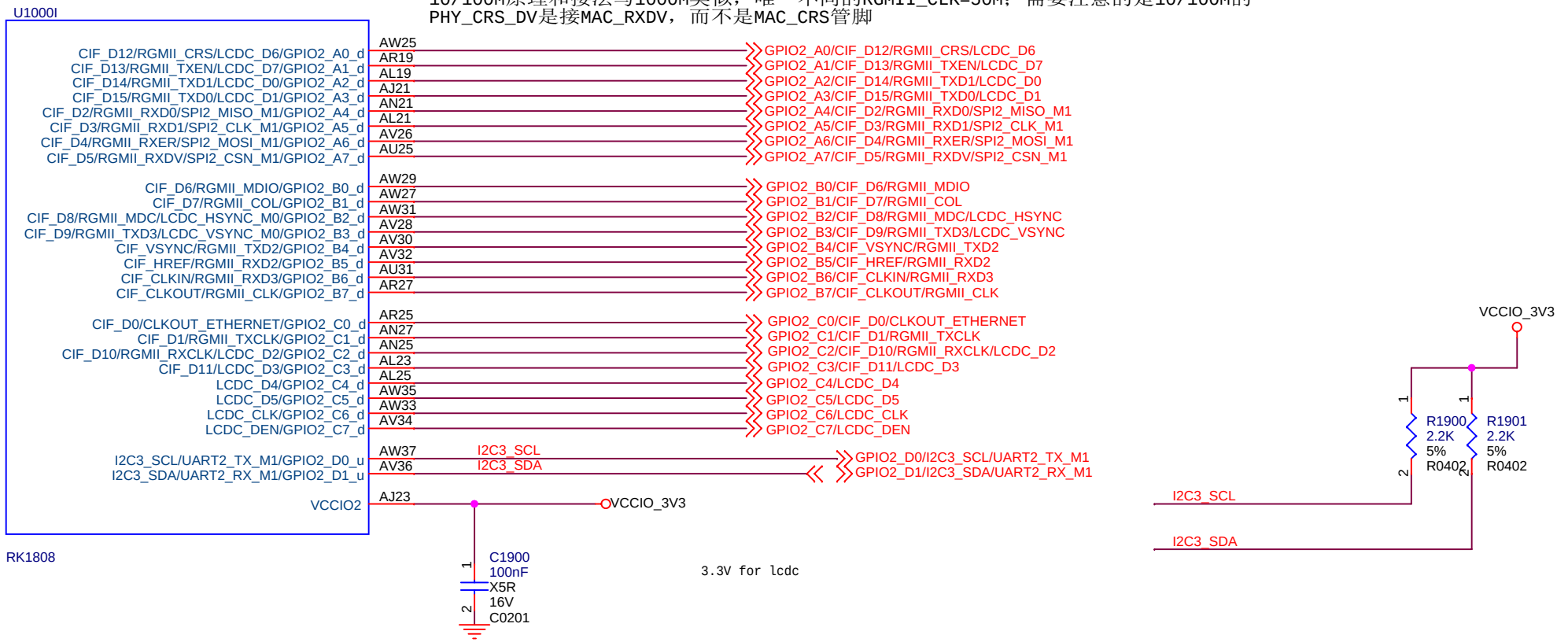
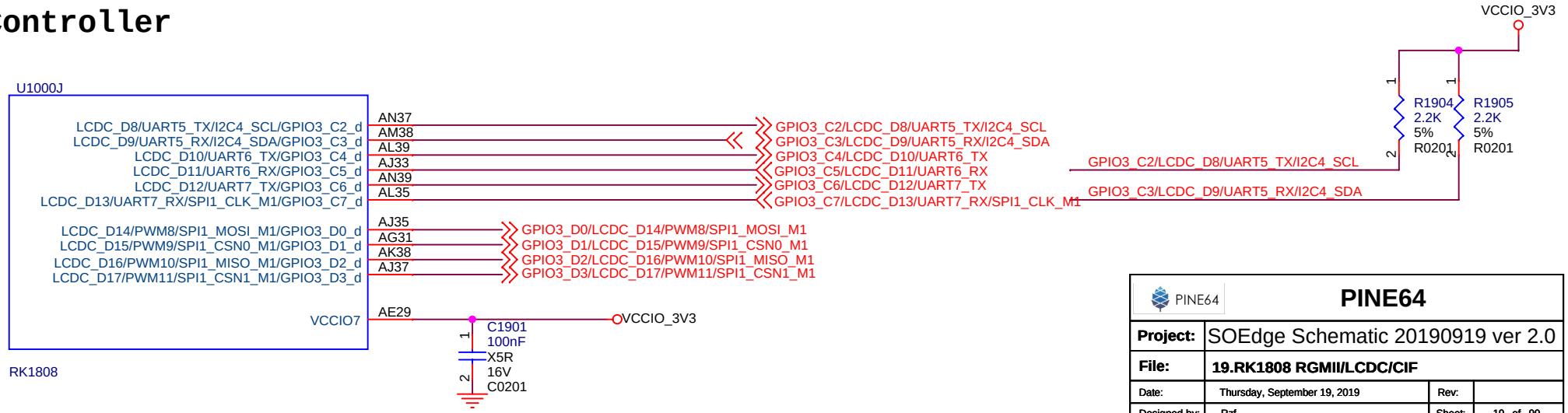
CIF/RGMII/LCDC Controller

10/100M原理和接法与1000M类似，唯一不同的RGMII_CLK=50M；需要注意的是10/100M的PHY_CRS_DV是接MAC_RXDV，而不是MAC_CRS管脚

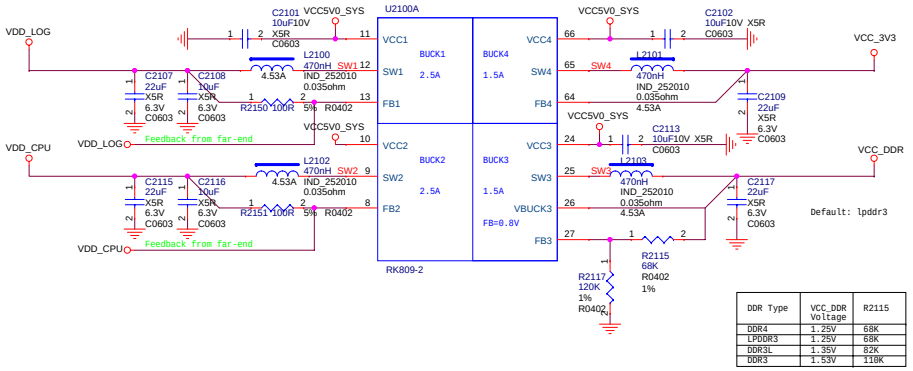


LCDC Controller



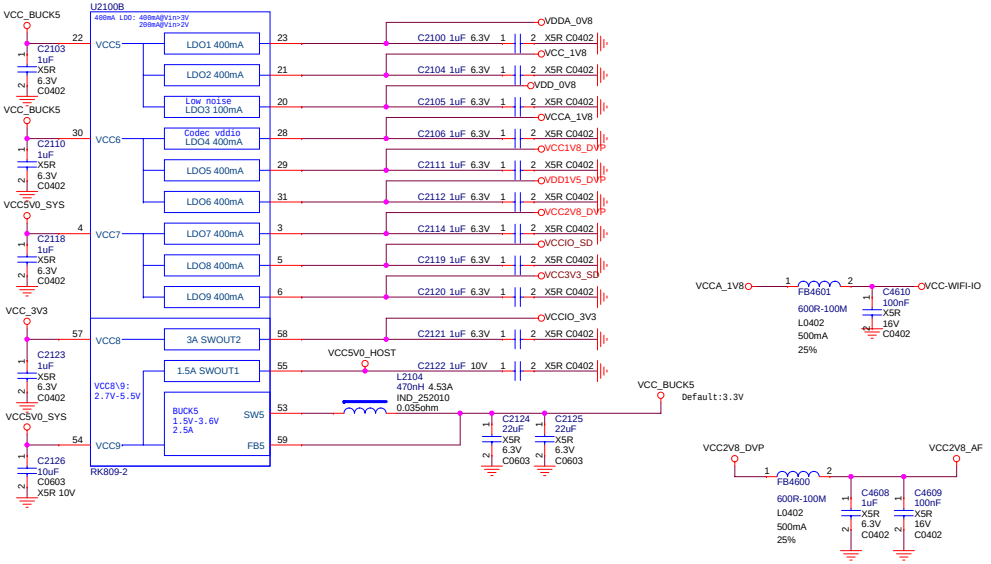
PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**19.RK1808 RGMII/LCDC/CIF**		
Date:	Thursday, September 19, 2019	Rev:	
Designed by:	Rzf	Sheet:	19 of 99

PMIC RK809-1 DCDC

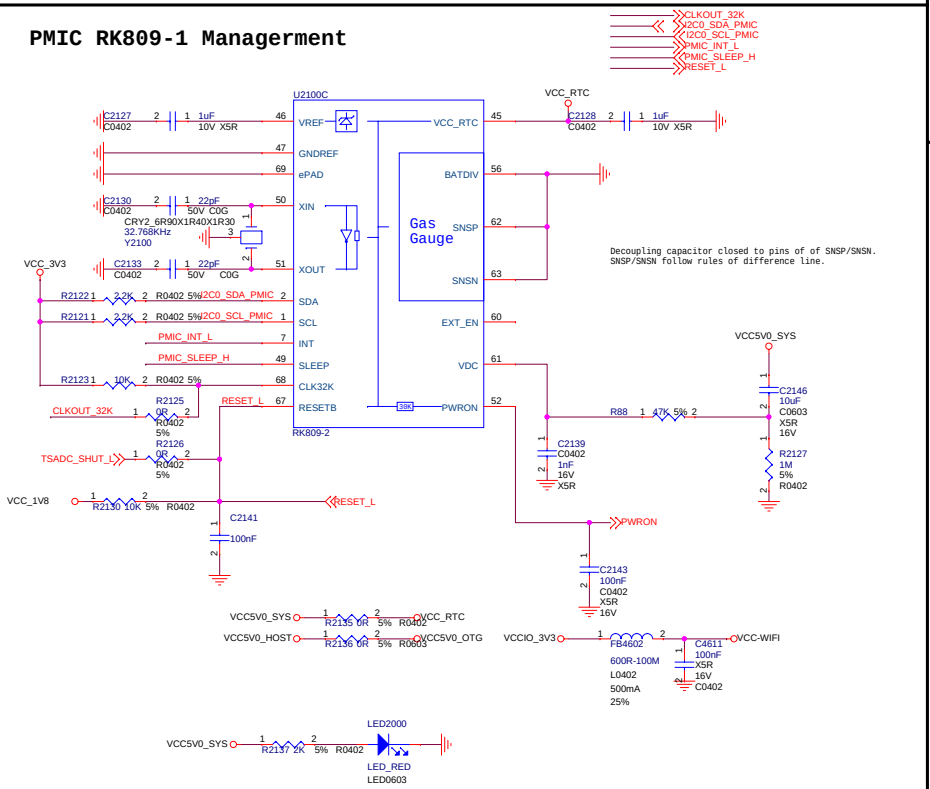


DDR Type	VCC_DDR Voltage	R2115
DDR4	1.25V	68K
LPDDR3	1.25V	68K
DDR3L	1.35V	82K
DDR3	1.53V	110K

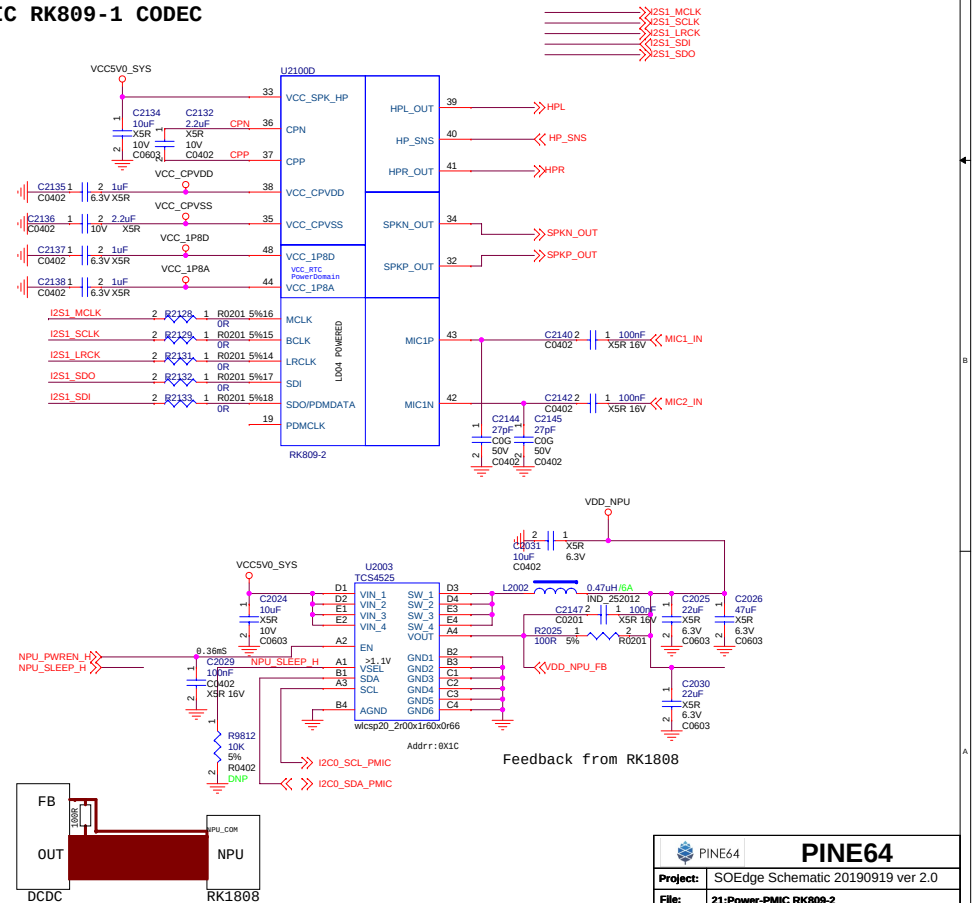
PMIC RK809-1 LDO



PMIC RK809-1 Managerment



PMIC RK809-1 CODEC



PINE64	**PINE64**
Project:	SOEdge Schematic 20190919 ver 2.0
File:	21:Power-PMIC RK809-2
Date:	Thursday, September 19, 2019
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Designed by:	Rzf
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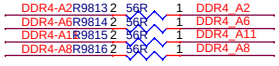
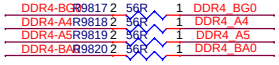
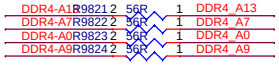
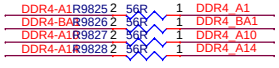
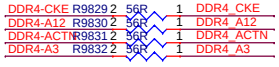
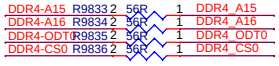




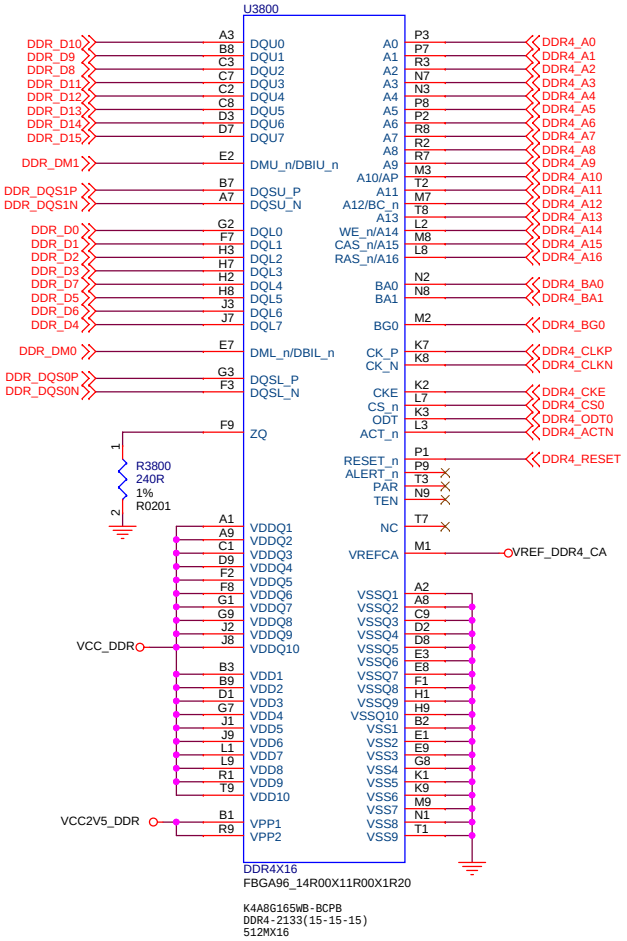








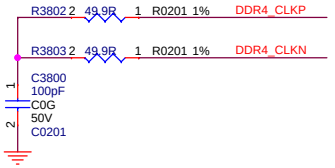
For Daisy Chain Scheduling

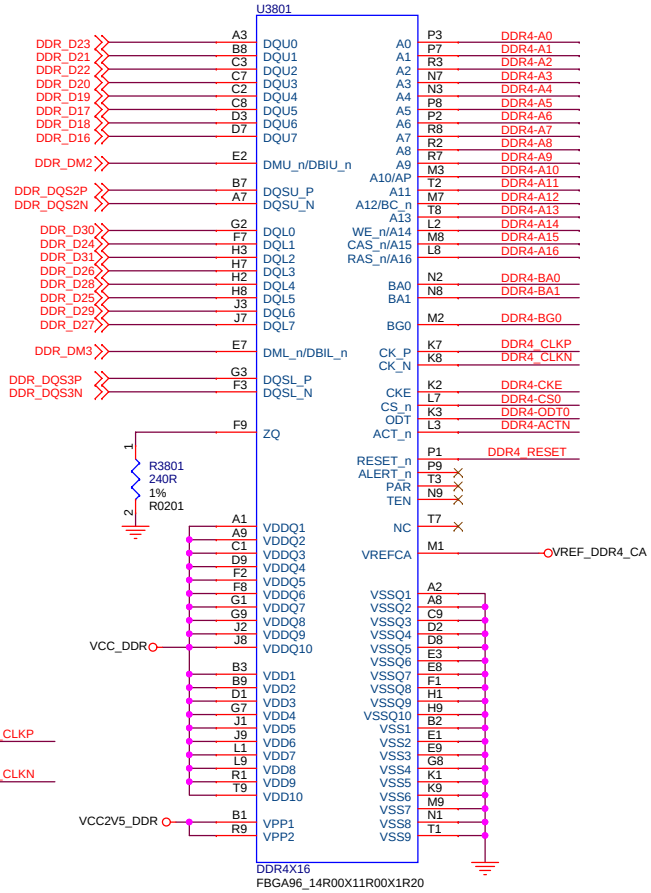


Date can be switched in group.

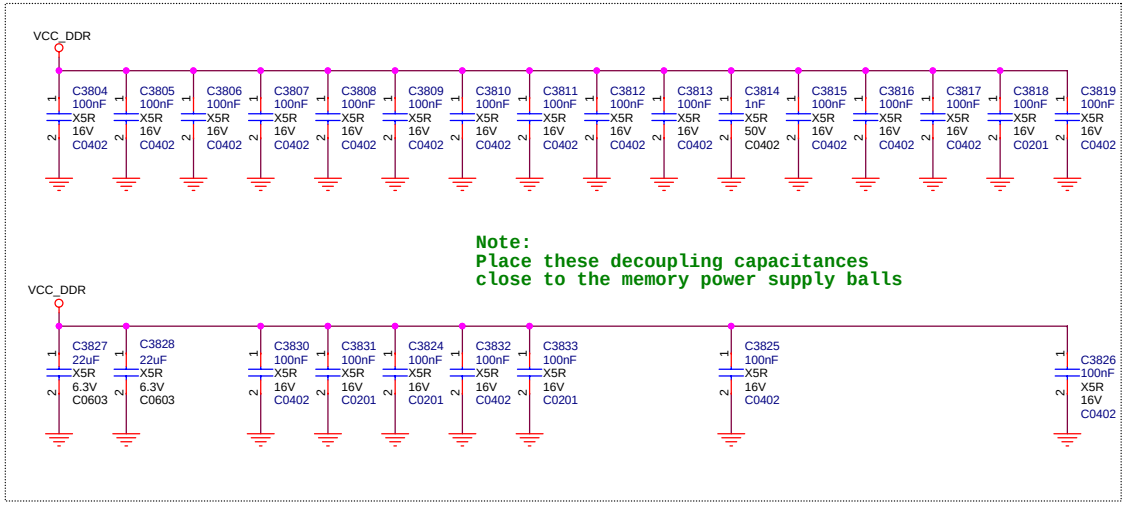
VDD(1.25V):Supply Voltage
VDDQ(1.25V):Supply Voltage for output
VPP(2.5V): Peak to Peak Voltage

VPP must be equal or greater than
VDD/VDDQ at all times.

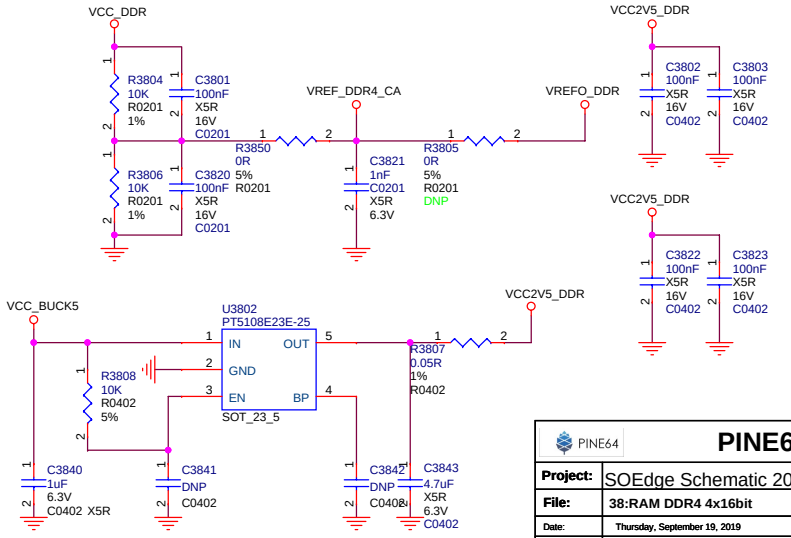




2X16bit DDR4



Remind: Refer to the latest AVL for parts selection.



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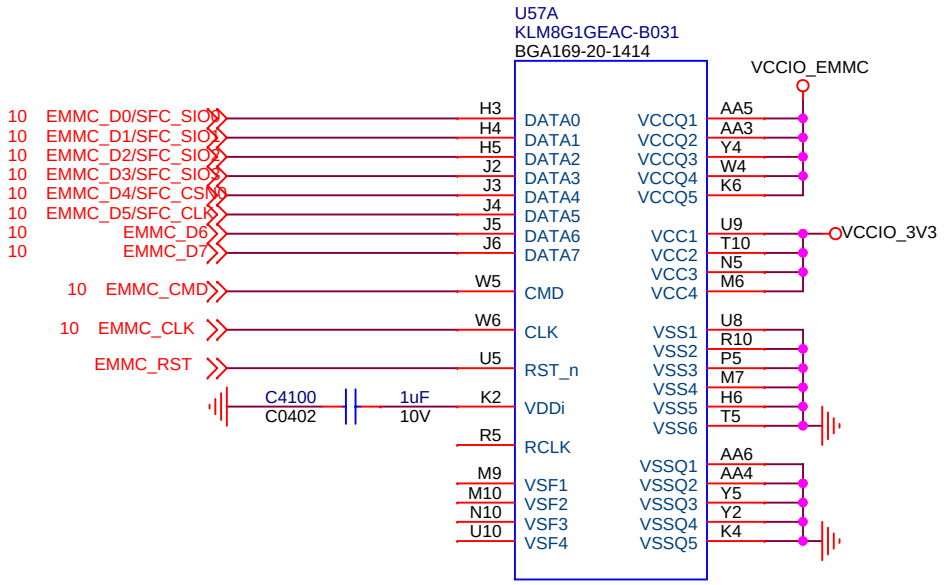
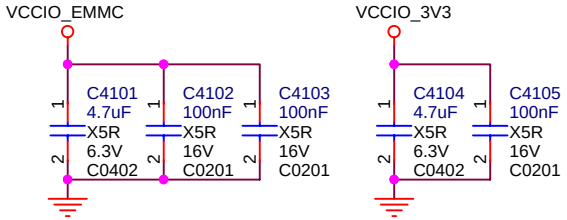
eMMC





Remind: Refer to the latest AVL for parts selection.

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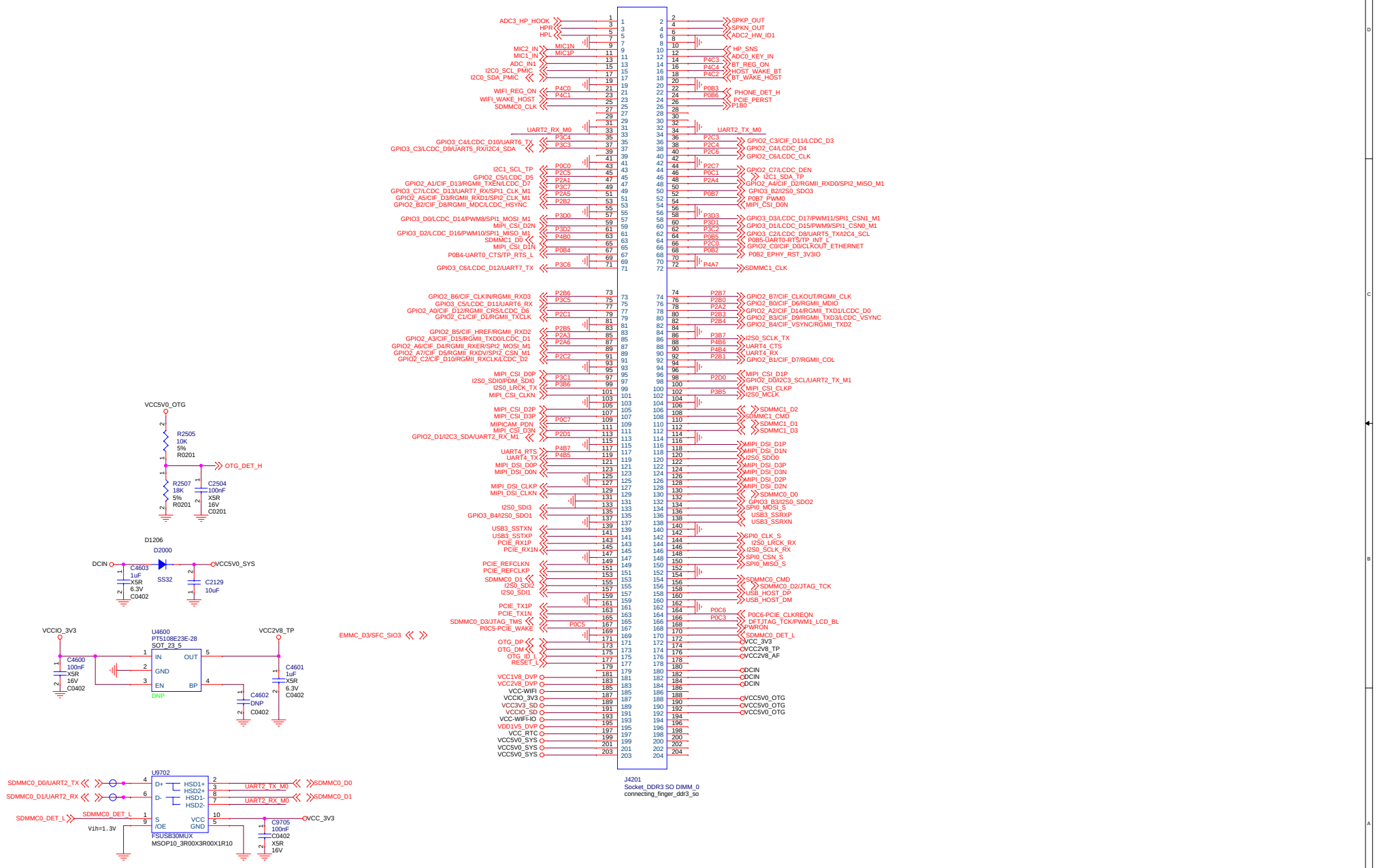

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Date: Thursday, September 19, 2019	Sheet 1 of 1		