

PineTab2 Tablet Schematic

PineTab2_REF_V2

Referenced Functions List

- 1) PMIC : RK817-5
- 2) RAM : LPDDR4/LPDDR4X 1x32Bit 200P
- 3) ROM --- eMMC5.1
- 4) Support --- Micro SD Card3.0
- 5) Support --- 1 x USB2.0 OTG + 1 x USB3.0 HOST + 2 x USB2.0 HOST
- 6) Support --- 1 x PCIe custom connector
- 7) Support : 4Lanes MIPI CSI Camera(5M) or 2Lane MIPI CSI Camera(2M)
- 8) Support : Digital Video TX
- 9) Support : 1 x MIPI DSI Panel with Touch Panel
- 10) Support : 1 x Dual MIPI DSI Panel
- 11) Support : a/b/g/n/ac 1x1 WIFI + BT
- 12) Support : Headphone output and Speaker out(1.3W@8ohm)
- 13) Support : Dual External Power Amplifier
- 14) Support : Gyroscope + Accelerometer + Motion + Hall + Ambient & Proximity
- 15) Support --- Array Key(MENU,VOL+,VOL-,ESC) + RESET KEY + PWRON KEY
- 16) Support --- SARADC
- 17) Support --- Debug UART


 PINE64		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	00.Cover_Page		
Date:	Tuesday, September 27, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	1 of 37

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Description

Note

Option

Notes


NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

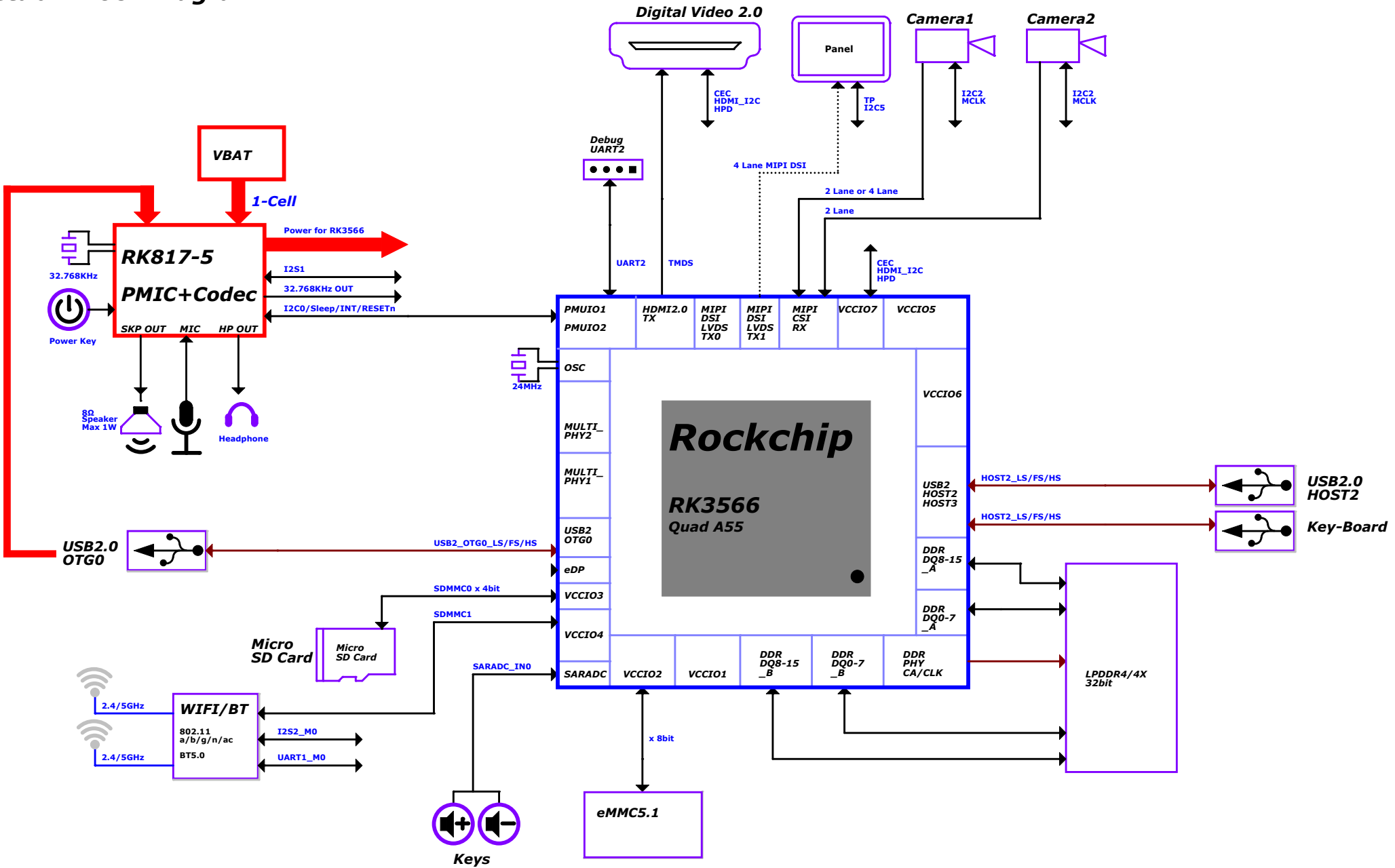
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Project:	PineTab2 Schematic-20230417		
File:	01.Index_and_Notes		
Date:	Tuesday, September 27, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	2 of 37

Revision History

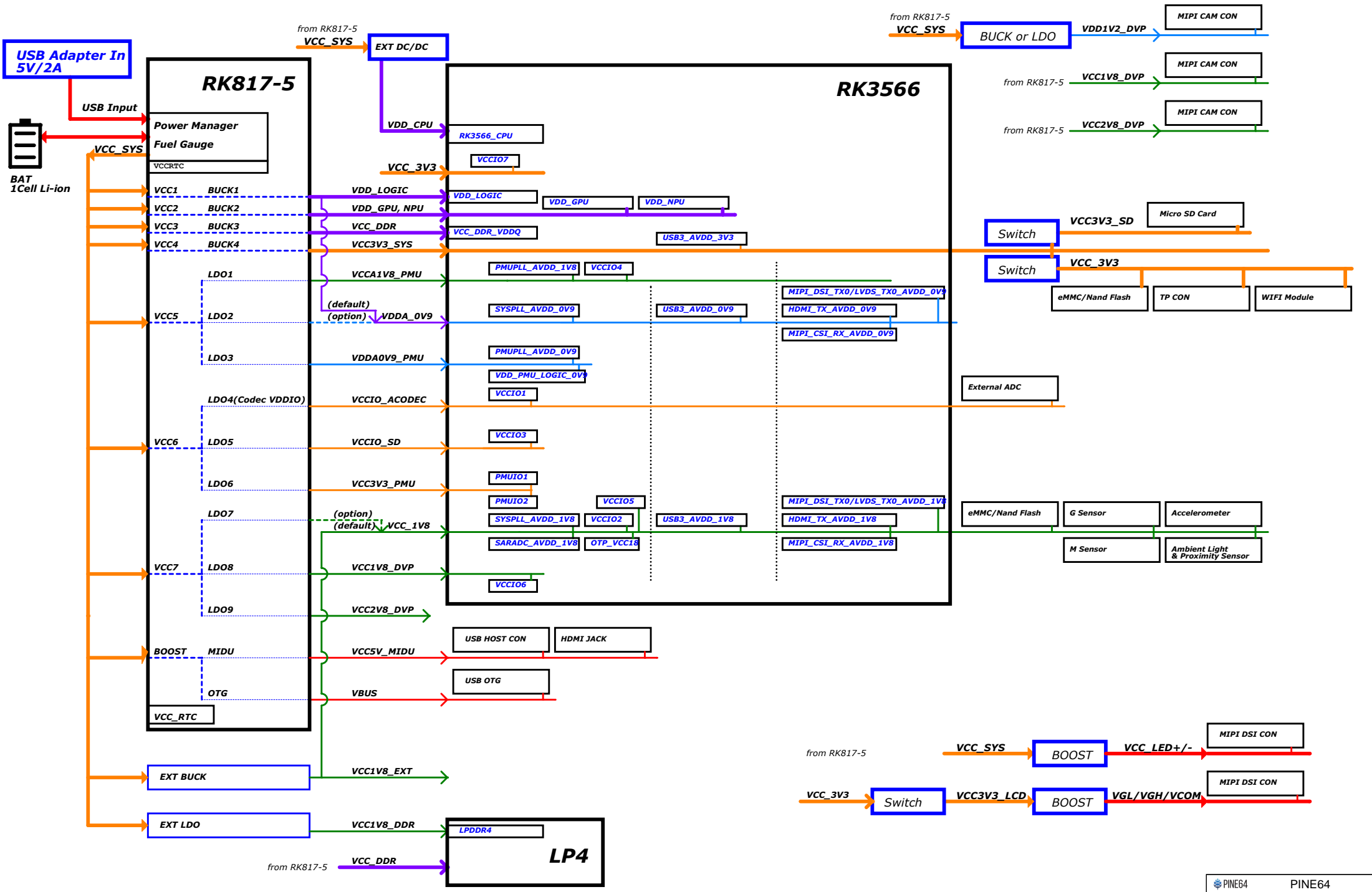
Version	Date	By	Change Description	Approved
V0.1	2022-0927	Xiexiaomin	1: 35页增加Pcie 2.0, FPC接口定义设计, 接扩展NVMe设备 2: 优化Type-C-UART插入识别, 增加与门电路硬件判断CC脚状态 UART信号接Type-C的SBU脚 3: 增加USB-C口24pin:USB 3.0, 为HOST功能 修改USB-C口为24pin:USB OTG功能, 5V输入, 集合UART串口, emmc disable功能 4: 36页增加SPI FLASH, 因GPIO1_C7与eMMC_RSTn复用, 故接为Standard SPI FLASH 5 WIFI更改为恒玄沉板与海华模块兼容设计	
V1.0	2023-0218	Xiexiaomin	1: 24页增加霍尔开关, 位号Q11 2: 28页恒玄WiFi芯片31脚改为RX, 30脚改为TX 3: 喇叭功率参数调整R160, R163更改为270K 4: 屏背光限流电阻参数更改为1.5R, 预留1.8V IO电压 5: 触摸芯片端的VCCIO需要上件2.2uF电容C315, 端pin13要追加电容C501 7: 调整USB 3.0定义, 位号USB2, 正面插支持3,,0, 反插2.0 8:增加PD诱电芯片CH224K, 位号U9014	
V2.0	2023-0417	Xiexiaomin	1:LCD0_RST_L_GPIO0_A6更改为LCD0_RST_L_GPIO0_C6 2:HALL_INT_L_GPIO0_C6更改为HALL_INT_L_GPIO0_A6 3:霍尔开关供电需要常开, 由VCC_3V3更改为VCC3V3_PMU 4:霍尔开关中断信号外部需要增加上拉电阻 5:USB 3.0定义非标Type-C口: 主控端的USB3_TX/RX分别接Type-C座子口的TX1与RX1即可 6:WIFI硬件原理版本更新, POWERON增加IO口控制, GPIO3_D3 6:WIFIid VBAT供电MOS开关使能增加三极管防漏电, 导通状态WIFI_PWREN由低电平更改为高电平	

 PINE64		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	02.Revision_History		
Date:	Monday, March 27, 2023	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
Sheet:	3 of 37		

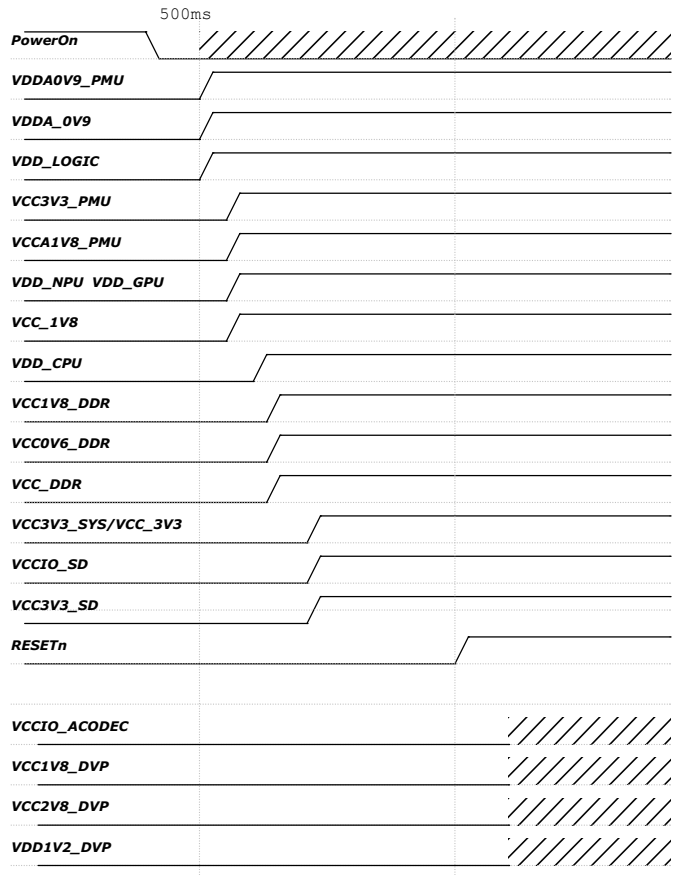
Pinetab2 Block Diagram



Power Diagram



Power Sequence & Power Path assignment



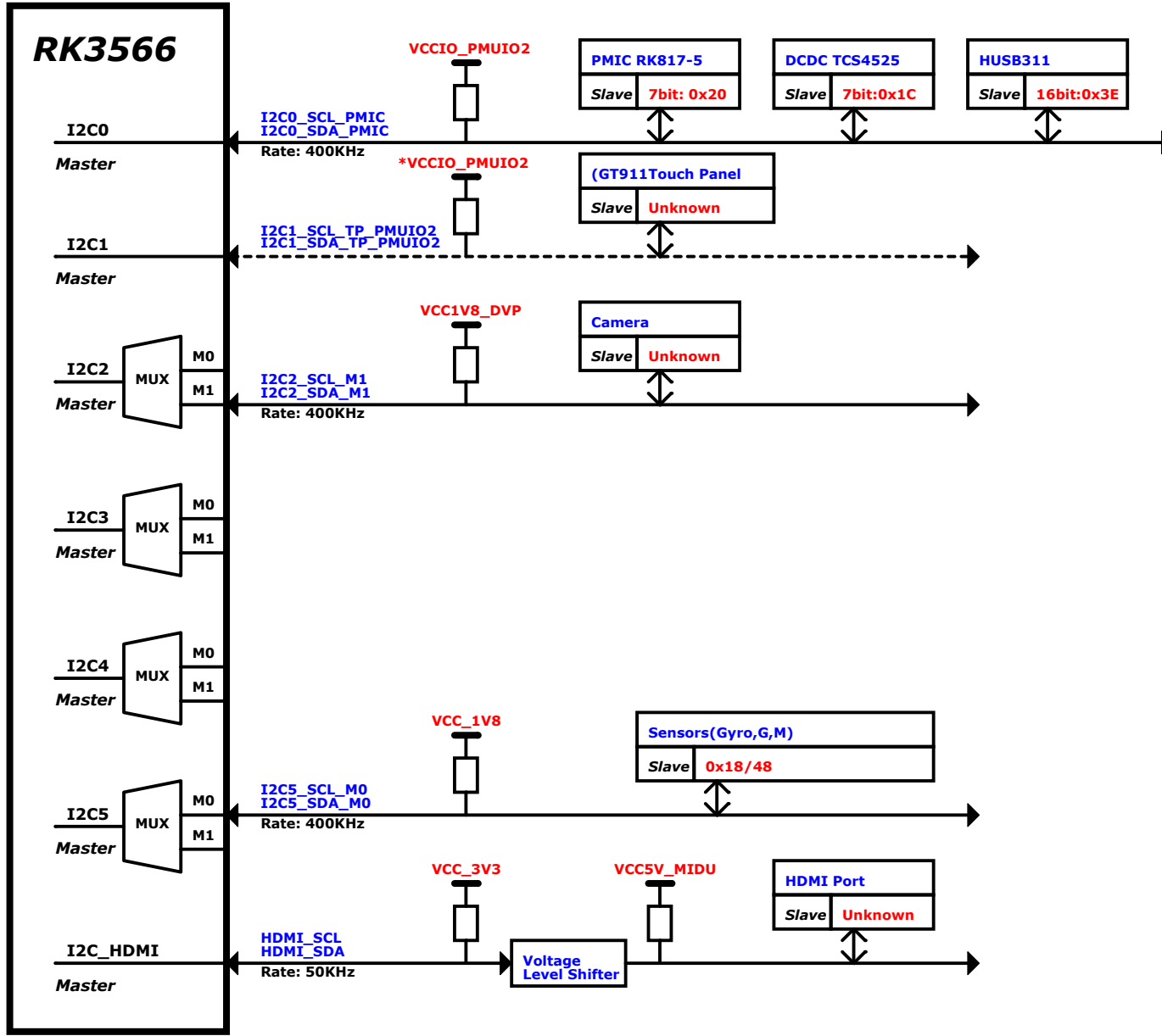
Power Source	PMIC Channel	Supply Limit	Power Supply Name	Time Slot	Default Voltage	Work Status	Sleep Status
VCC_SYS	RK817-5_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF
VCC_SYS	RK817-5_BUCK2	2.5A	VDD_NPU,VDD_GPU	Slot:2	0.9V	ON	OFF
VCC_SYS	RK817-5_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON
VCC_SYS	RK817-5_BUCK4	1.5A	VCC3V3_SYS	Slot:4	3.3V	ON	OFF
VCC_SYS	RK817-5_LDO1	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON
	RK817-5_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF
	RK817-5_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_LDO4	0.4A	VCCIO_ACODEC	N/A	--/3.3V	ON	OFF
	RK817-5_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF
	RK817-5_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON
VCC_SYS	RK817-5_LDO7	0.4A	VCC_1V8	Slot:2	1.8V	ON	OFF
	RK817-5_LDO8	0.4A	VCC1V8_DVP	N/A	--/1.8V	ON	OFF
	RK817-5_LDO9	0.4A	VCC2V8_DVP	N/A	--/2.8V	ON	OFF
VCC_BAT	RK817-5_RESETn			Slot:4+5			
VCC_BAT	RK817-5_BOOST RK817-5_OTG	1.5A	VCC5V_MIDU VBUS	N/A	--/5.0V	ON	OFF
VCC3V3_SYS	Switch		VCC_3V3	Slot:4	3.3V	ON	OFF
VCC3V3_SYS	Switch		VCC3V3_SD	Slot:4	3.3V	ON	OFF
VCC_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF
VCC_SYS	EXT BUCK	2A	VDD1V2_DVP	N/A	--/1.2V	ON	OFF

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCCA1V8_PMU	VCCA1V8_PMU	1.8V/*3.3V	1.8V as default, dts config should follow the HW design
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO_WL	VCC_1V8	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_1V8	1.8V	
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC1V8_DVP	1.8V	
VCCIO7	1N8	YES	YES	VCCIO7	VCC_3V3	3.3V	

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design. **!!! Attention**

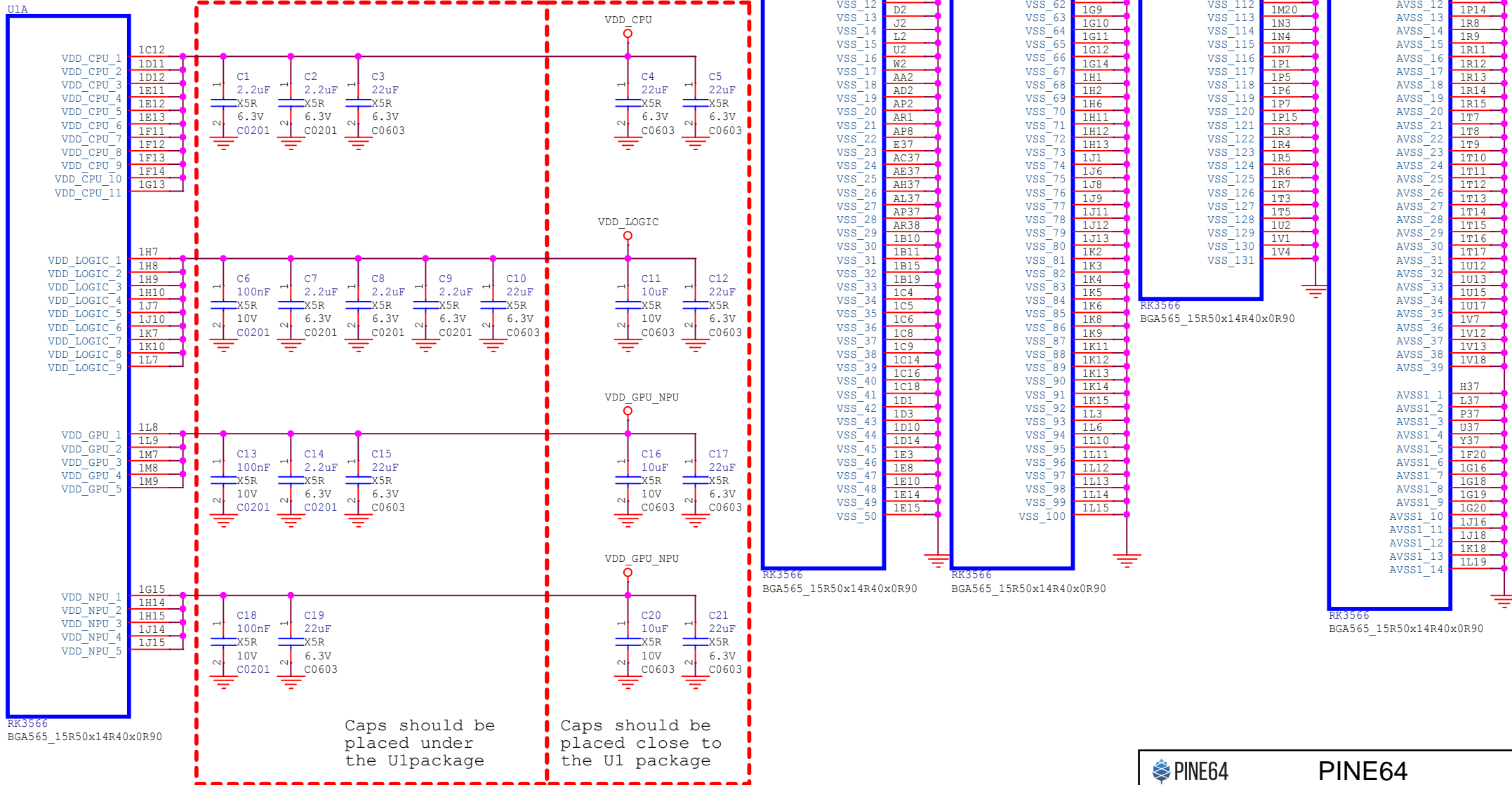
I2C MAP



PINE64		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	06.I2C_Bus_Map		
Date:	Tuesday, September 27, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
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RK3566_ABCDE

(Power&GND)



		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	07.RK3566_Power/GND		
Date:	Friday, February 17, 2023	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	8 of 37

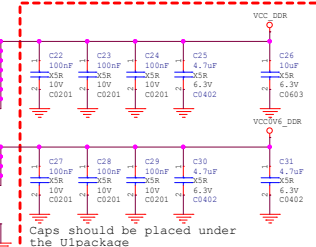
DDR4				LPDDR4				DDR3				LPDDR3			
DDR_DQ0_A	DQ0	DDR4_DQ0_A	LPDDR4_DQ0_A	DDR3_DQ0	LPDDR3_DQ0	DDR4_DQ0	LPDDR4_DQ0_B	DDR3_A0	LPDDR3_A0	DDR4_A0	LPDDR4_A0	DDR3_A0	LPDDR3_A0	DDR4_A0	LPDDR4_A0

DDR3	VDDQ	VDDQL
DDR3	1.35V	1.35V
DDR4	1.50V	1.50V
LPDDR3	1.20V	1.20V
LPDDR4	1.10V	1.10V
LPDDR4X	1.10V	0.60V

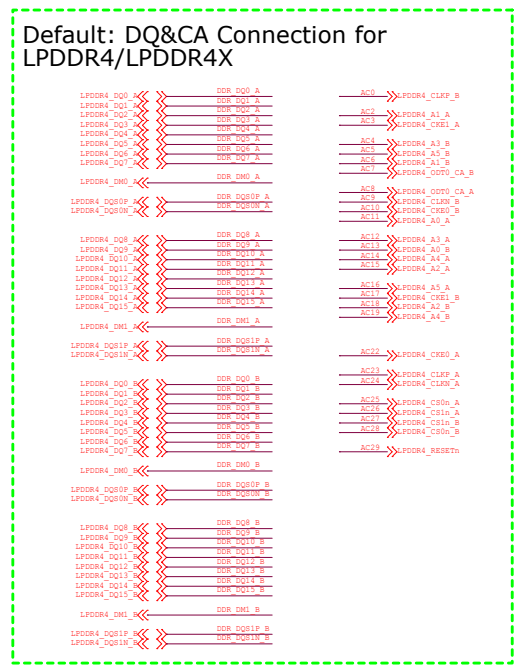
Note: Except DDR3, other DQ sequences can not be swap

Note: Sequences can not be swap

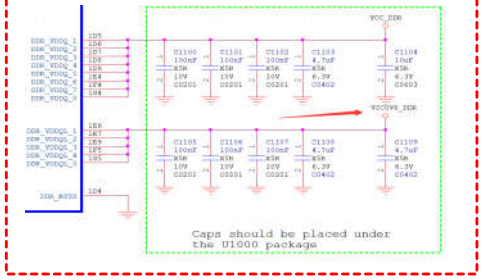
Note: Pull up for LPDDR4/LPDDR4X --> R1100=DNF, R1101=120R; Pull down for DDR4/DDR3/LPDDR3 --> R1100=120R, R1101=DNF; The resistor parameter is 120R ±1%.



For LPDDR4X DDR_VDDQL = 0.6V, refer to the connection example

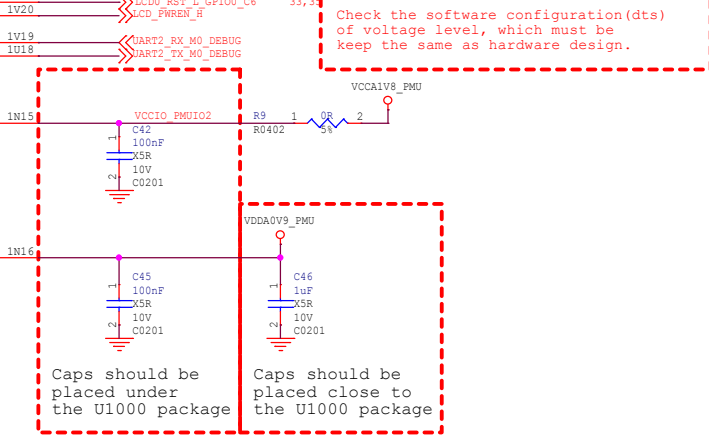
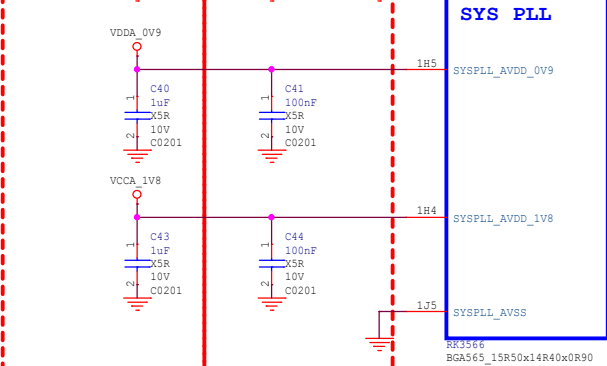
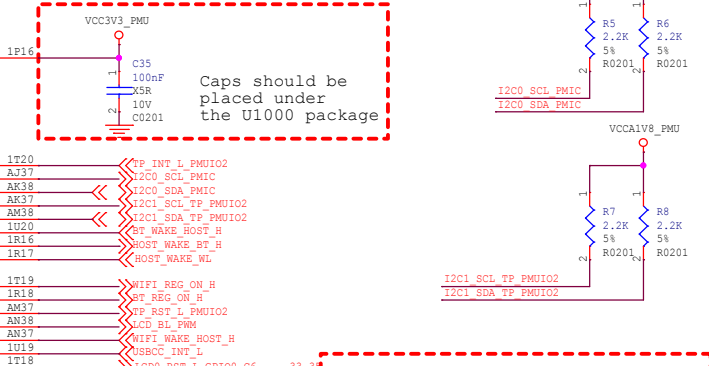
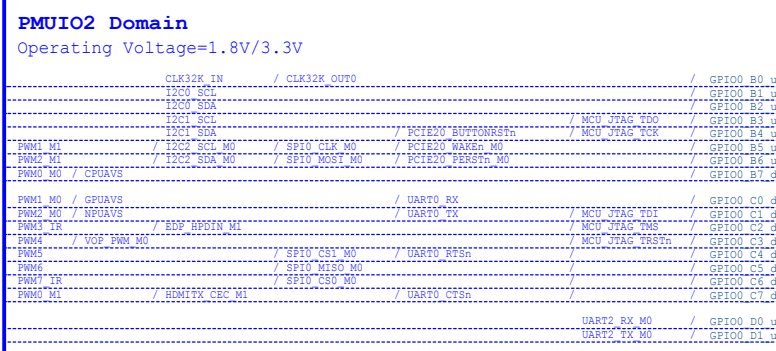
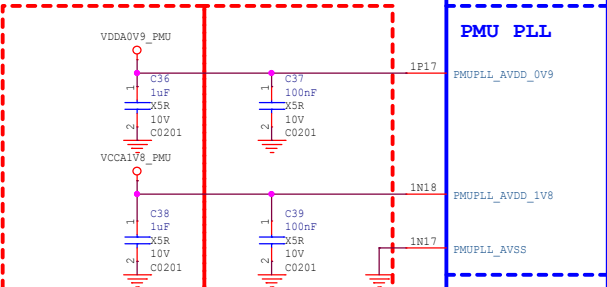
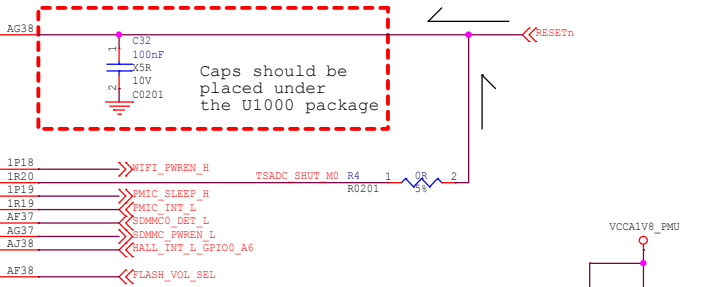
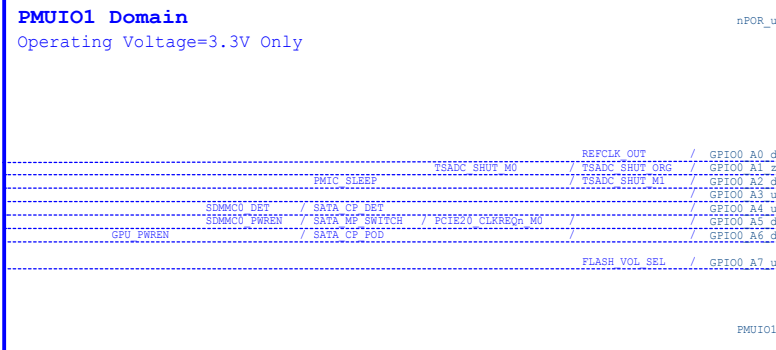
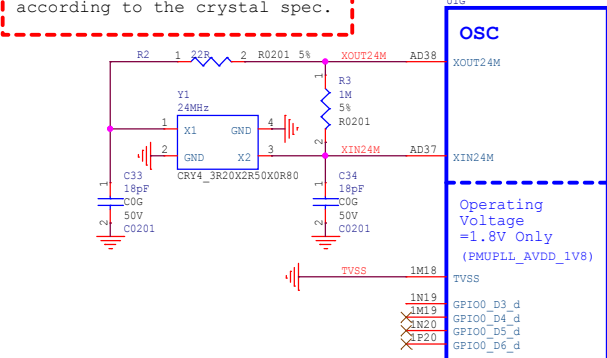


Note: LPDDR4x mode: Pin 1E6, 1E7, 1E9, 1F5, 1G5 connected to VCC0V6_DDR power supply



RK3566_G (OSC/PLL/PMUIO1/2)

Adjust the load capacitor according to the crystal spec.



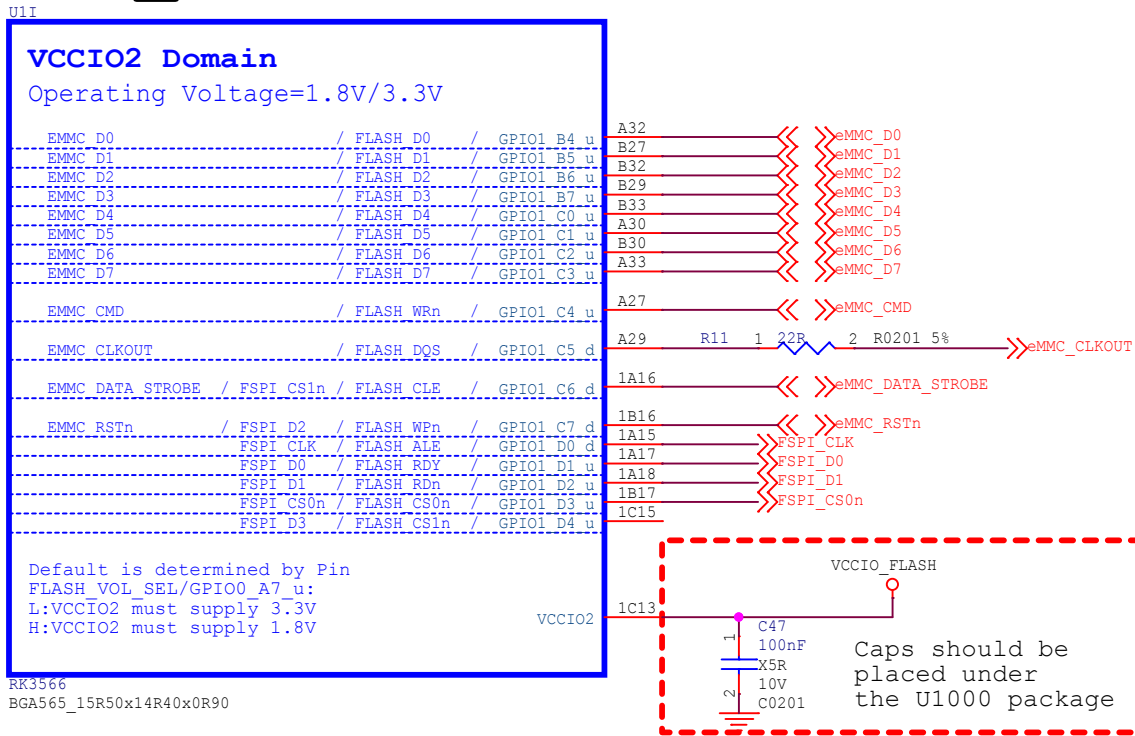
Caps should be placed close to the U1000 package

Caps should be placed under the U1000 package

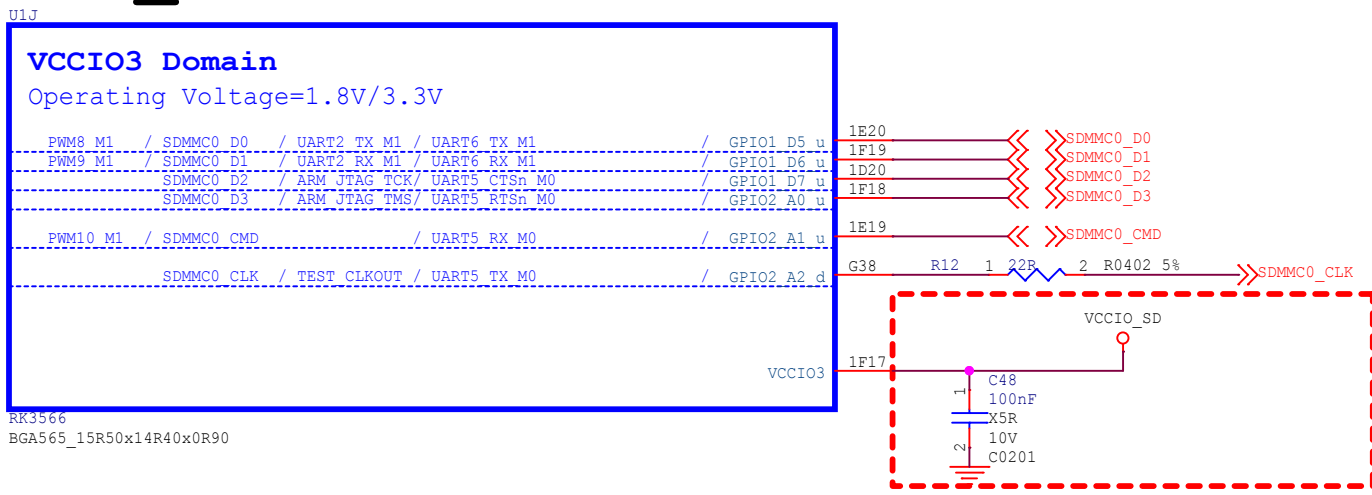
Check the software configuration (dts) of voltage level, which must be keep the same as hardware design.

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Project:	PineTab2 Schematic-20230417		
File:	09.RK3566_OSC/PLL/PMUIO		
Date:	Monday, March 27, 2023	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
Sheet:	10	of	37

RK3566_I (VCCIO2 Domain)



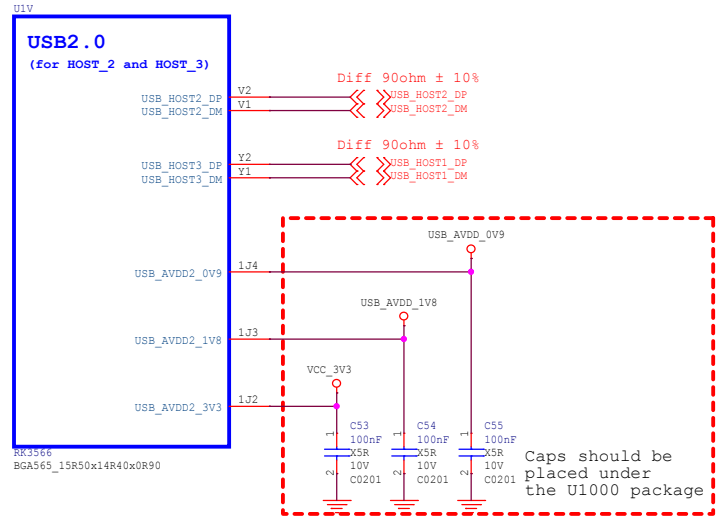
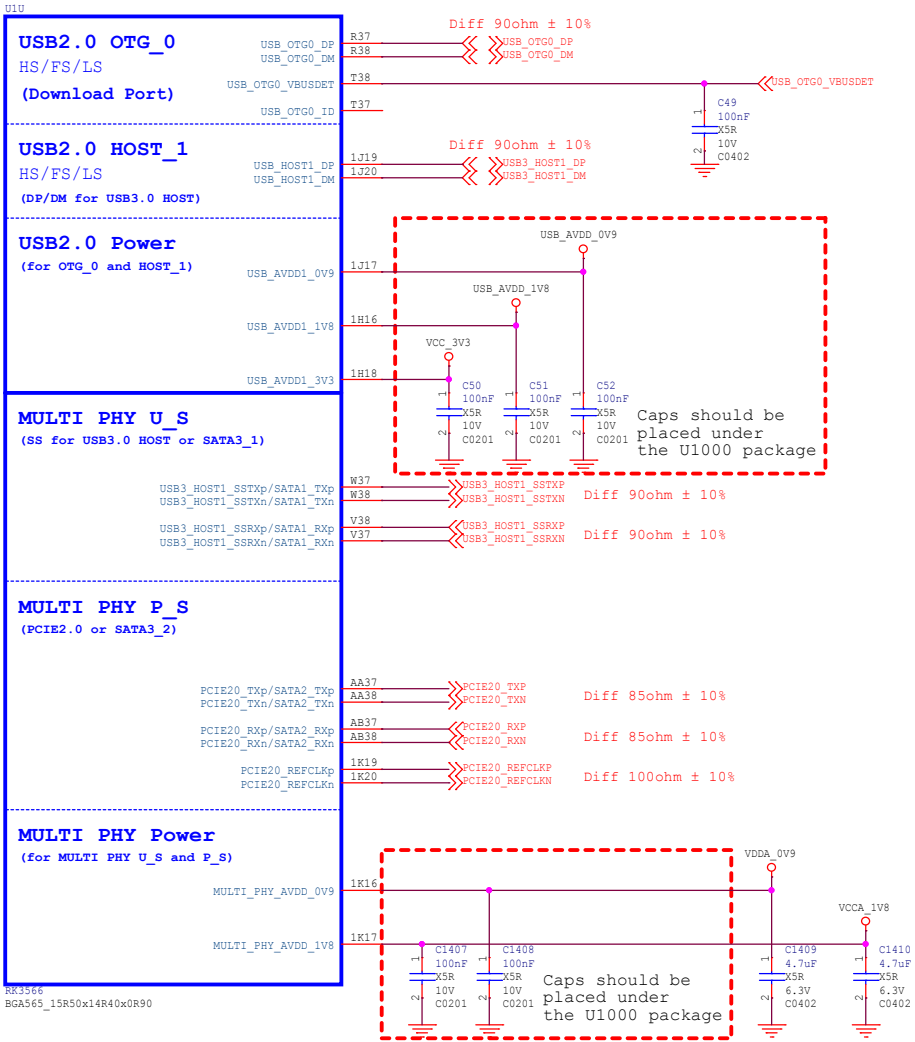
RK3566_J (VCCIO3 Domain)



		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	10.RK3566_Flash/SD_Controller		
Date:	Wednesday, September 28, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	11 of 37

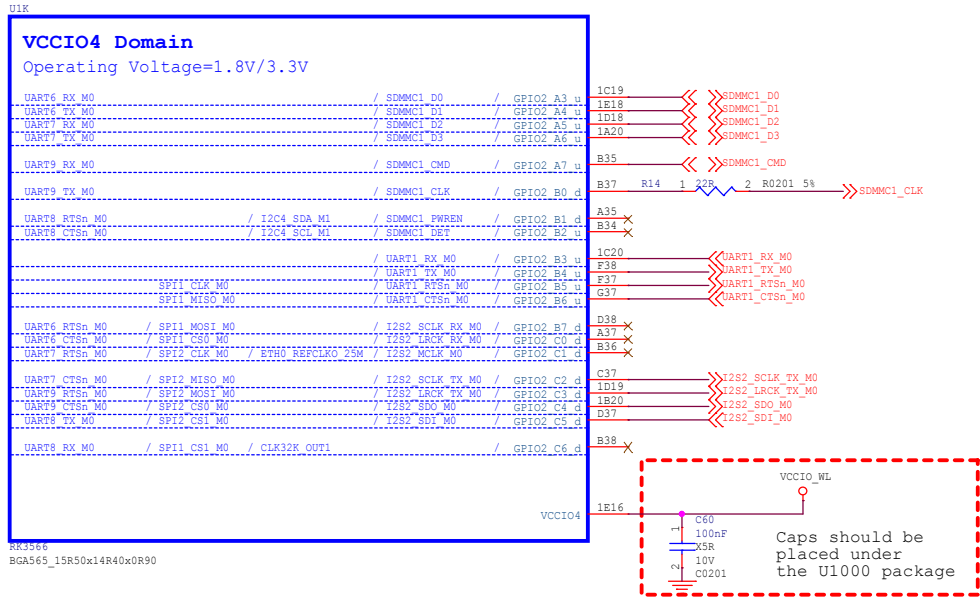
RK3566_U (USB3.0/PCIe2.0x1/SATA)

RK3566_V (USB2.0 HOST)

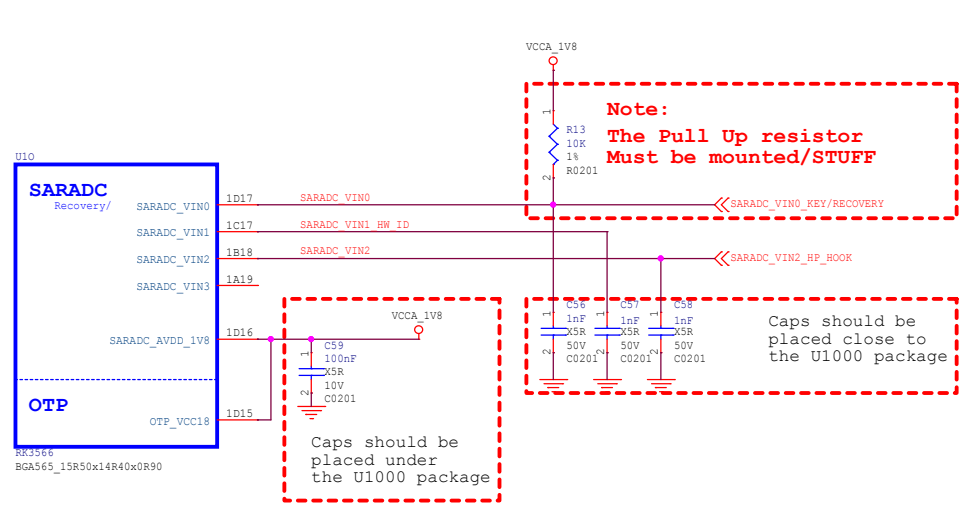


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Project:	PineTab2 Schematic-20230417
File:	11.RK3566_USB/PCIe/SATA_PHY
Date:	Sunday, October 09, 2022
Designed by:	Daniel.J
Reviewed by:	Default
Rev:	V2.0
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RK3566_K (VCCIO4 Domain)

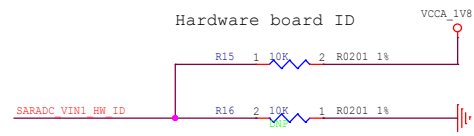
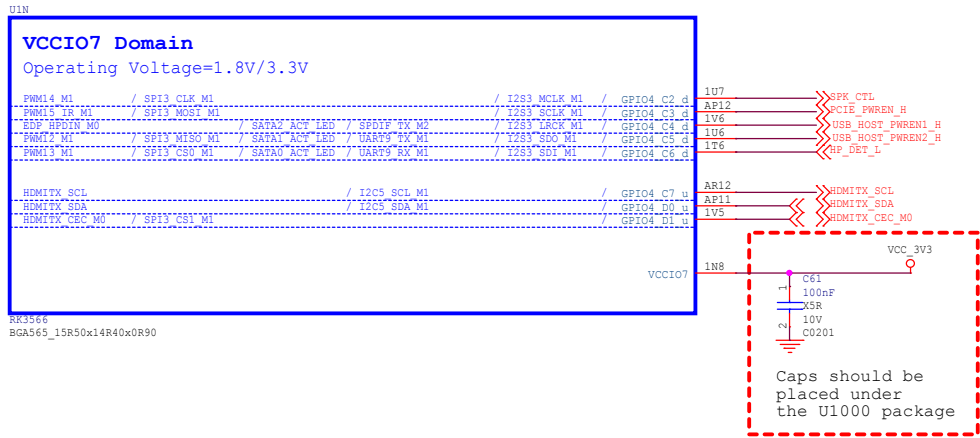


RK3566_O (SARADC/OTP)

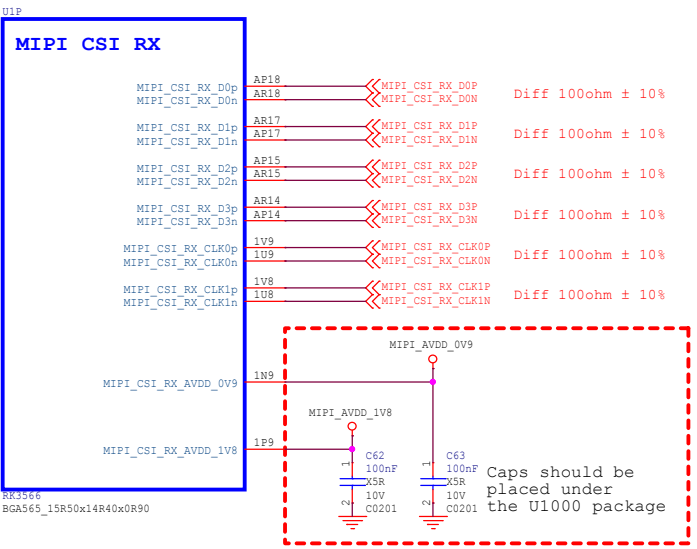
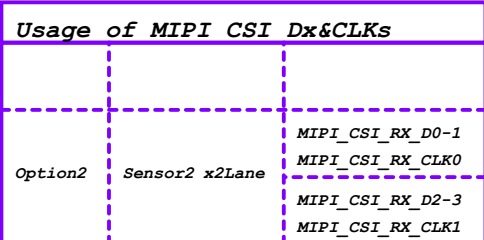


SARADC_VIN1_HW_ID	Rup	Rdown	ADC	
Version 1	10K	DNP	1023	1.8V
Version 2	20K	100K	852	1.5V
Version 3	18K	36K	681	1.2V
Version 4	51K	51K	512	0.9V
Version 5	36K	18K	340	0.6V
Version 6	100K	20K	170	0.3V
Version 7	DNP	10K	0	0V

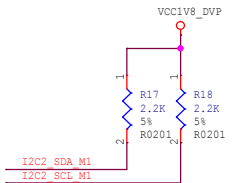
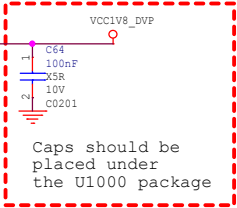
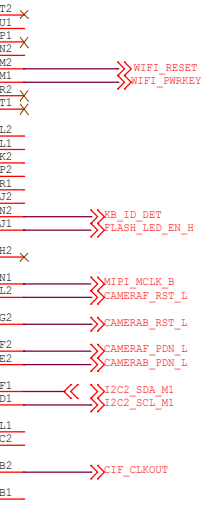
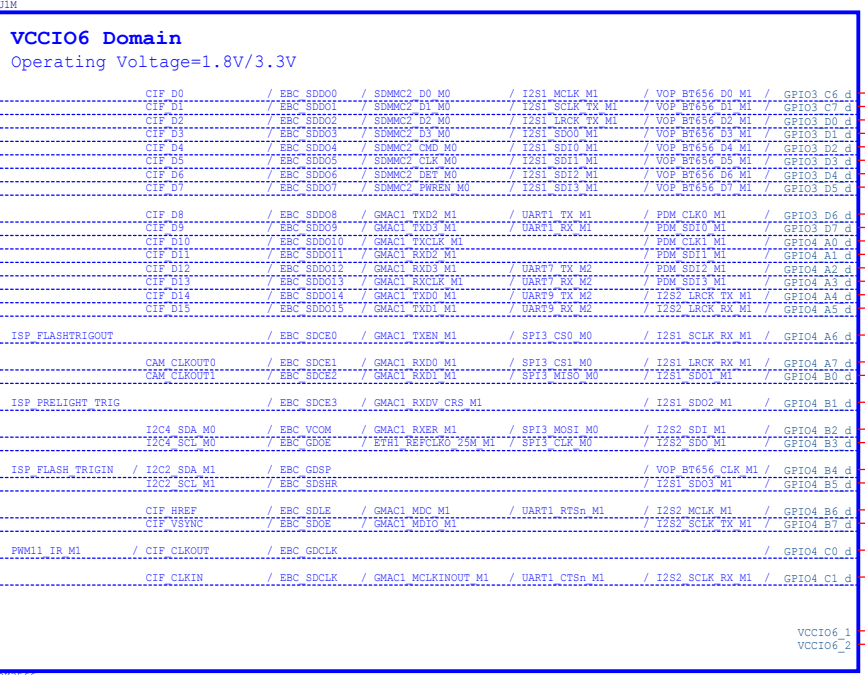
RK3566_N (VCCIO7 Domain)



RK3566_P (MIPI CSI_RX)

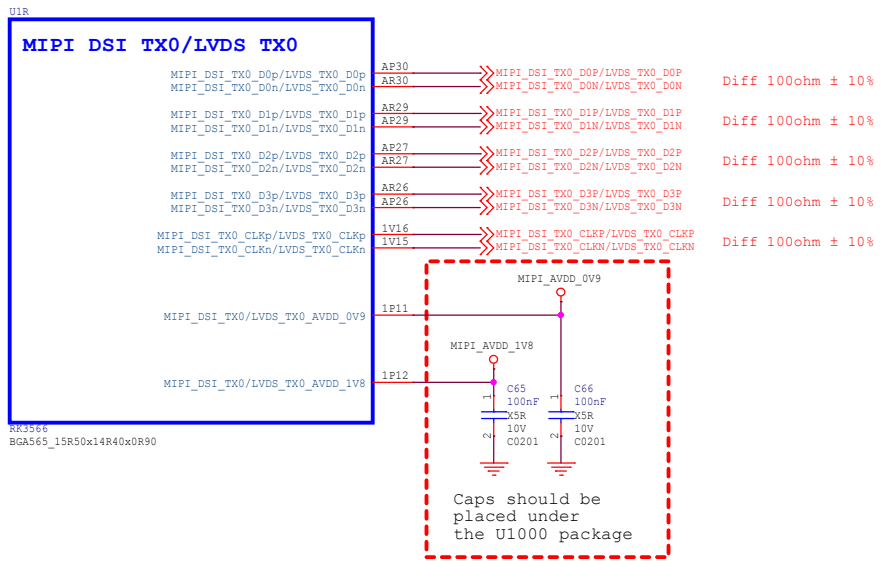


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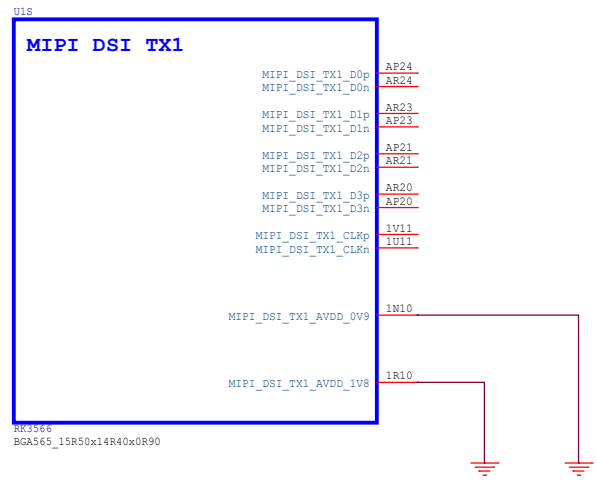


Note:
default VCCIO of Camera is 1.8V

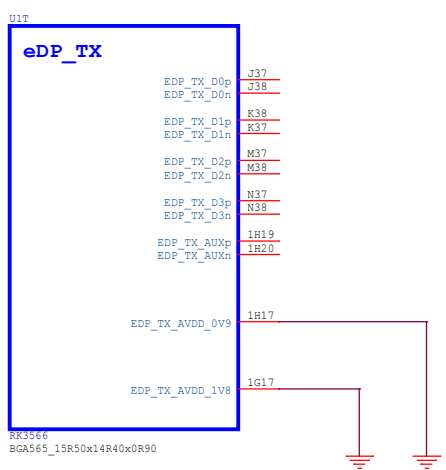
RK3566_R (MIPI_DSI_TX0/LVDS_TX0)



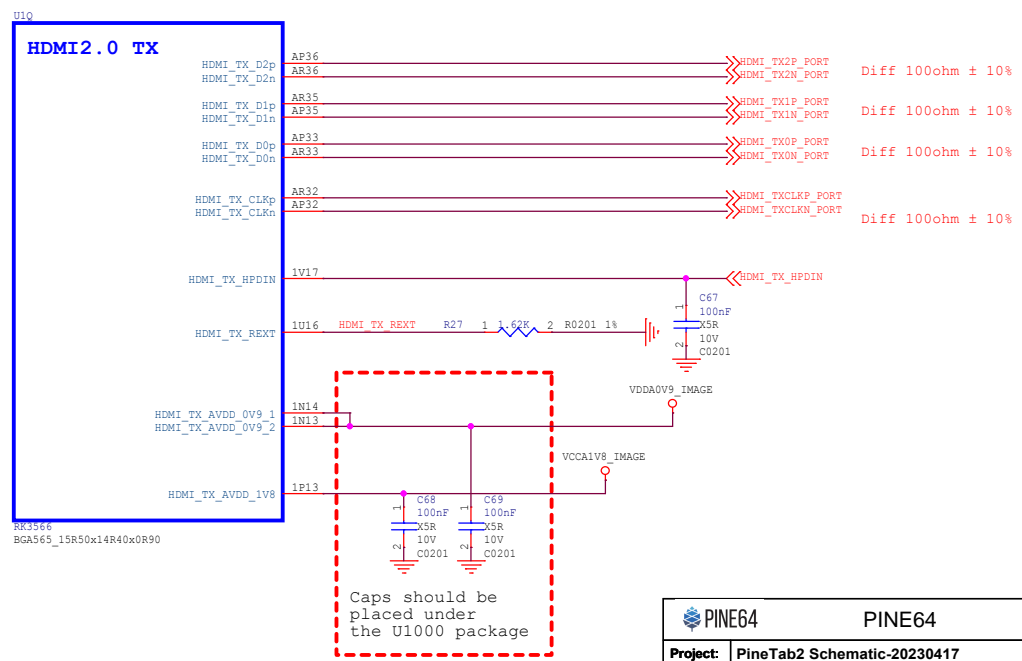
RK3566_S (MIPI_DSI_TX1)



RK3566_T (eDP TX)



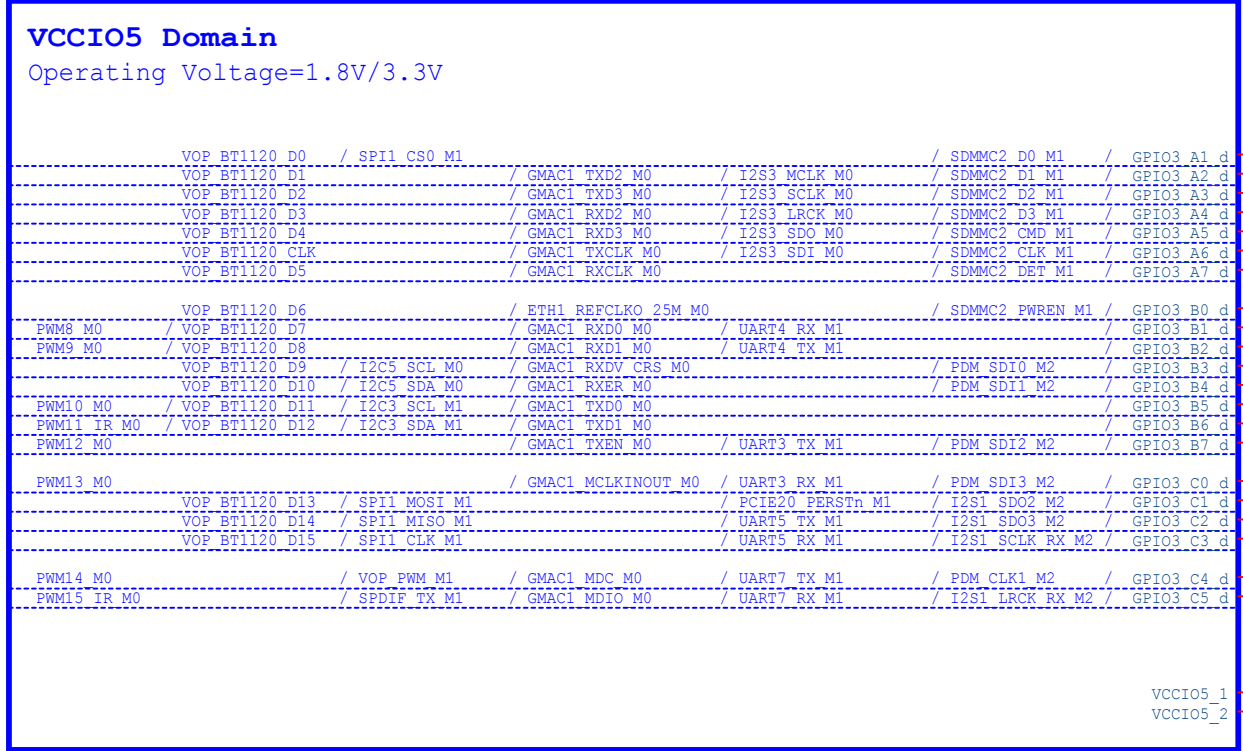
RK3566_Q (HDMI2.0 TX)



		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	14.RK3566_VO_Interface_1		
Date:	Tuesday, September 27, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	15 of 37

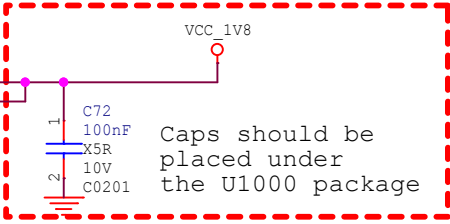
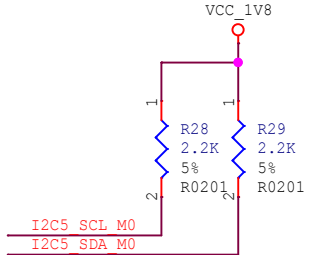
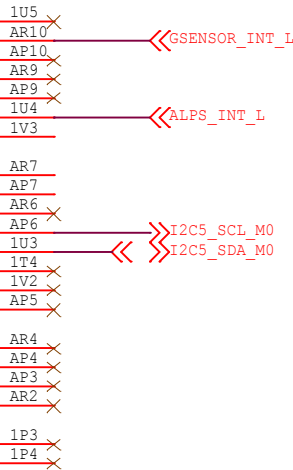
RK3566_L (VCCIO5 Domain)

U1L



RK3566
BGA565_15R50x14R40x0R90

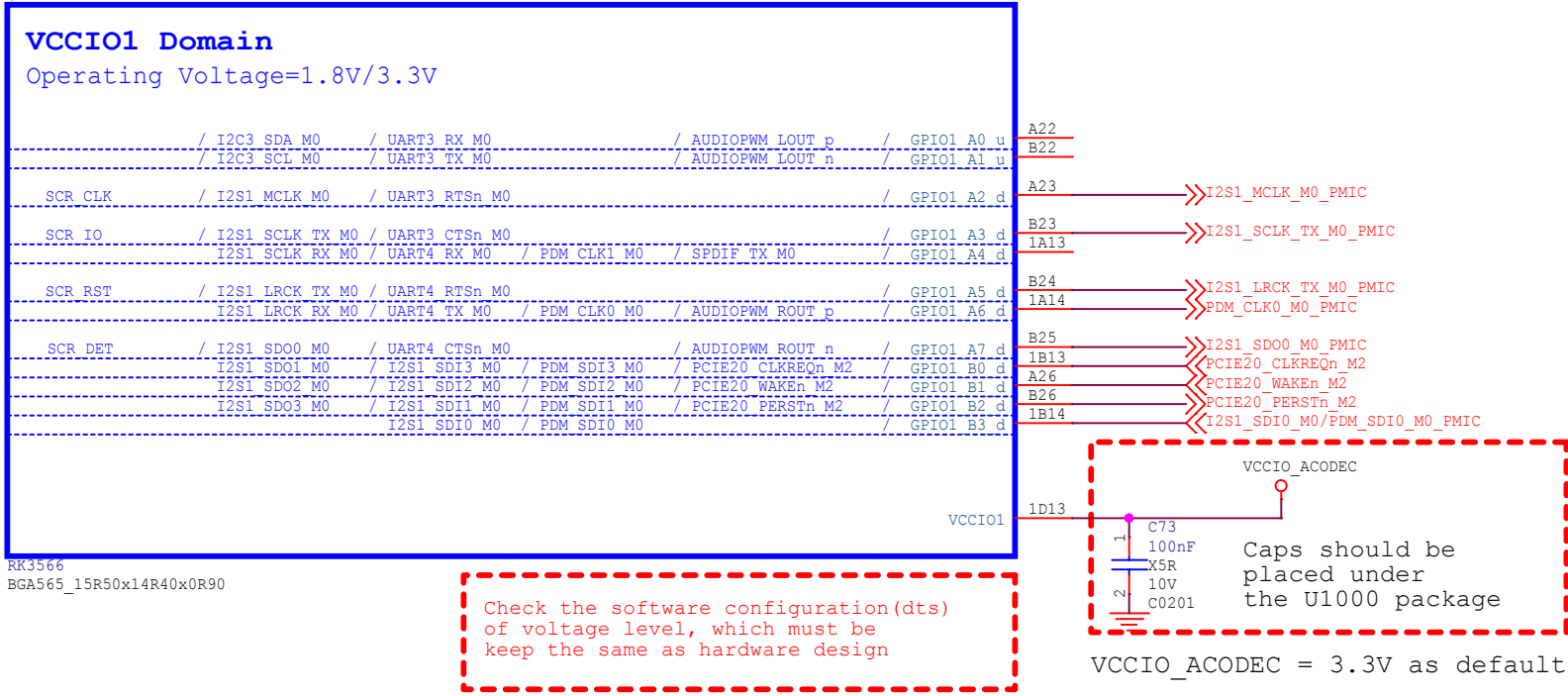
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design



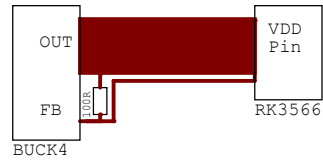
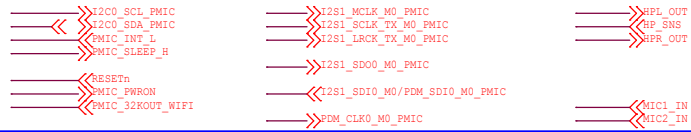
		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	15.RK3566_VO_Interface_2		
Date:	Tuesday, October 11, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	16 of 37

RK3566_H (VCCIO1 Domain)

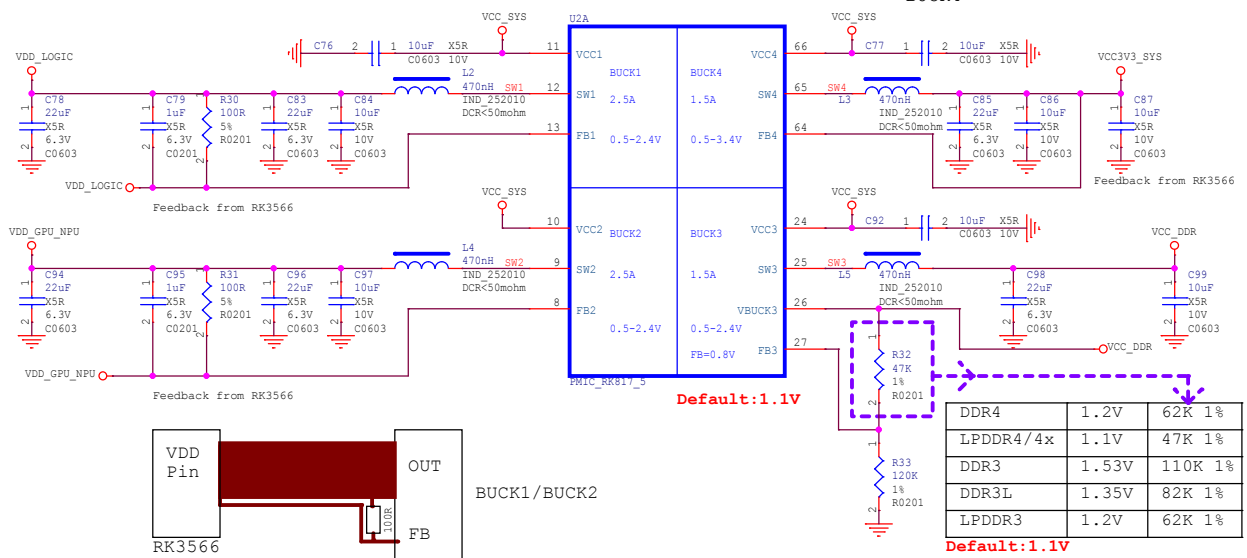
U1H



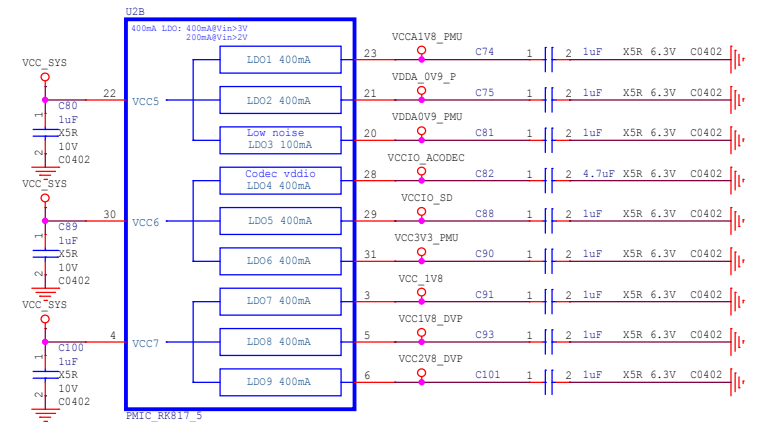
		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	16.RK3566_Audio_Interface		
Date:	Tuesday, September 27, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	17 of 37



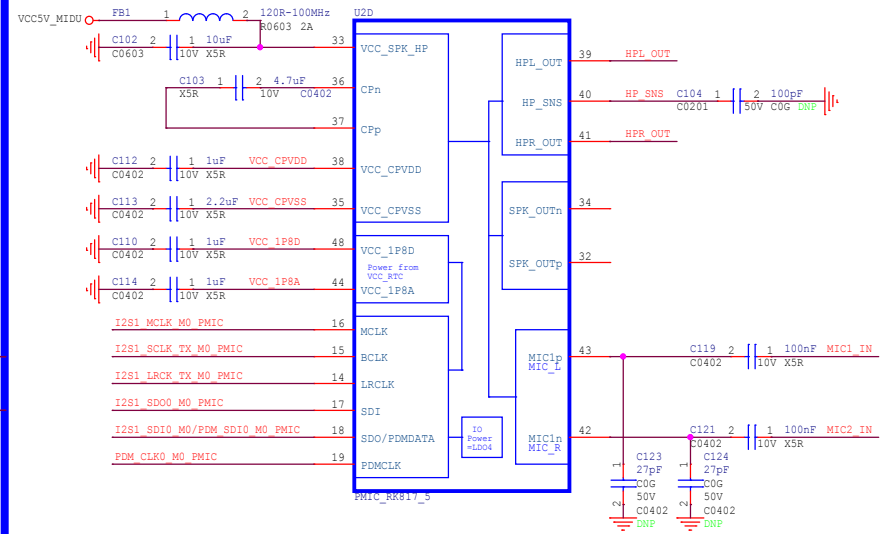
PMIC RK817 DCDC



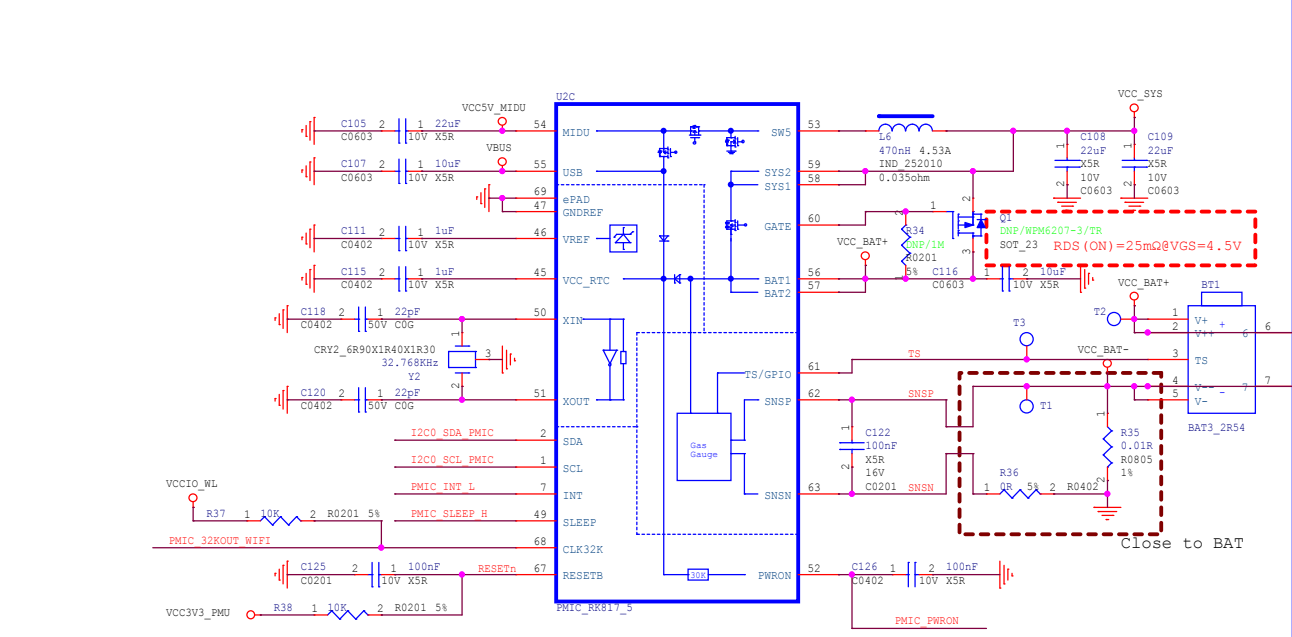
PMIC RK817 LDO



PMIC RK817 CODEC

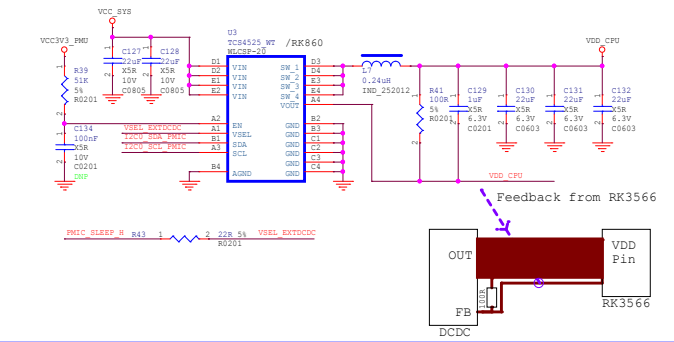


PMIC RK817 Management

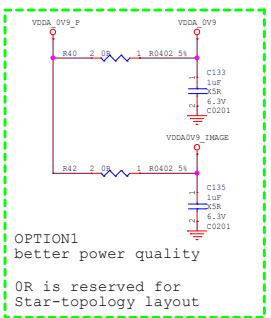




VDD_CPU_EXT(DEFAULT)

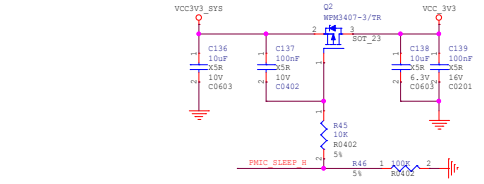


VDDA_0V9, VDDA0V9_IMAGE

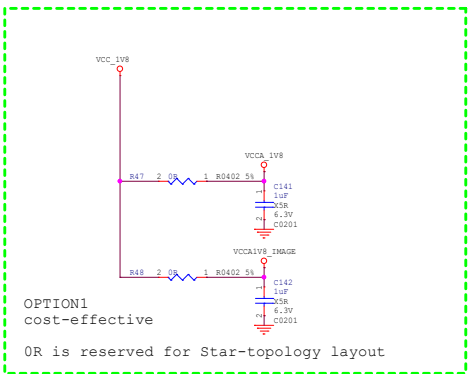


OPTION1
better power quality
OR is reserved for
Star-topology layout

VCC_3V3 (Power OFF under SLEEP)

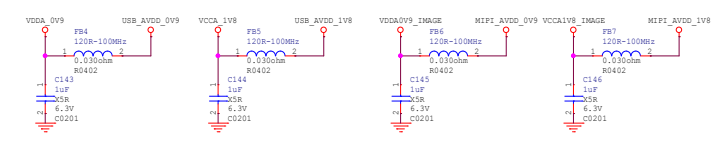


VCC_1V8, VCCA_1V8, VCCA1V8_IMAGE

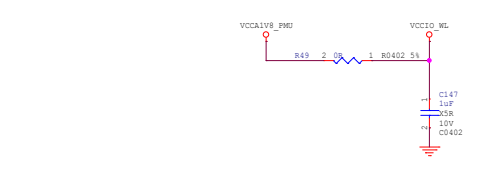


OPTION1
cost-effective
OR is reserved for Star-topology layout

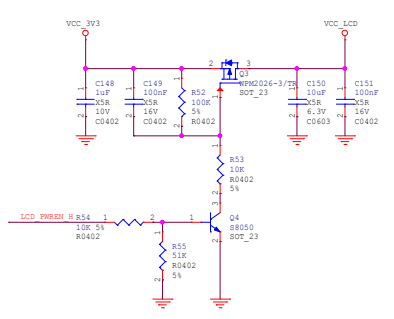
Power for USB / MIPI



VCCIO_WL

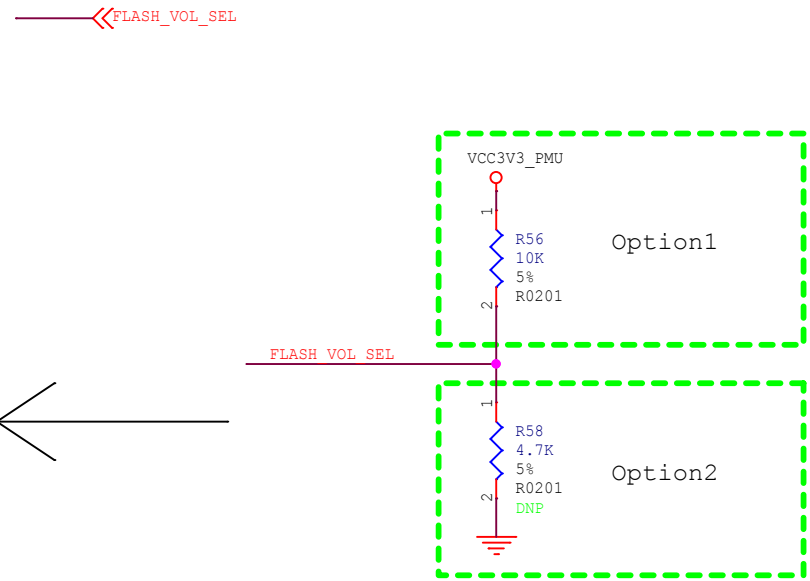
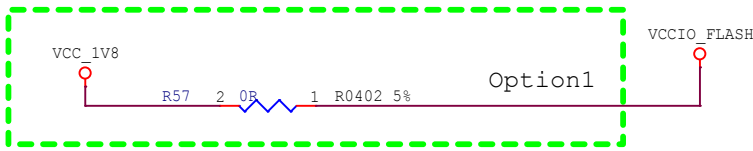


Power for MIPI Panel



Flash Power Manage

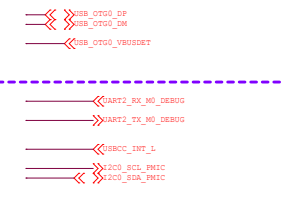
	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=L(Default)



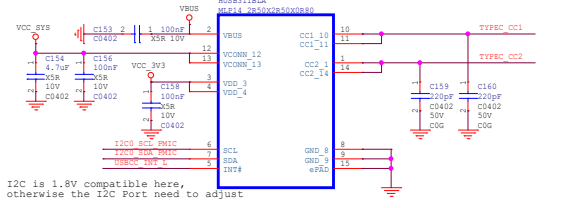
FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
 Logic=L: 3.3V IO driven
 Logic=H: 1.8V IO driven

		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	19.Power_Flash_Power_Manage		
Date:	Tuesday, September 27, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	20 of 37

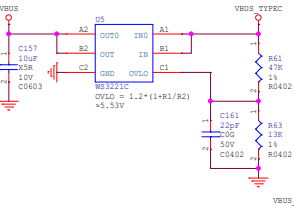
USB2.0 OTG



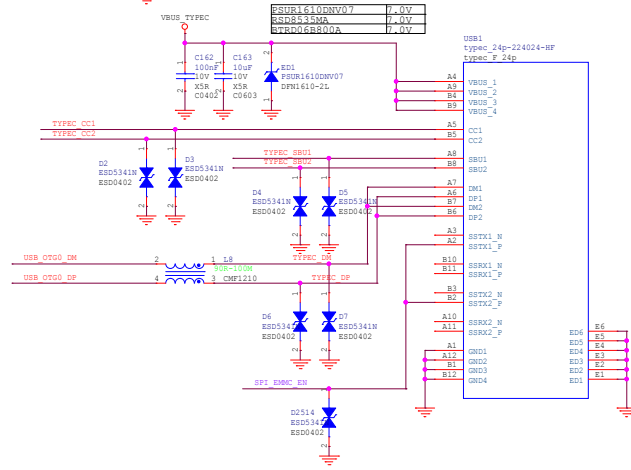
CC Detection



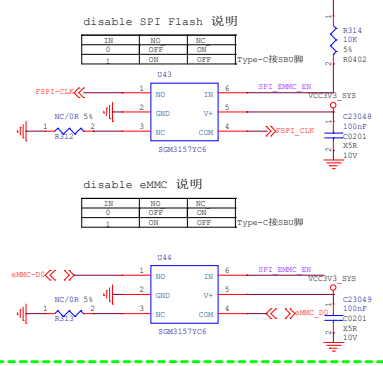
OVP



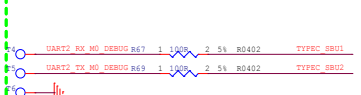
TypeC Port



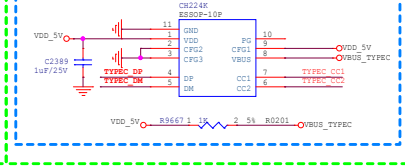
SD卡启动禁用SPI eMMC电路



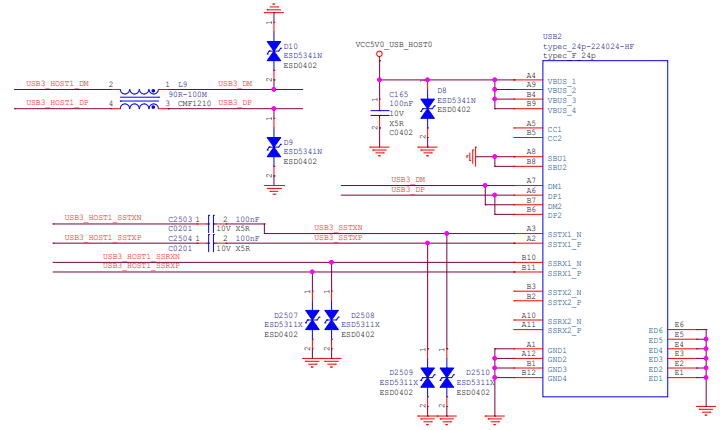
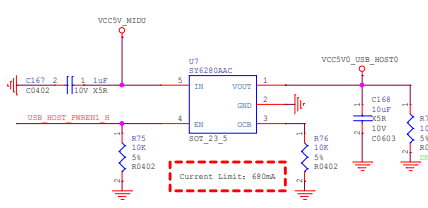
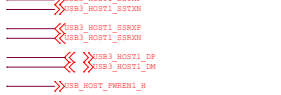
SBU-UART



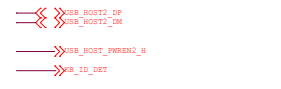
PD诱电芯片



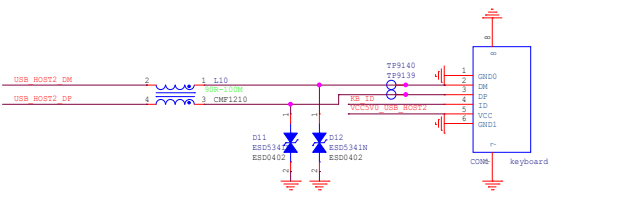
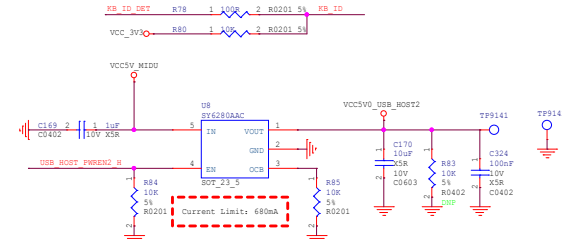
USB3.0 HOST TYPE-C



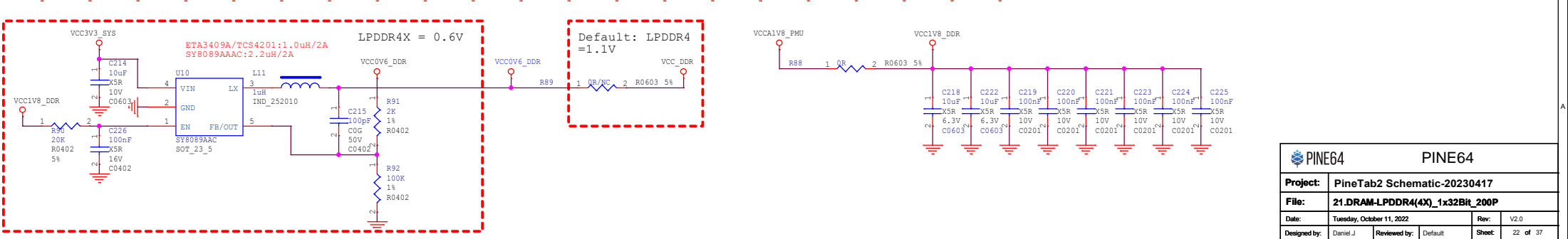
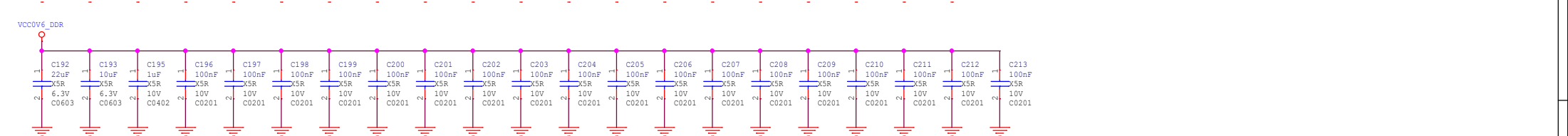
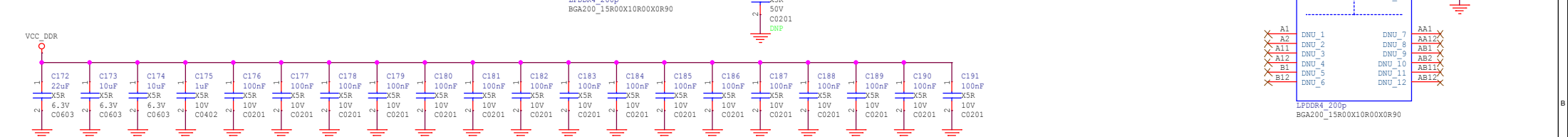
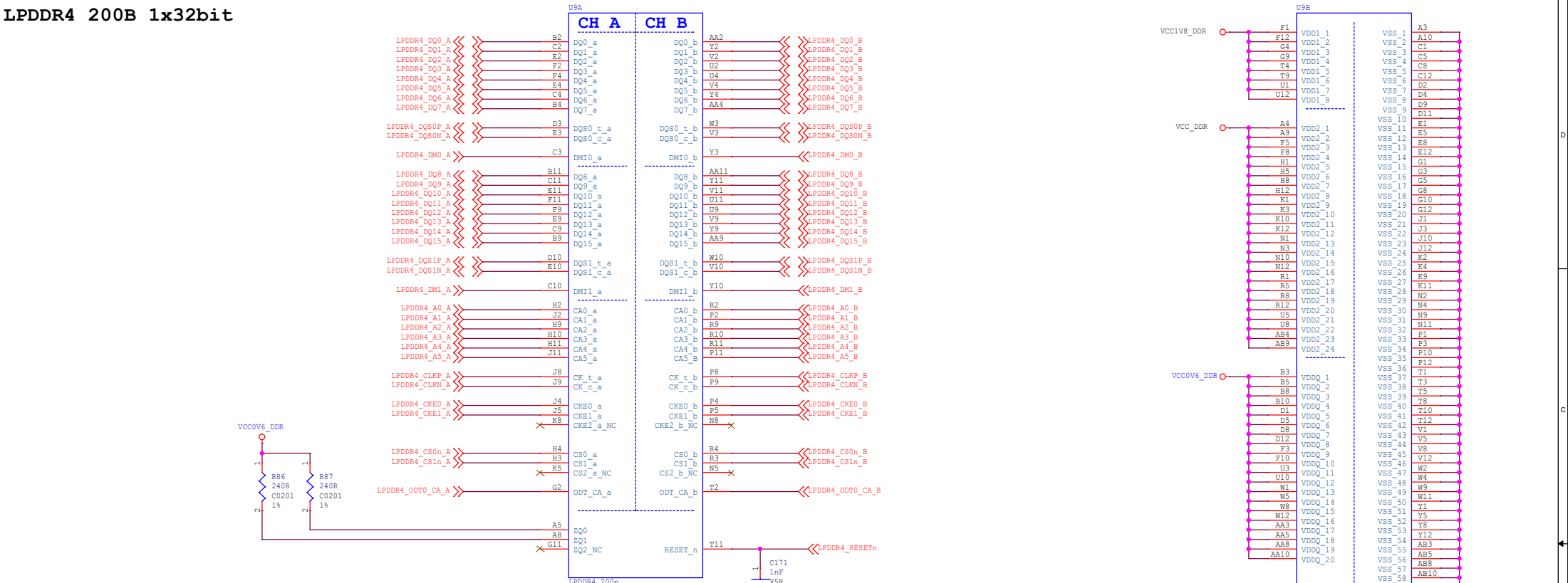
USB2.0 HOST POGO PIN



键盘检测ID

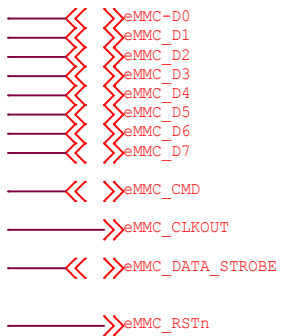


LPDDR4 200B 1x32bit



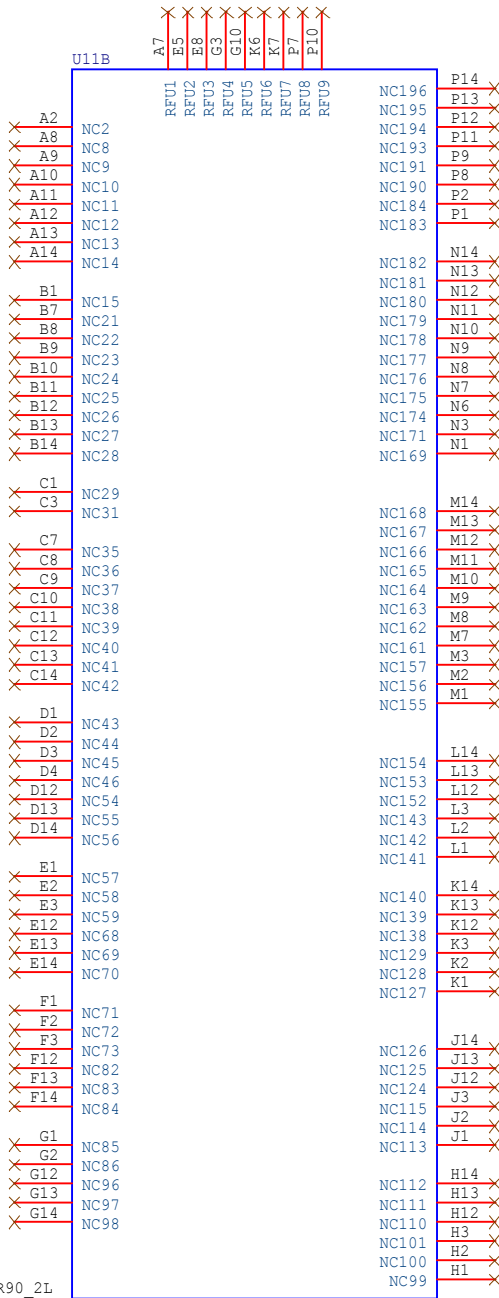
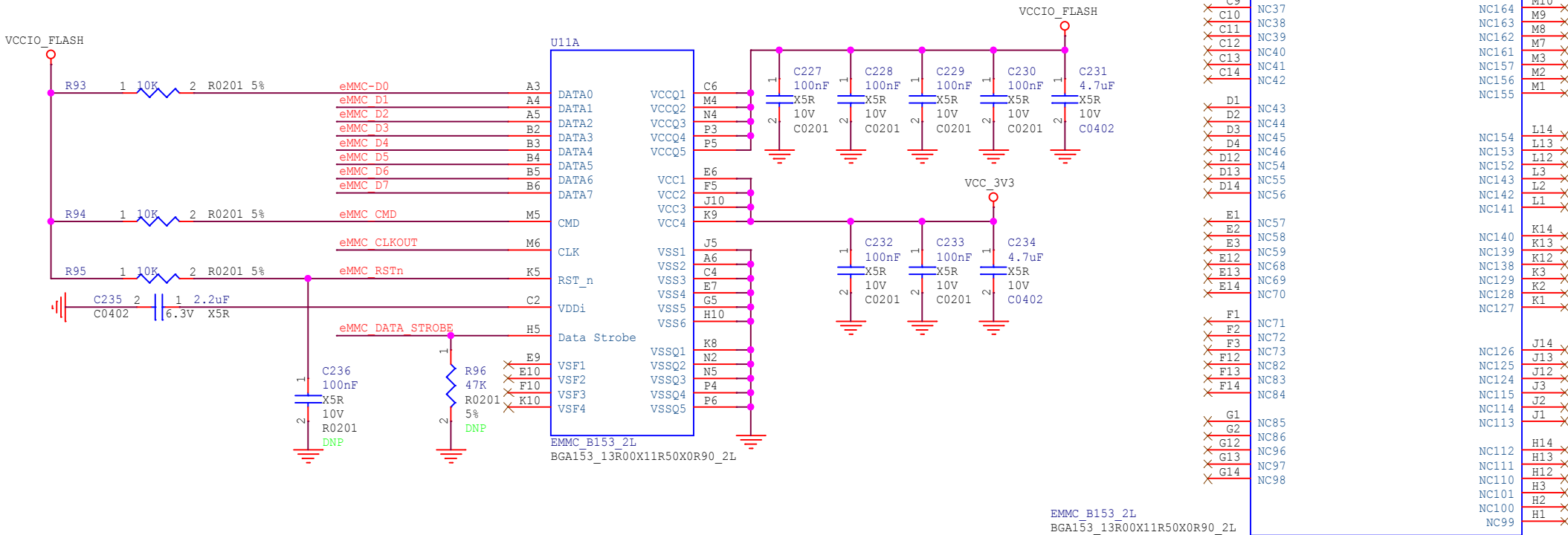
PINE64		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	21.DRAM-LPDDR4(4X)_1x32Bit_200P		
Date:	Tuesday, October 11, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	22 of 37

eMMC



1. eMMC or Nand Flash:
Short 'eMMC_D0/FLASH_D0' and GND to enter Maskrom Mode.

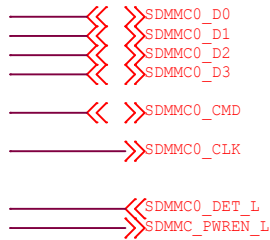
Be sure to reserve the testpoints for firmware burning or update.



EMMC B153 2L
BGA153_13R00X11R50X0R90_2L

		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	22.Flash-eMMC_Flash		
Date:	Wednesday, September 28, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	23 of 37

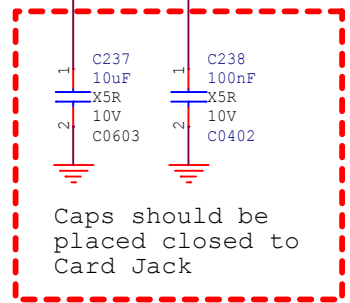
MicroSD Card



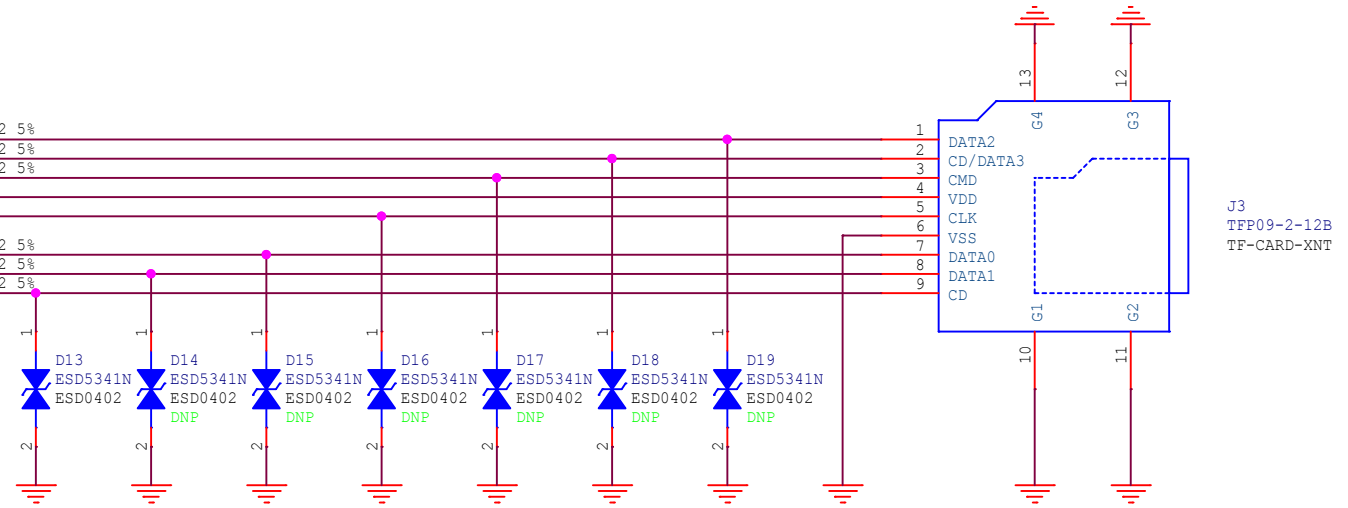
Note:
 Take care of the type of MicroSD Card Jack,
 The type here follow the logic below:
 DET is float @ card ejected; the internal pull up decided the IO pin status
 DET is connected to GND @ card inserted
 If other type of Jack is used, need to shift the status of DET.

VCC3V3_SD

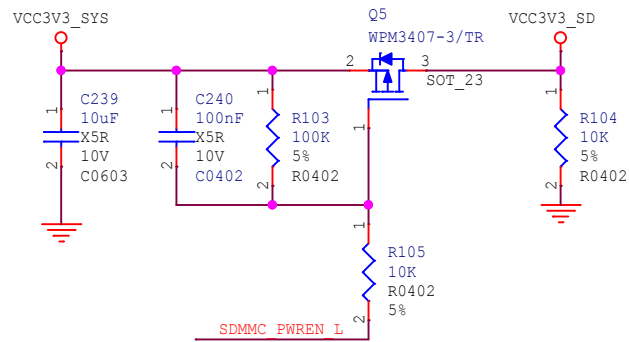
SDMMC0 D2	R98	1	22R	2	R0402 5%
SDMMC0 D3	R97	1	22R	2	R0402 5%
SDMMC0 CMD	R99	1	22R	2	R0402 5%
SDMMC0 D0	R100	1	22R	2	R0402 5%
SDMMC0 D1	R101	1	22R	2	R0402 5%
SDMMC0 DET L	R102	1	100R	2	R0402 5%



Caps should be placed closed to Card Jack



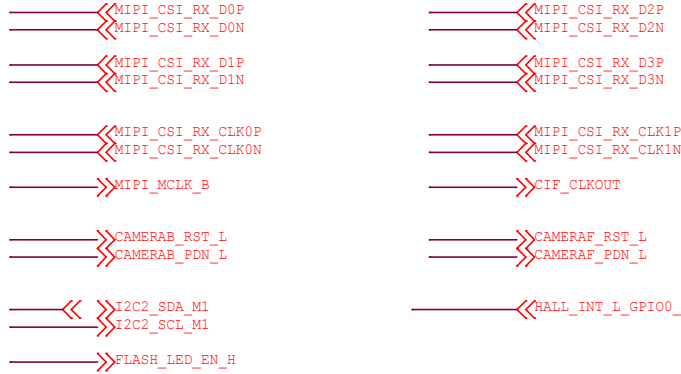
MicroSD Card



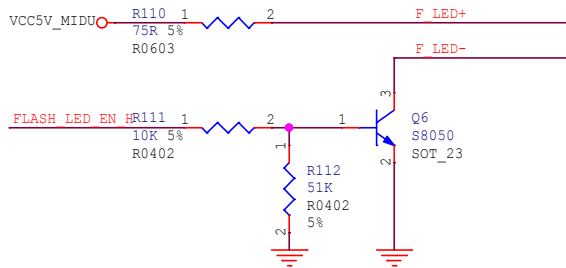
		<h2>PINE64</h2>	
Project:	PineTab2 Schematic-20230417		
File:	23.Flash-MicroSD_Card		
Date:	Wednesday, January 18, 2023	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	24 of 37

MIPI Camera (MIPI_CSI_RX 2+2lanes)

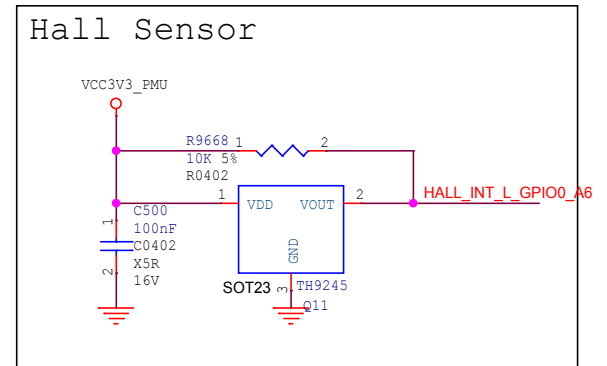
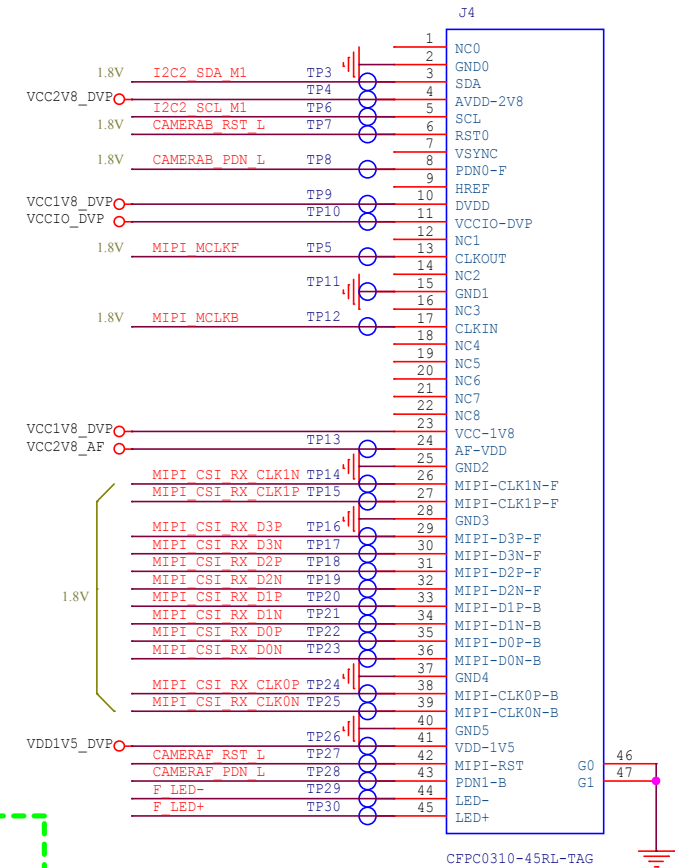
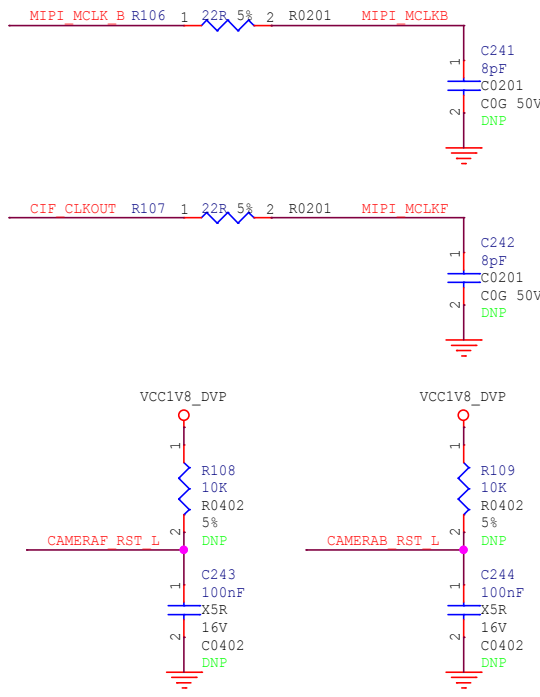
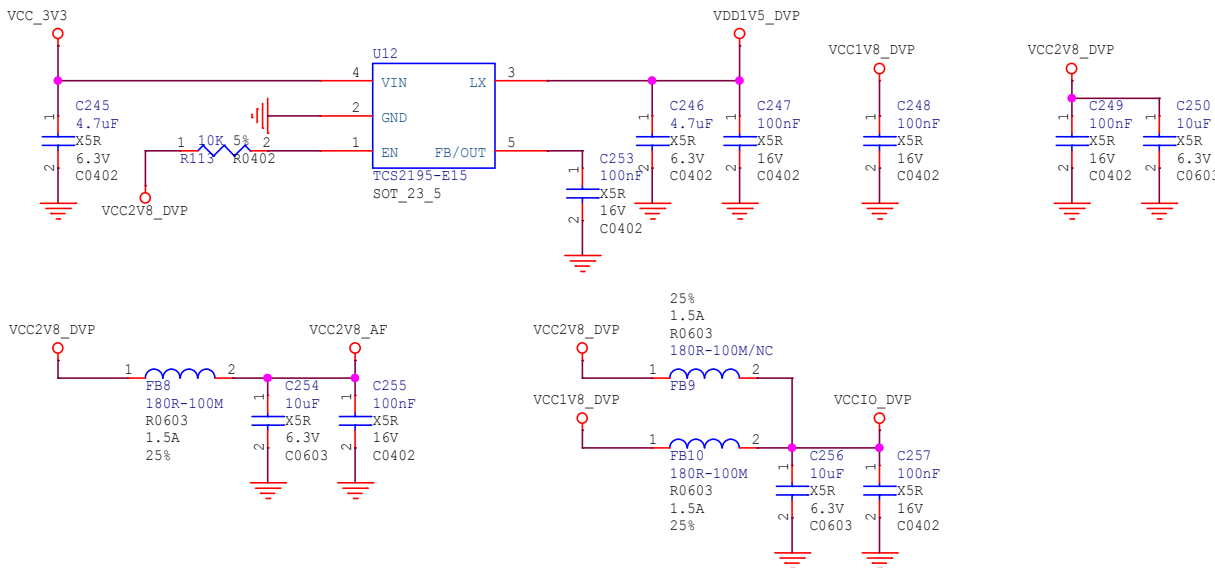
前200W GC02M2, 后500W OV5648



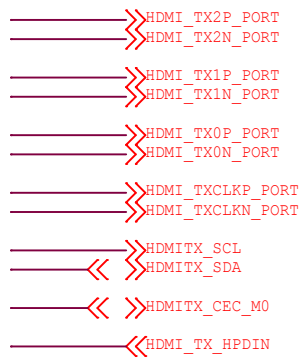
FLASH LED



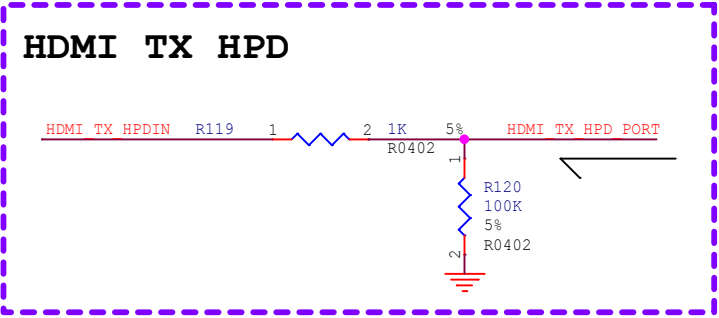
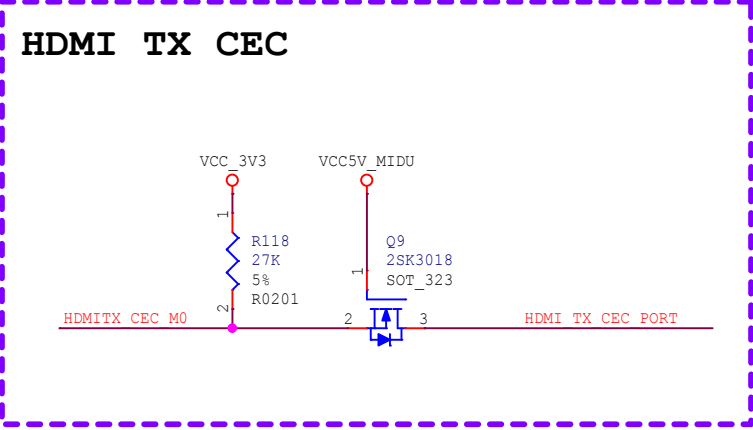
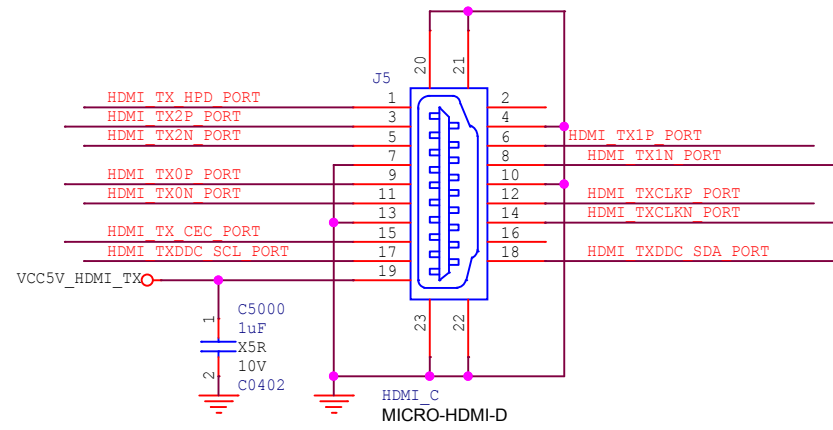
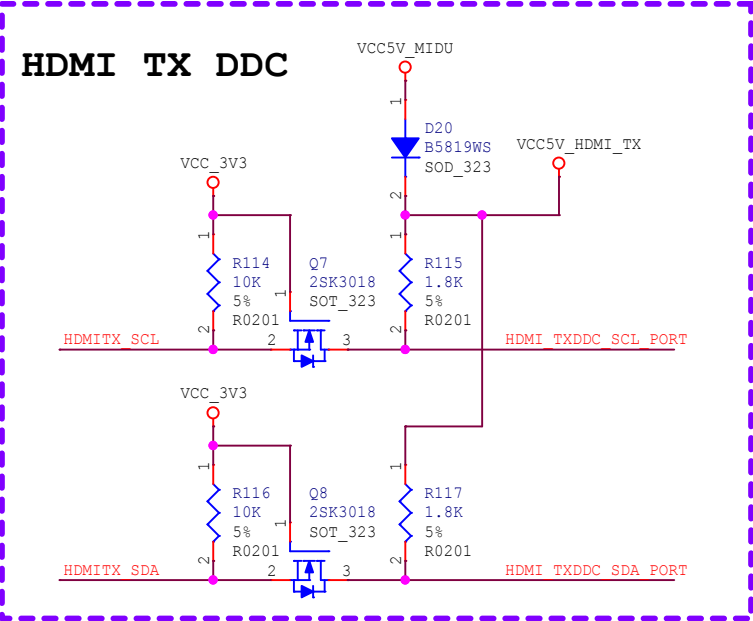
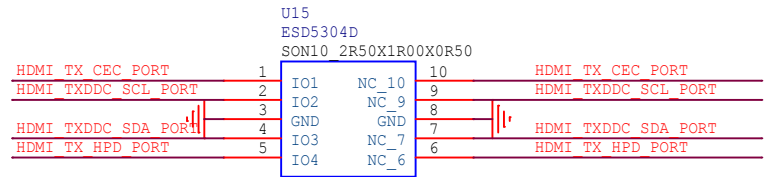
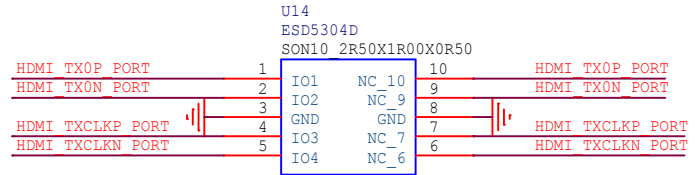
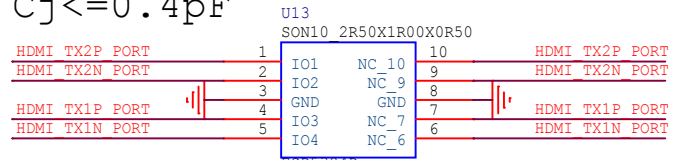
Power for Camera



		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	24.VI-Camera_MIPI_CSI(Dual)		
Date:	Monday, March 27, 2023	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
Sheet:	25 of 37		



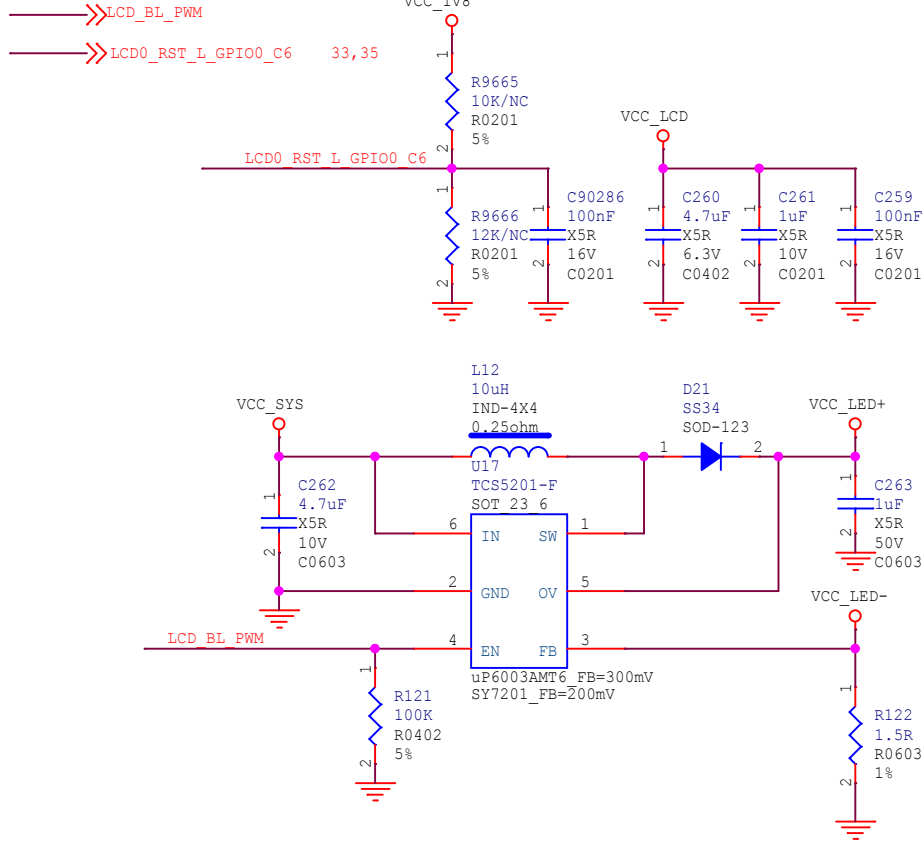
Cj <= 0.4pF



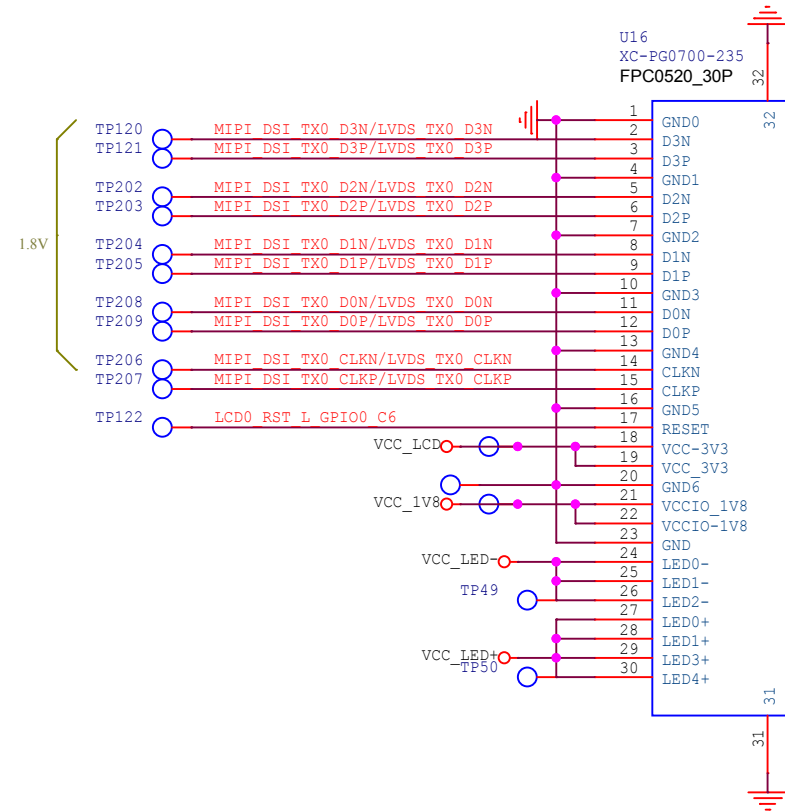
		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	25.VO-DV2.0_TX		
Date:	Tuesday, September 27, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	26 of 37

MIPI Panel

- MIPI_DSI_TX0_D0P/LVDS_TX0_D0P
- MIPI_DSI_TX0_D0N/LVDS_TX0_D0N
- MIPI_DSI_TX0_D1P/LVDS_TX0_D1P
- MIPI_DSI_TX0_D1N/LVDS_TX0_D1N
- MIPI_DSI_TX0_D2P/LVDS_TX0_D2P
- MIPI_DSI_TX0_D2N/LVDS_TX0_D2N
- MIPI_DSI_TX0_D3P/LVDS_TX0_D3P
- MIPI_DSI_TX0_D3N/LVDS_TX0_D3N
- MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP
- MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN



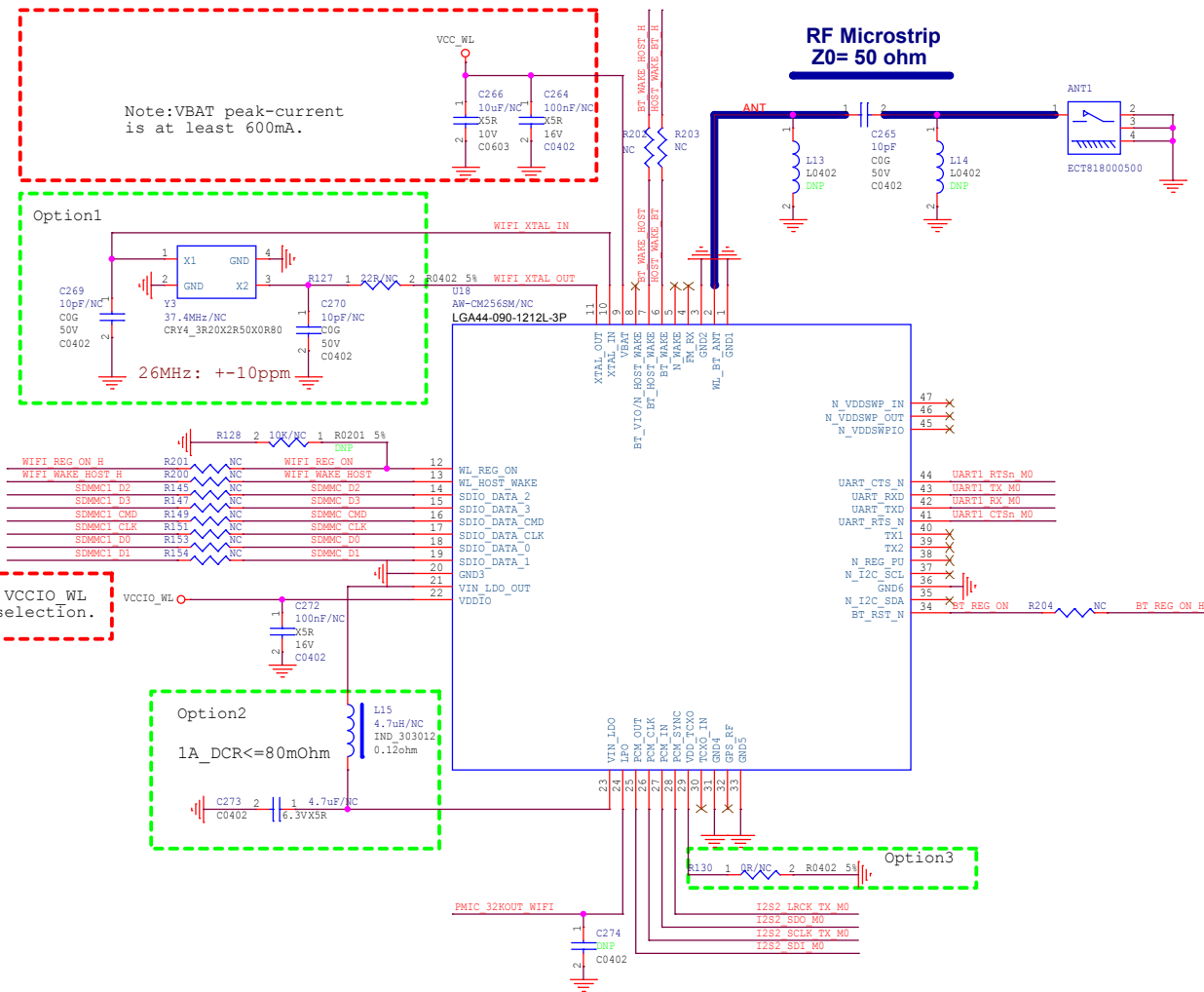
Adjust power supply according to specific panel needs.



		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	26.VO-LCM_MIPI(Single)		
Date:	Friday, March 24, 2023	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	27 of 37

SDIO WIFI/BT Module-1T1R

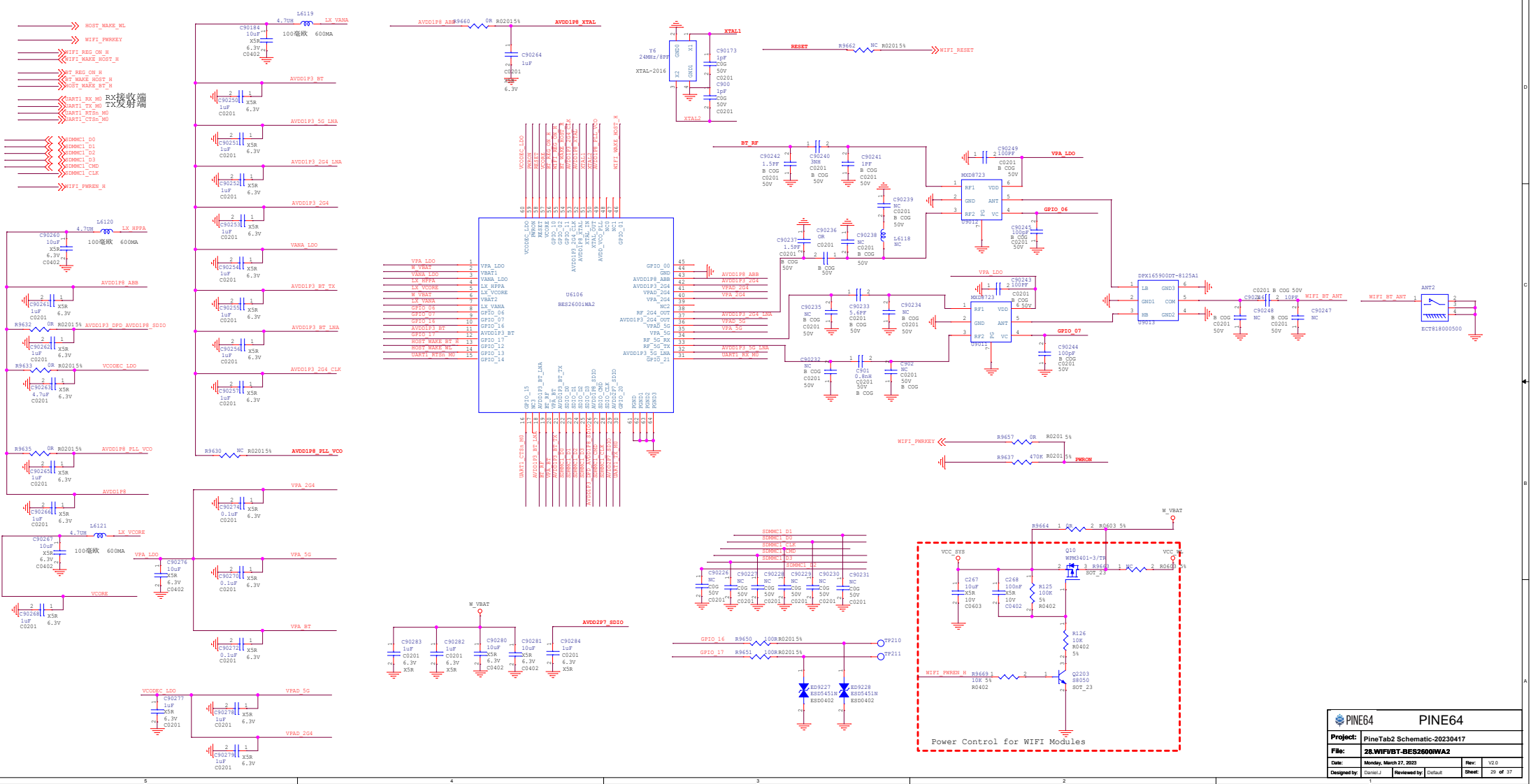
- >>SDMMC1_D0
- >>SDMMC1_D1
- >>SDMMC1_D2
- >>SDMMC1_D3
- >>SDMMC1_CMD
- >>SDMMC1_CLK
- >>WIFI_REG_ON_H
- >>WIFI_WAKE_HOST_H
- >>UART1_RX_M0
- >>UART1_TX_M0
- >>UART1_RTSn_M0
- >>UART1_CTSn_M0
- >>BT_REG_ON_H
- >>BT_WAKE_HOST_H
- >>HOST_WAKE_BT_H
- >>I2S2_SCLK_TX_M0
- >>I2S2_LCKK_TX_M0
- >>I2S2_SDO_M0
- >>I2S2_SDI_M0
- >>PMIC_32KOUT_WIFI



See page22 for VCCIO_WL power connect selection.

Note:
 Yes: option circuit be mounted
 No: option circuit not be mounted

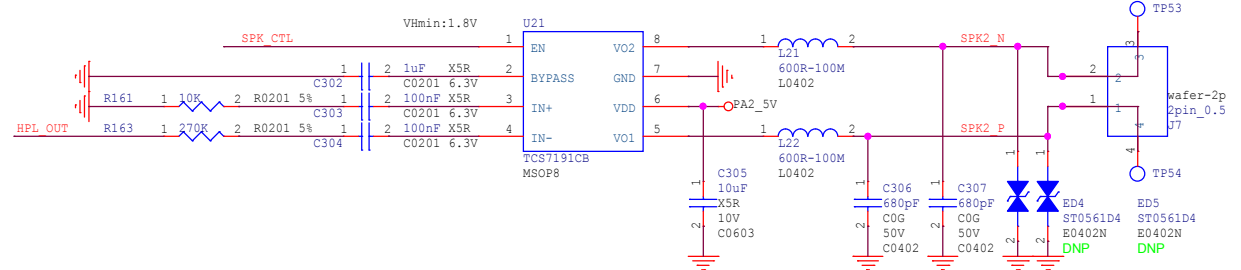
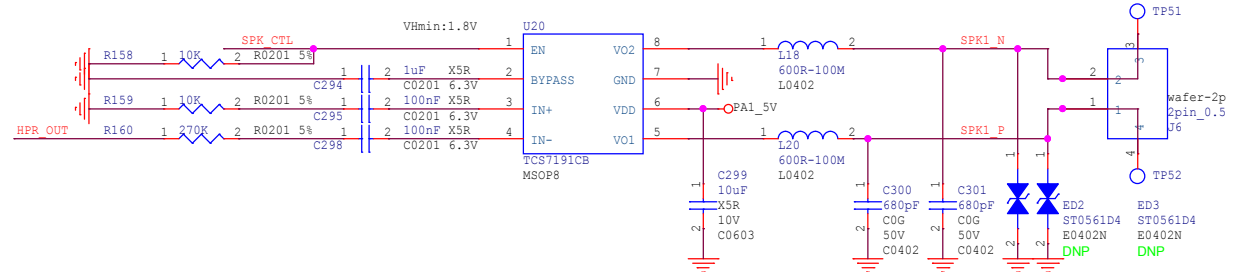
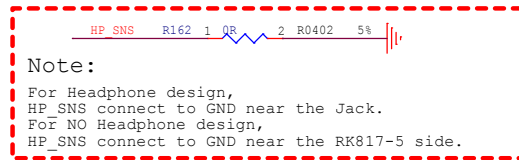
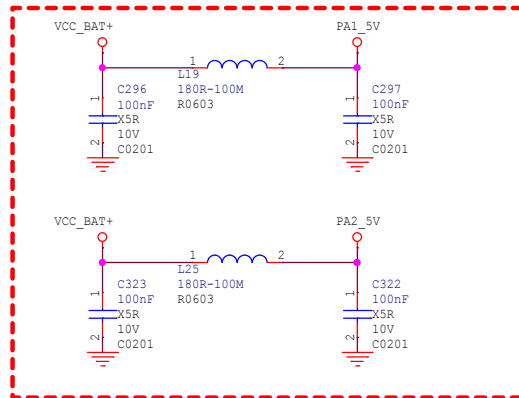
OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3	OPTION4	OPTION5
	a	b/g/n	ac	5GHz								
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	No	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	No	No



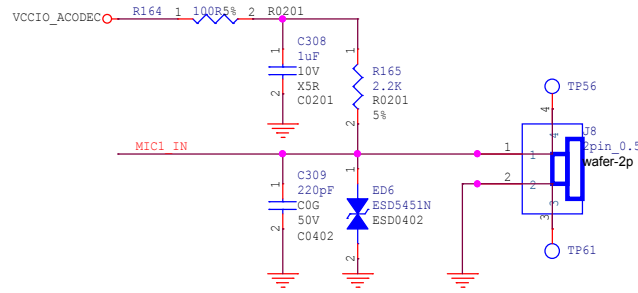
PINE64	
Project: PineTab2 Schematic-20230417	
File: 28.WIFI/VT-BES2600WA2	
Date: Monday, March 27, 2023	Rev: V2.0
Designed by: Daniel	Reviewed by: Default
Sheet: 29 of 37	

- >>> HPL_OUT
- >>> HP_SNS
- >>> HPR_OUT
- >>> SPK_CTL
- <<< MIC1_IN
- <<< MIC2_IN
- <<< HP_DET_L
- <<< SARADC_VIN2_HP_HOOK

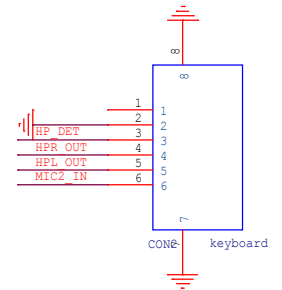
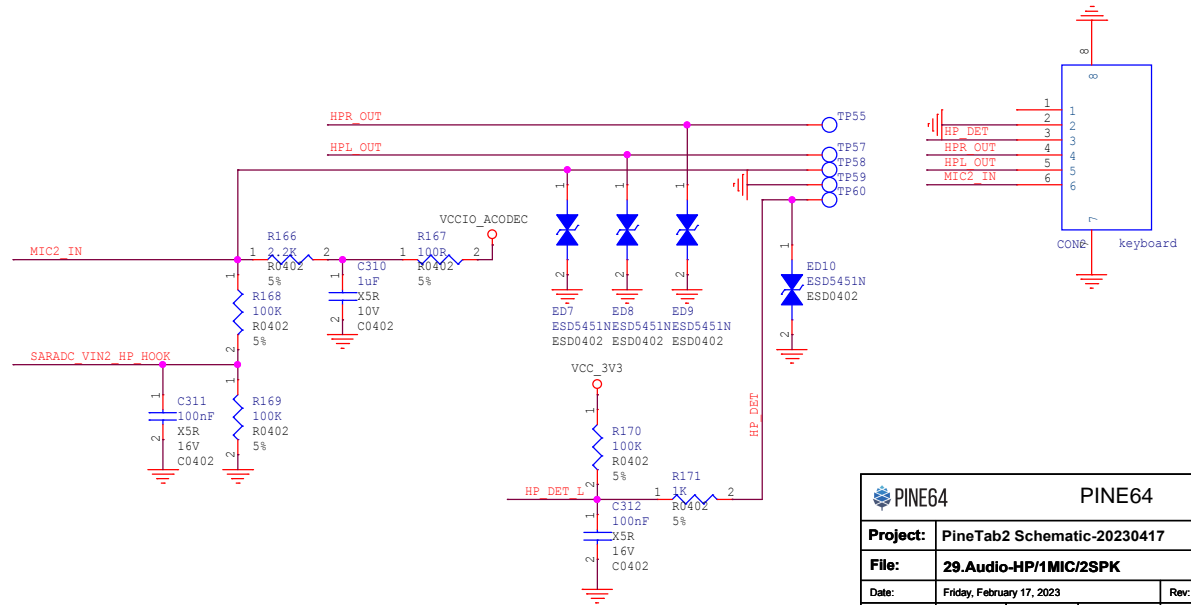
Speaker Output (Stereo)



Microphone Input (Single-ended)



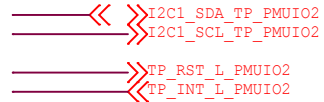
Headphone Jack (4-pole with DET & MIC)



PINE64		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	29.Audio-HP/1MIC/2SPK		
Date:	Friday, February 17, 2023	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
Sheet:	30		of 37

TP COB Connector

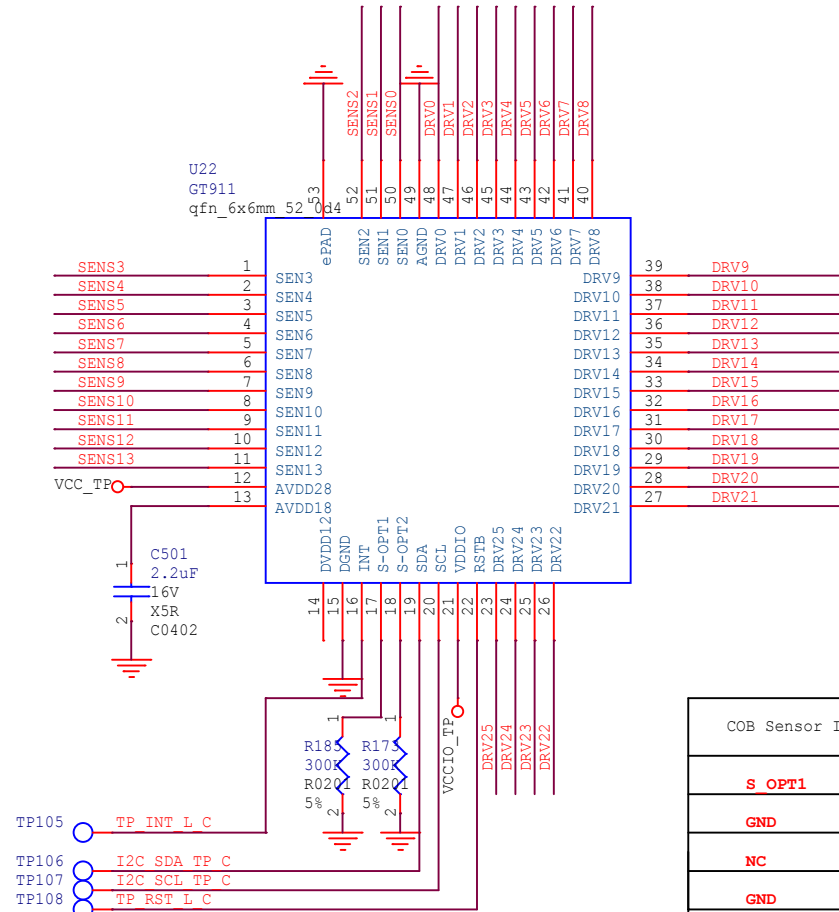
Note: 26x14 channel,
suit for Touch Panel size ≤ 12"



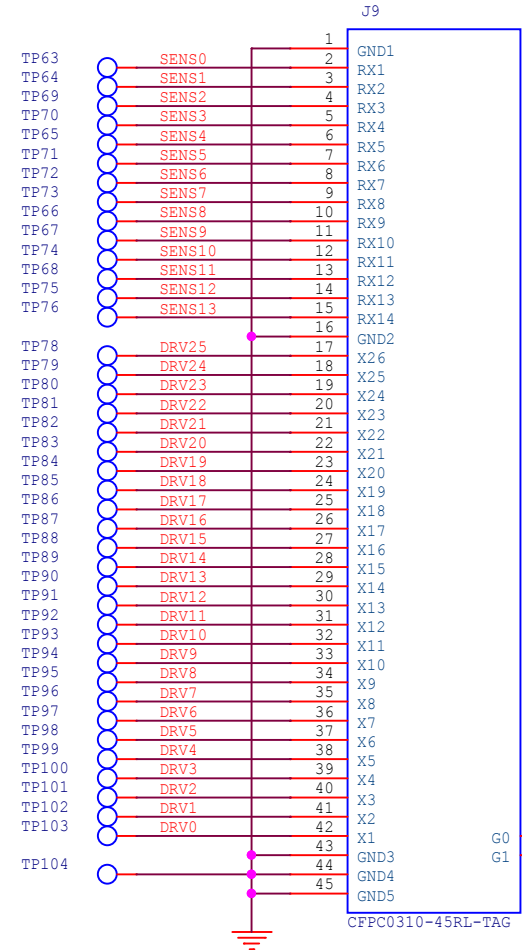
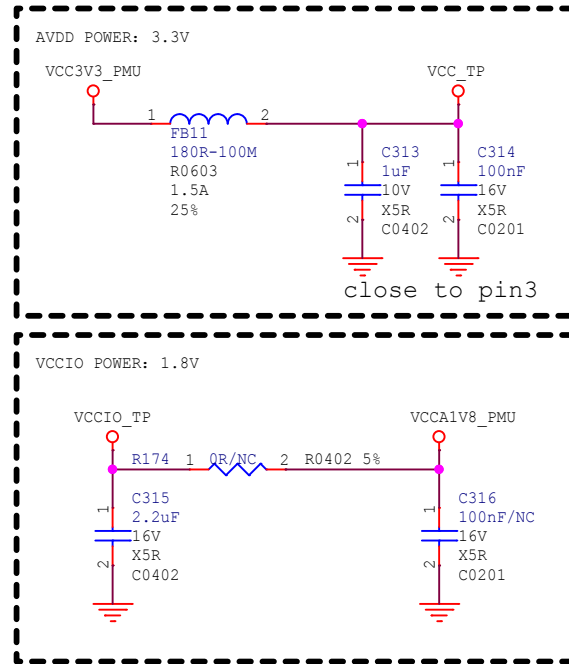
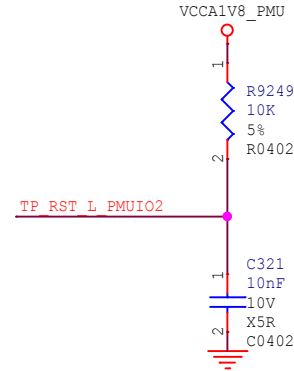
I2C1 SDA TP PMUIO2	R181	1	0R	2	R0201 5%	I2C SDA TP C
I2C1_SCL TP PMUIO2	R182	1	0R	2	R0201 5%	I2C_SCL TP C
TP_RST_L PMUIO2	R183	1	0R	2	R0201 5%	TP_RST L C
TP_INT_L PMUIO2	R184	1	0R	2	R0201 5%	TP_INT L C

default VCCIO=1.8V

Support touch to wake under sleep mode



default VCCIO=1.8V



S OPT1	S OPT1	模组ID
GND	GND	模组1 (默认)
NC	GND	模组3
GND	NC	模组4
NC	NC	模组6

PINE64	
Project:	PineTab2 Schematic-20230417
File:	30.TP_Connector-COB
Date:	Tuesday, November 08, 2022
Rev:	V2.0
Designed by:	Daniel.J
Reviewed by:	Default
Sheet:	31 of 37

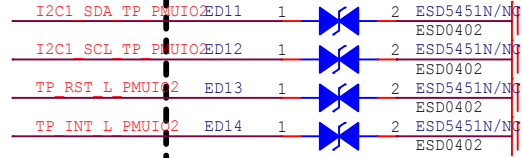
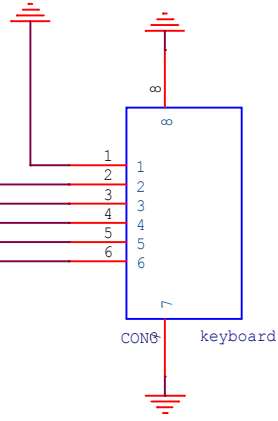
TP COF Connector (option)

I2C1_SDA_TP_PMUIO2
 I2C1_SCL_TP_PMUIO2
 TP_RST_L_PMUIO2
 TP_INT_L_PMUIO2

VCCIO=1.8V

TP_RST_L_PMUIO2
 I2C1_SDA_TP_PMUIO2
 I2C1_SCL_TP_PMUIO2
 TP_INT_L_PMUIO2

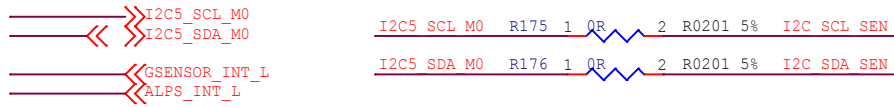
VCC_TP



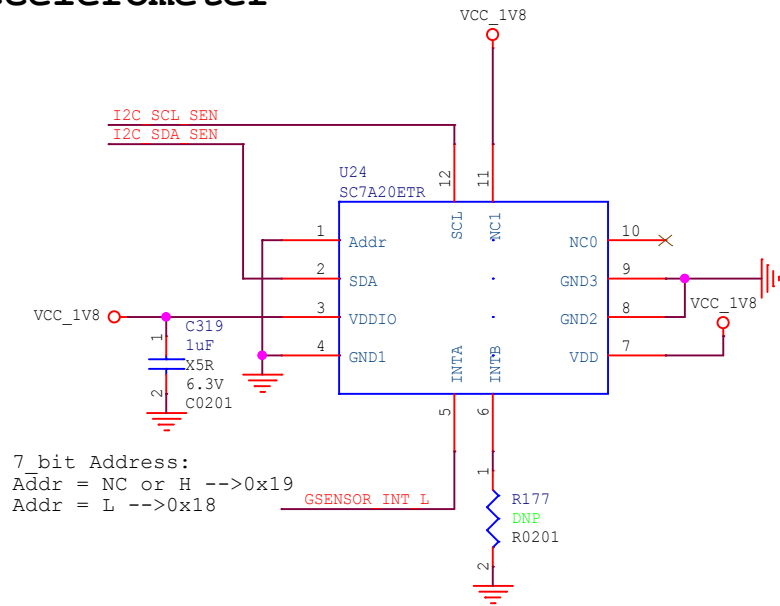
Place ESDs closed to connector

PINE64		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	31.TP_Connector-COF(option)		
Date:	Friday, October 14, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
Sheet:	32 of 37		

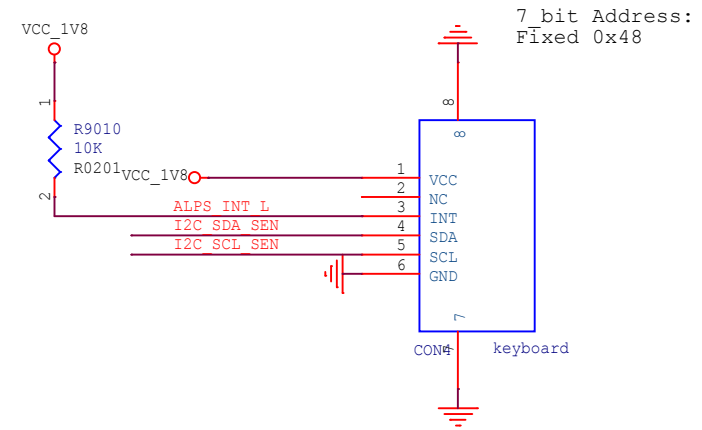
Sensors



Accelerometer



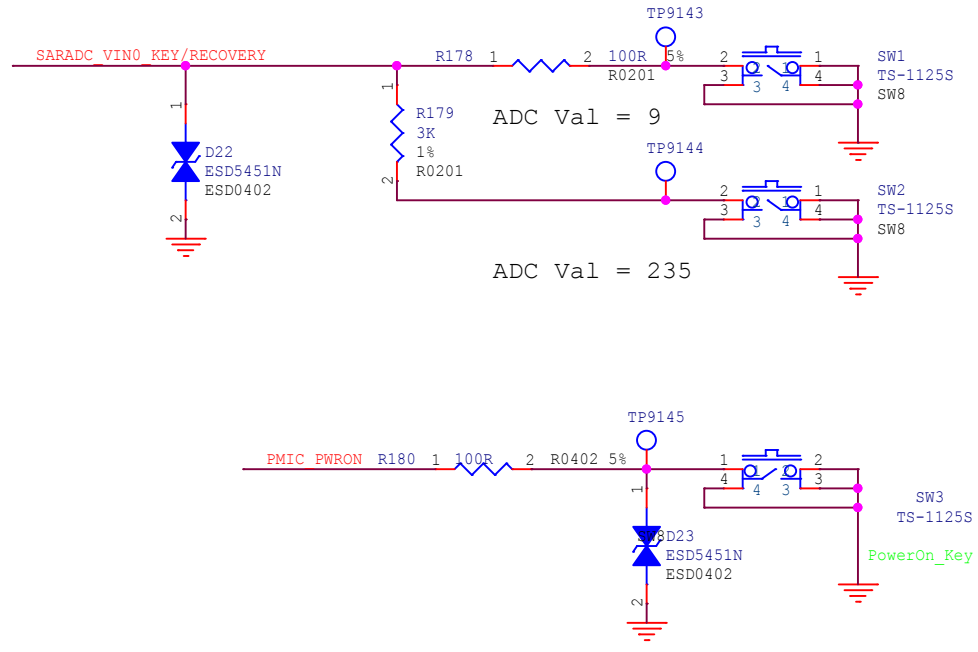
Ambient Light & Proximity Sensor



		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	32.Sensors		
Date:	Tuesday, September 27, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	33 of 37

ADC KEY

<< SARADC_VINO_KEY/RECOVERY
<< PMIC_PWRON



V+/RECOVERY_Key

V-_Key

Key Name	ADC Value
VOL+/RECOVERY	9
VOL-	235

Just as an example.

		<h2>PINE64</h2>	
Project:	PineTab2 Schematic-20230417		
File:	33.KEY_Array/Reset/PWRON		
Date:	Friday, October 14, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	34 of 37

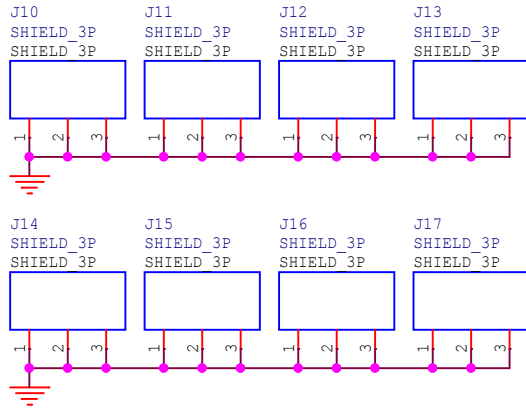
Page of Accessories


PCB Mark Point

Mechanical Hole

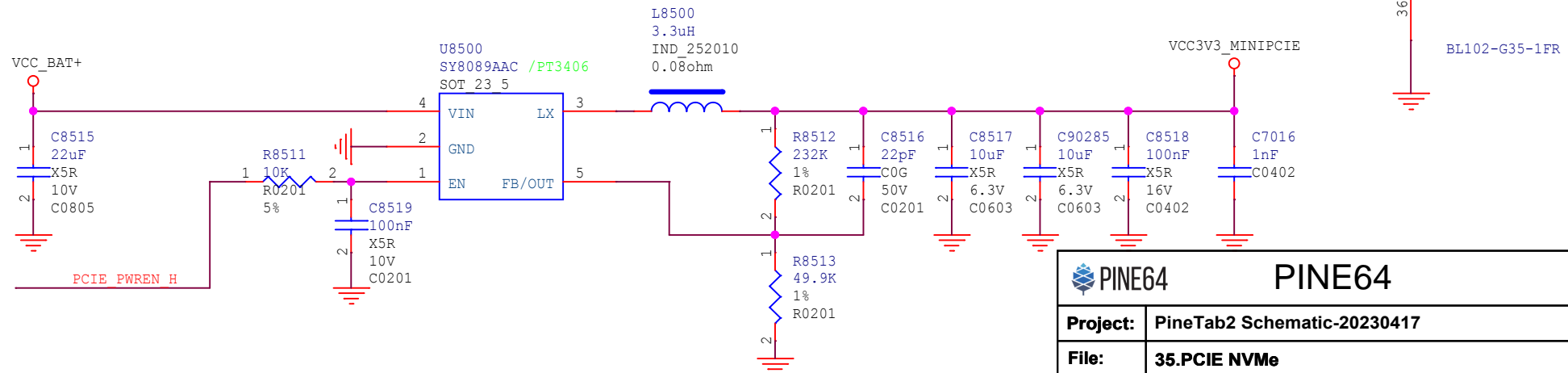
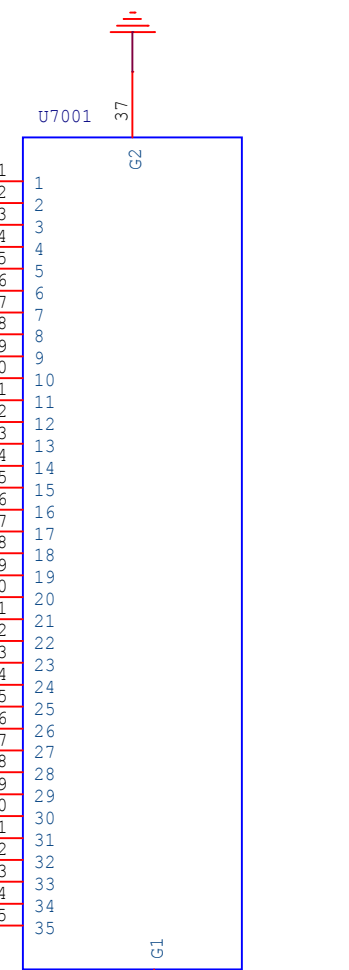
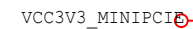
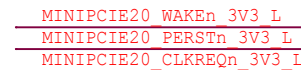
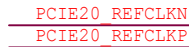
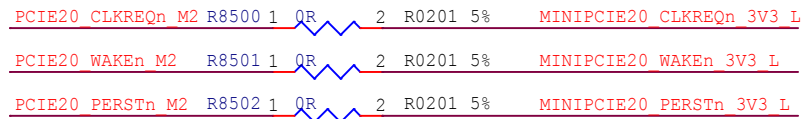
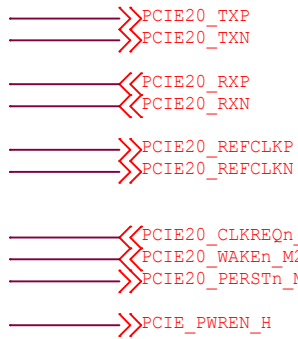
Heatsink

Shield



 PINE64		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	34.Mark/Hole/Heatsink		
Date:	Tuesday, September 27, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	35 of 37

NVMe PCIe 2.0

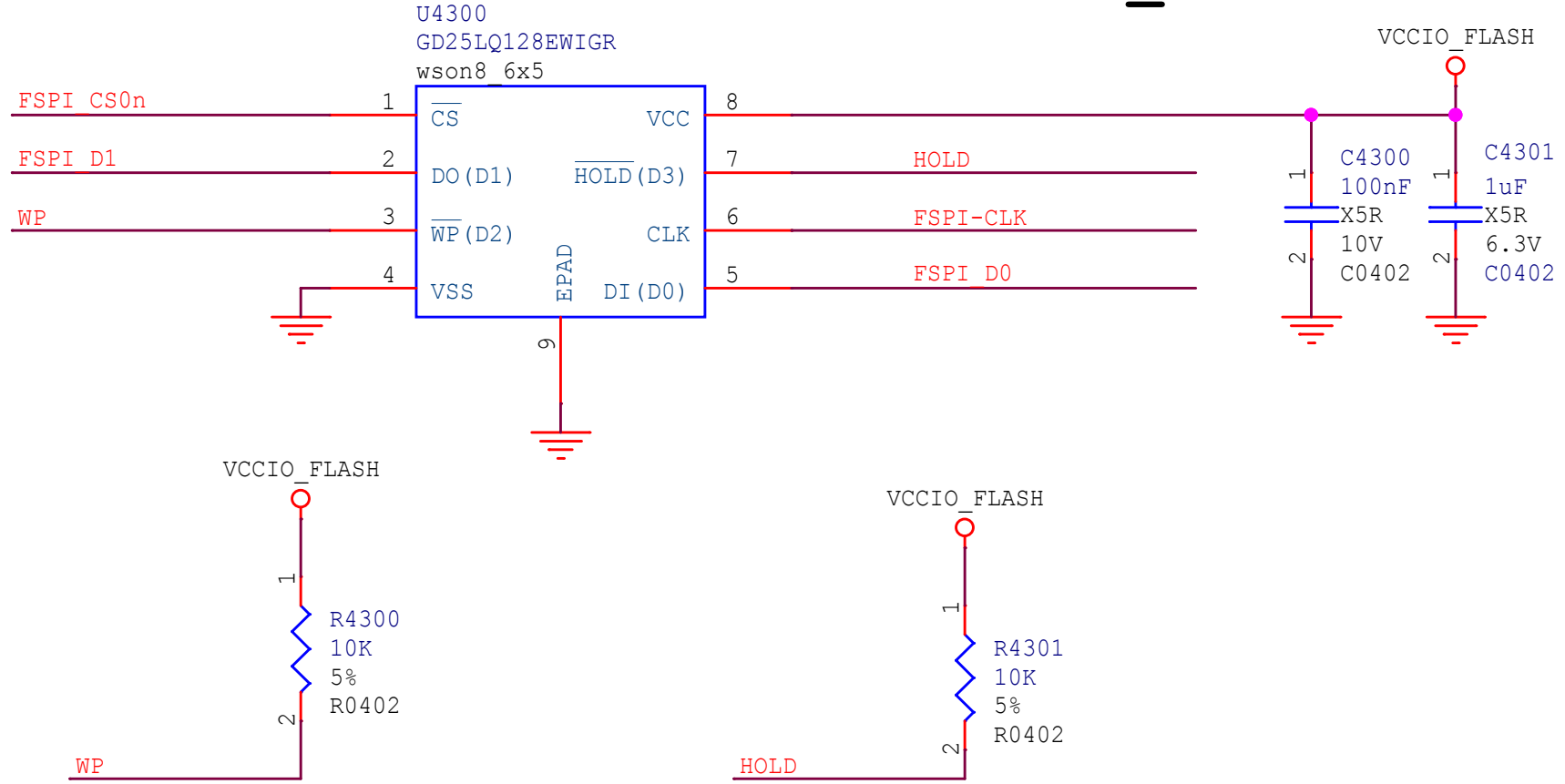



		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	35.PCI2 NVMe		
Date:	Saturday, March 25, 2023	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	36 of 37

Standard SPI FLASH 128M



default VCC = VCCIO_FLASH 1.8V



 PINE64		PINE64	
Project:	PineTab2 Schematic-20230417		
File:	36.Flash-SPI_FLASH		
Date:	Tuesday, September 27, 2022	Rev:	V2.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	37 of 37