PineNote Schematics v1.1

Main Functions Introduction

1) PMIC: RK817-5+Charger+DiscretePower
2) RAM: LPDDR4 1x32Bit(Default:4GB)
3) ROM: eMMC5.1(Default:128GB)
4) Support: Support: 1 x USB2.0 OTG
5) Support: 8Bit/16Bit E-Paper
6) Support: a/b/g/n/ac WIFI, BT5.0
7) Support: Gyroscope-sensor G-sensor M-sensor PS-sensor
8) Support: Speaker out(1.3W@8ohm)
9) Add Console UART thru USB-C port
10) Add internal digital video port

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**00.Cover Page**				
Date:	Tuesday, August 24, 2021			**Rev:**	V1.2
Designed by:	<designer>	**Reviewed by:**	<Checker>	**Sheet:**	0 of 99

Table of Content

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

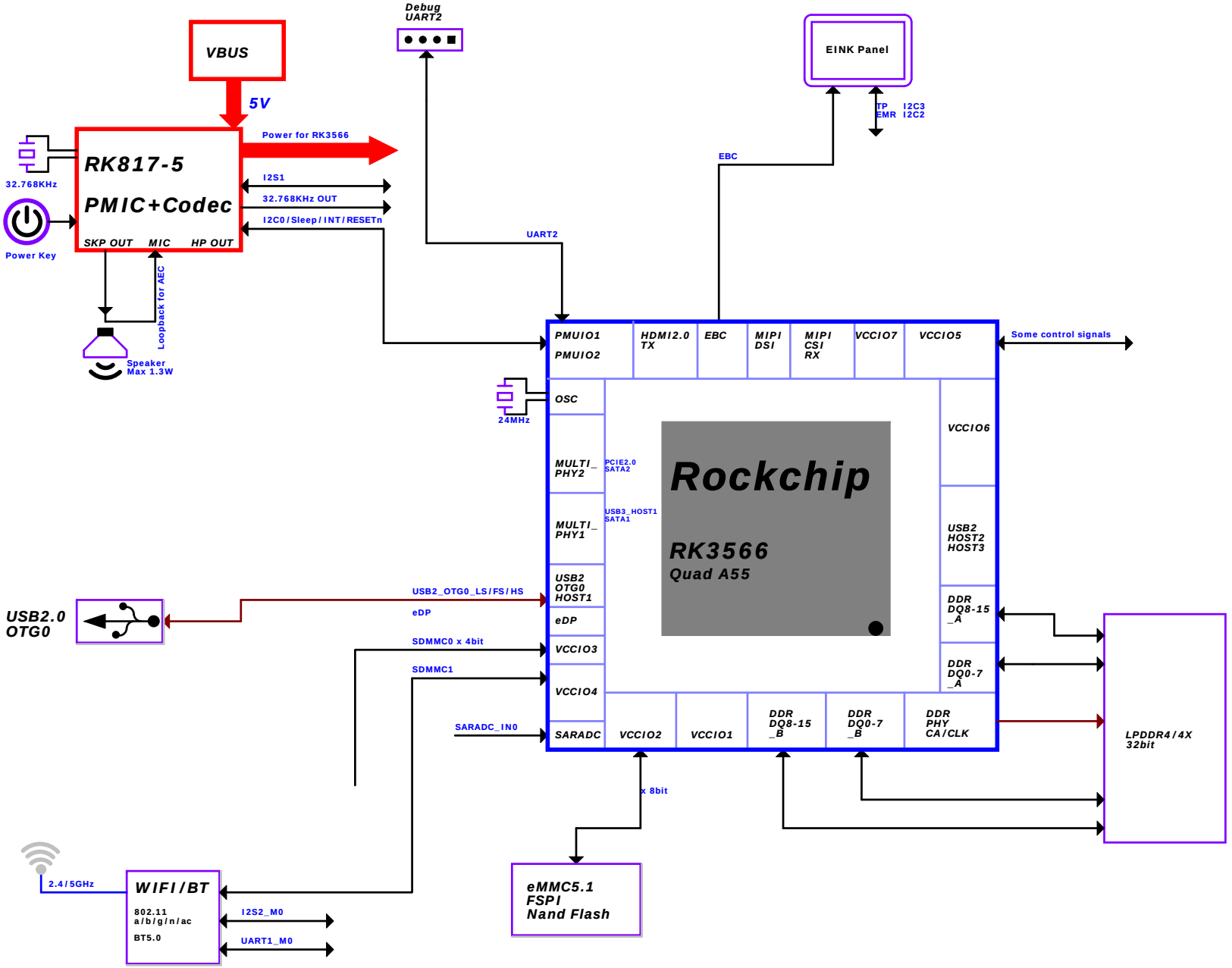
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	01.Index and Notes				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	1 of 99

Revision History

Version	Date	By	Change Dsecription	Approved
V0.1	2020-10-26	ZHM	1: Revision preliminary version	
V1.1	2021-07-26	Pine64	1: PineNote schematic released	

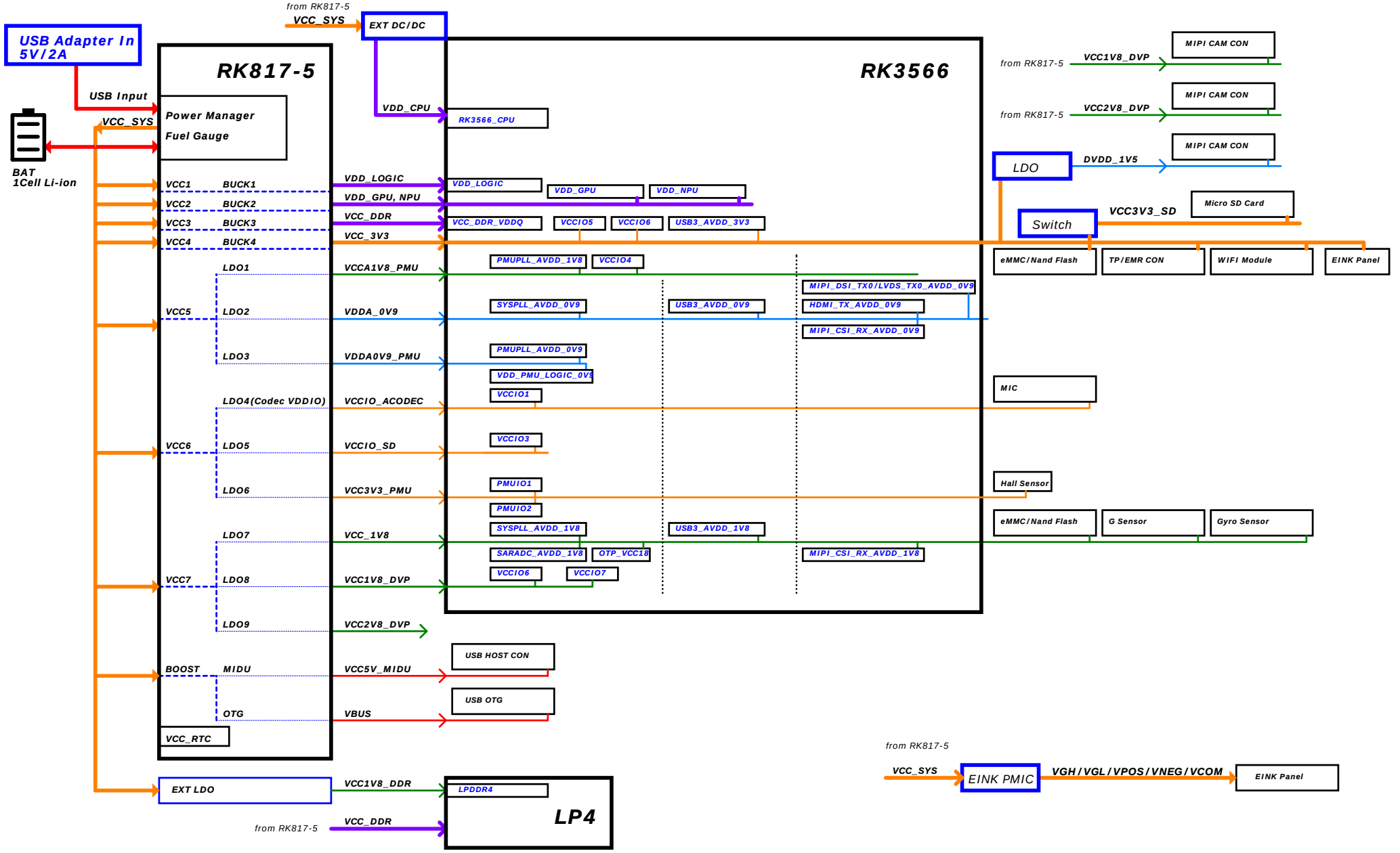
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	02.Revision History				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	2 of 99

RK3566 Ref Block Diagram



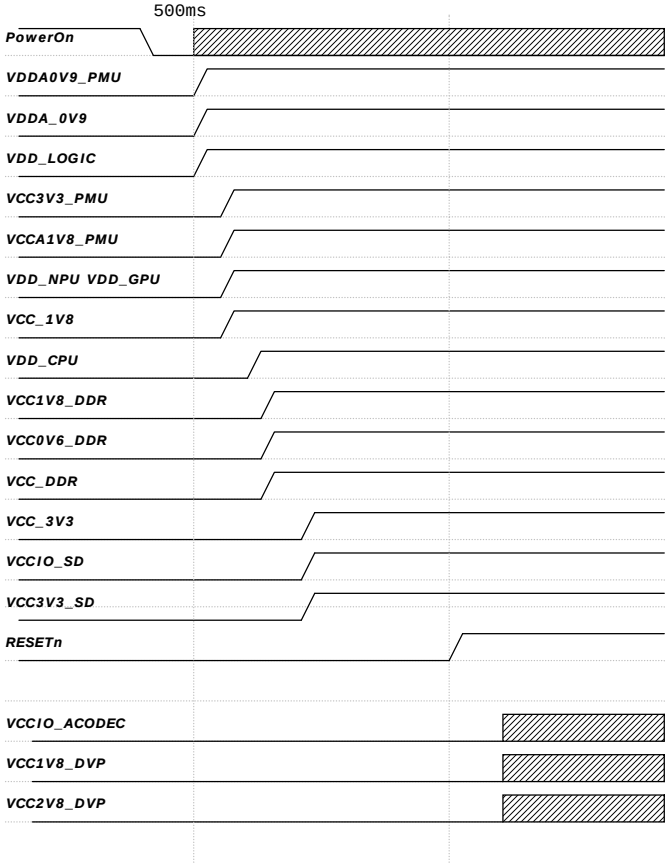
PINE64	
Project:	PineNote Mainboard Schematic-20210824
File:	03.Block Diagram
Date:	Tuesday, August 24, 2021
Rev:	V1.2
Designed by:	Daniel.J
Reviewed by:	Default
Sheet:	3 of 99

Power Diagram



PINE64	
Project:	PineNote Mainboard Schematic-20210824
File:	04.Power Diagram
Date:	Tuesday, August 24, 2021
Rev:	V1.2
Designed by:	Daniel.J
Reviewed by:	Default
Sheet:	4 of 99

Power Sequence &Power Path assignment



Power Source	PMIC Channel	Supply Limit	Power Supply Name	Time Slot	Default Voltage	Work Status	Sleep Status
VCC_SYS	RK817-5_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_BUCK2	2.5A	VDD_NPU,VDD_GPU	Slot:2	0.9V	ON	OFF
VCC_SYS	RK817-5_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON
VCC_SYS	RK817-5_BUCK4	1.5A	VCC_3V3	Slot:4	3.3V	ON	OFF
VCC_SYS	RK817-5_LDO1	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON
	RK817-5_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF
	RK817-5_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_LDO4	0.4A	VCCIO_ACODEC	N/A	1.8V	ON	OFF
	RK817-5_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF
	RK817-5_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON
VCC_SYS	RK817-5_LDO7	0.4A	VCC_1V8	Slot:2	1.8V	ON	OFF
	RK817-5_LDO8	0.4A	VCC1V8_DVP	N/A	1.8V	ON	OFF
	RK817-5_LDO9	0.4A	VCC2V8_DVP	N/A	2.8V	ON	OFF
VCC_BAT	RK817-5_RESETn			Slot:4+5			
VCC_BAT	RK817-5_BOOST RK817-5_OTG	1.5A	VCC5V_MIDU VBUS	N/A	5.0V	ON	OFF
VCC_3V3	Switch		VCC3V3_SD	Slot:4	3.3V	ON	OFF
VCC_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF

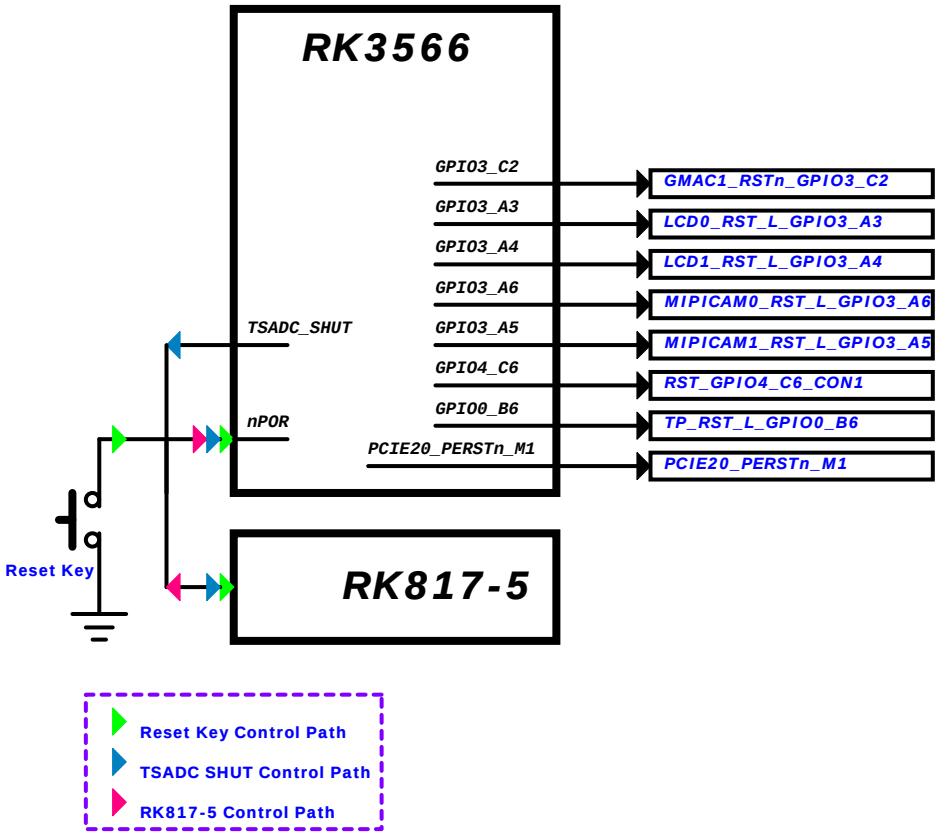
IO Power Domain Map

Refer to the actual design!

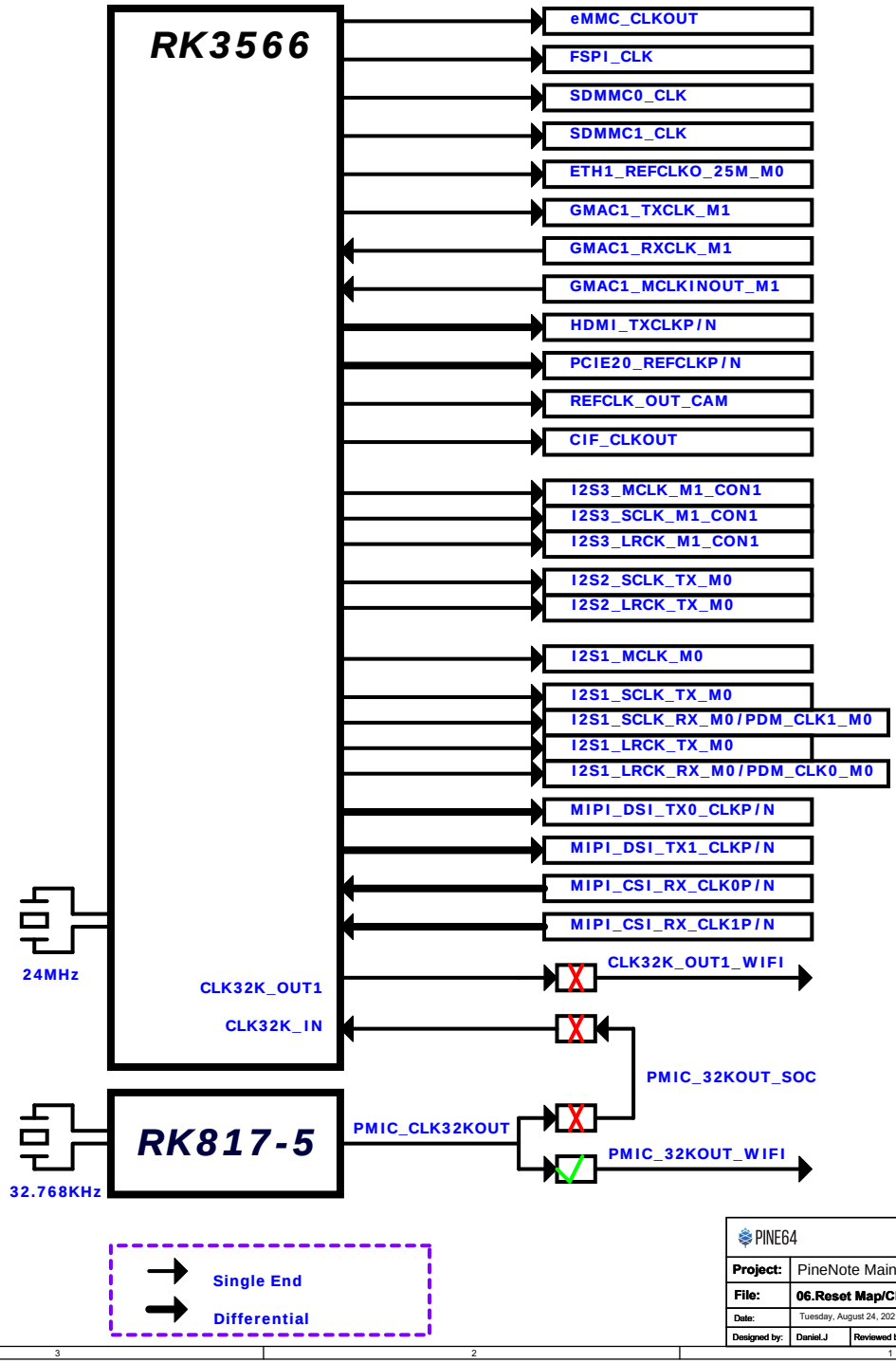
IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO4	VCC1V8_PMU	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_3V3	3.3V	
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC_3V3	3.3V	
VCCIO7	1N8	YES	YES	VCCIO7	VCC1V8_DVP	1.8V	

PINE64	PINE64		
Project:	PineNote Mainboard Schematic-20210824		
File:	05.Power Sequence/IO Domain Map		
Date:	Tuesday, August 24, 2021	Rev:	V1.2
Designed by:	Daniel.J / Reviewed by: Default	Sheet:	5 of 99

RESET Signal MAP

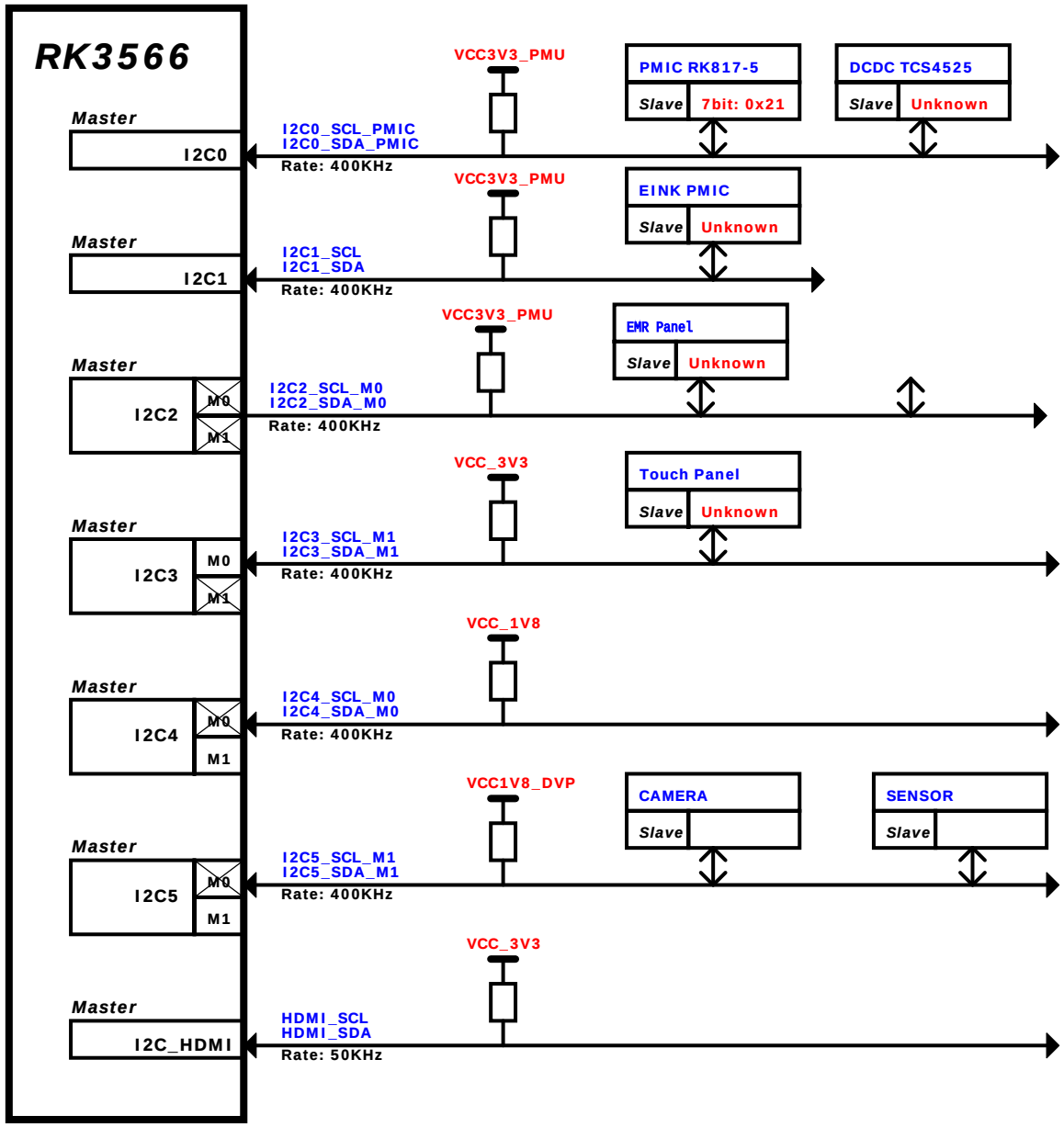


Clock Map



PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	06.Reset Map/Clock Map				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	6 of 99

I2C MAP

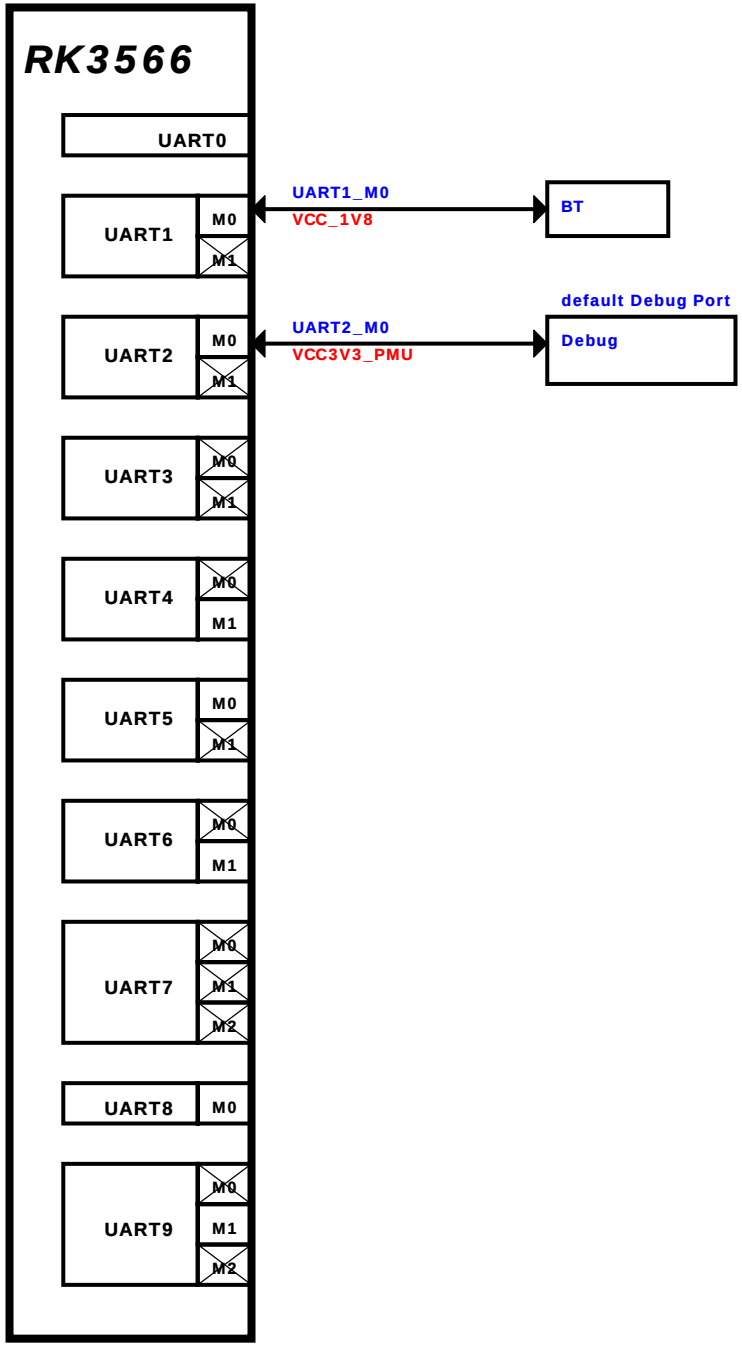


M0 Unselected IOmux path

M1 IOmux path in use

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	07.I2C Bus Map				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	7 of 99

UART MAP

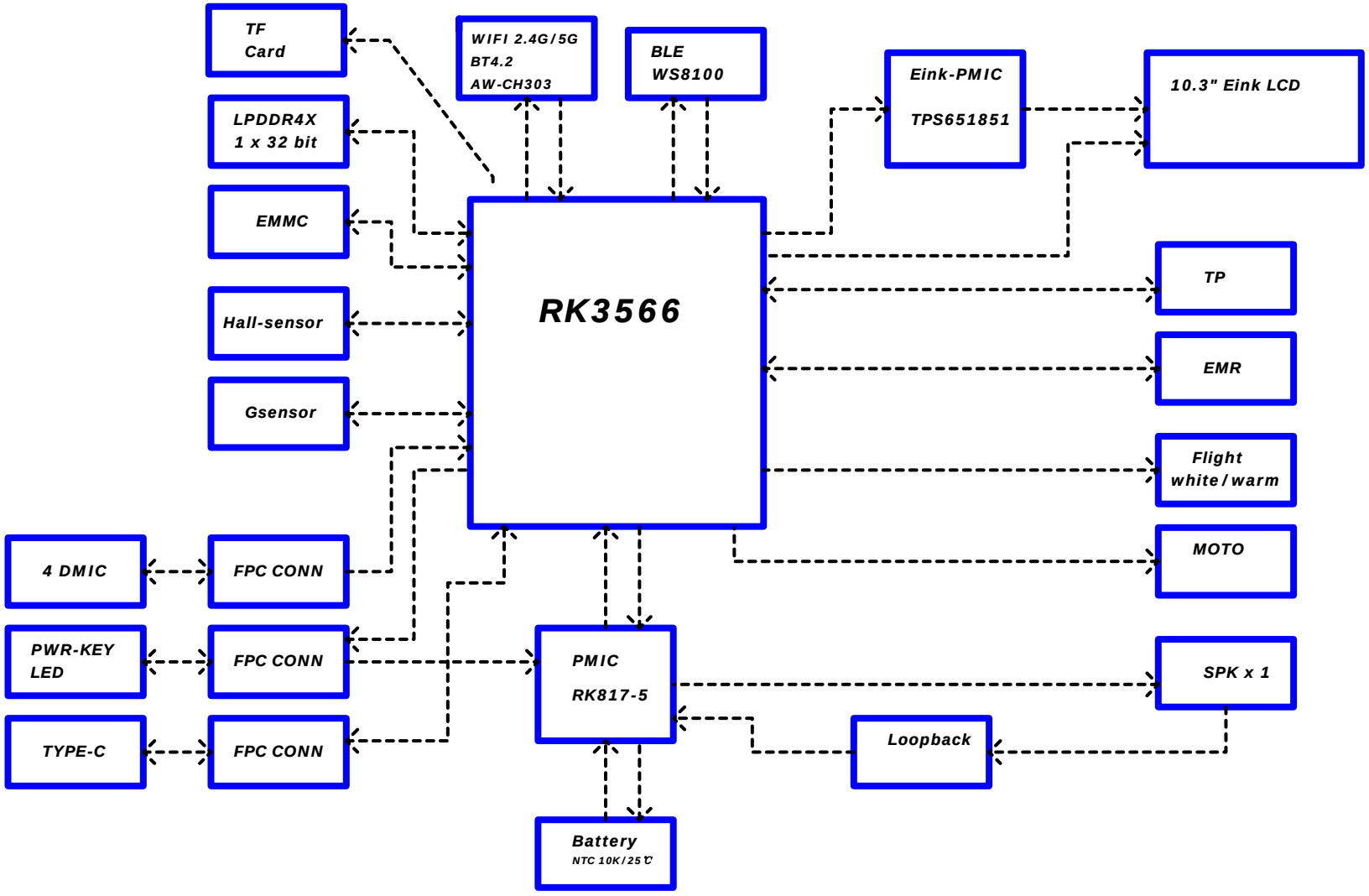


UART1_M0
VCC_1V8
BT

default Debug Port
UART2_M0
VCC3V3_PMU
Debug

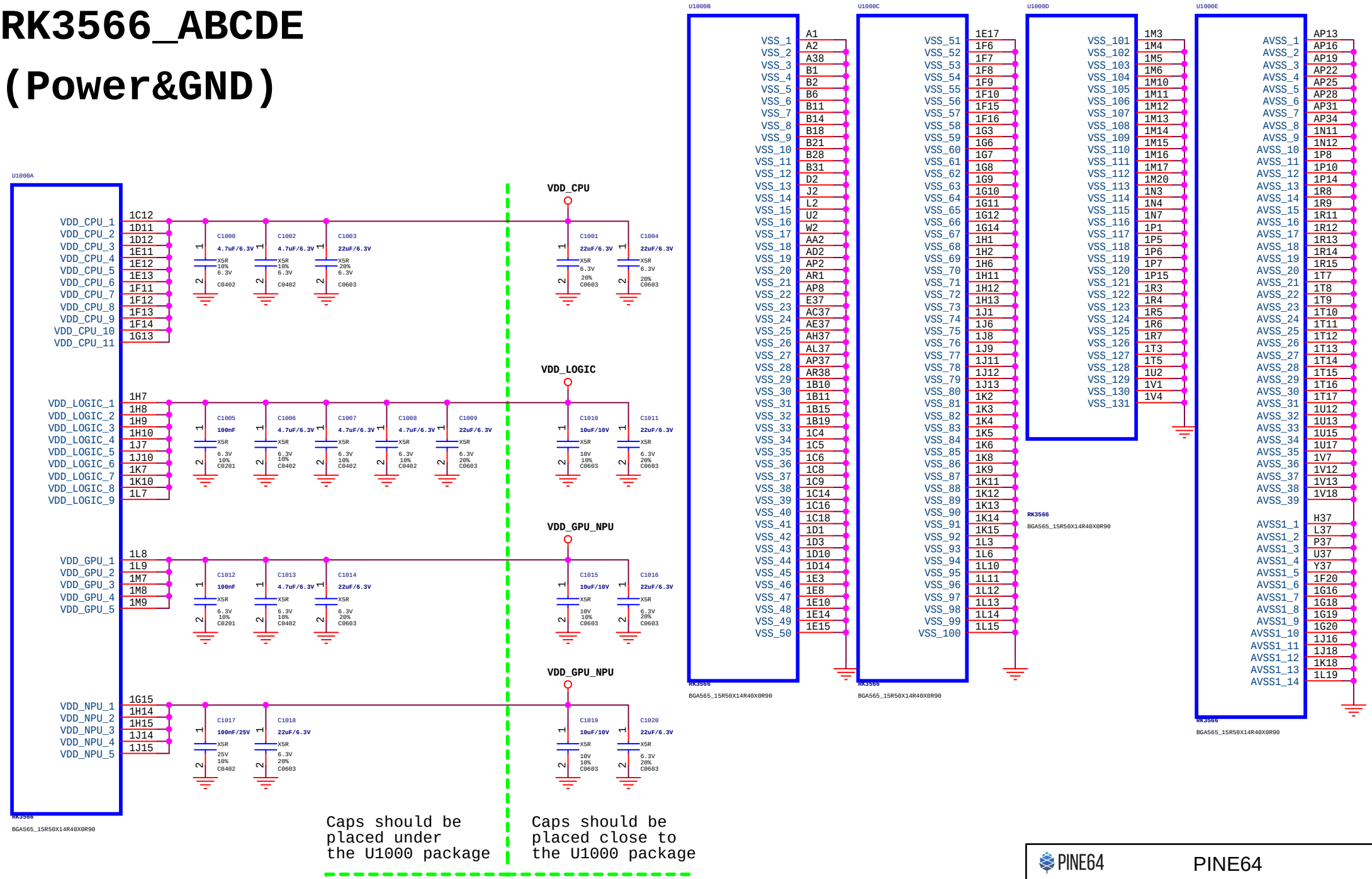
M0 Unselected IOmux path
M1 IOmux path in use

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	08.UART Map				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	8 of 99



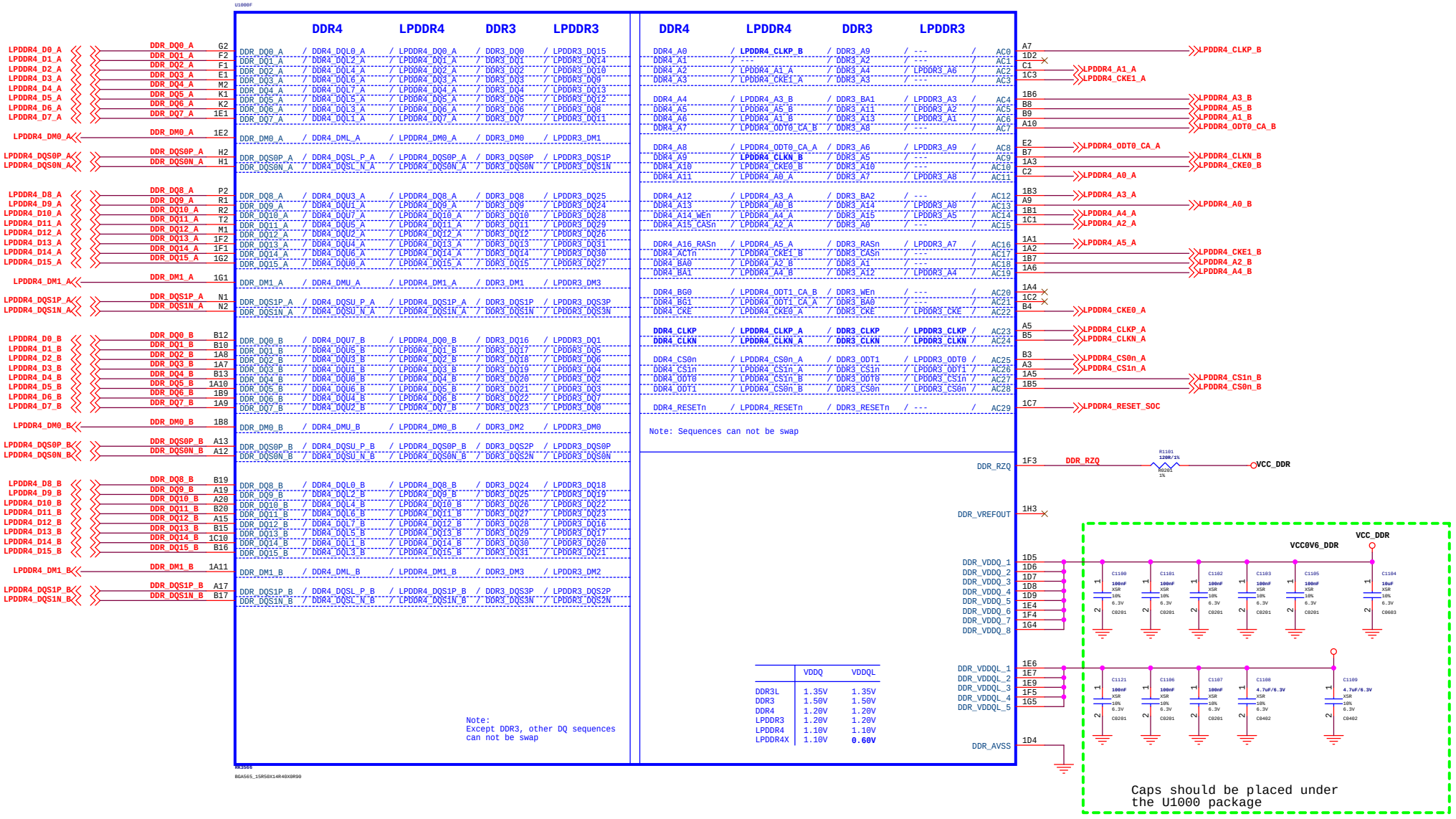
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	09. Diangram				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	9 of 99

RK3566_ABCDE (Power&GND)



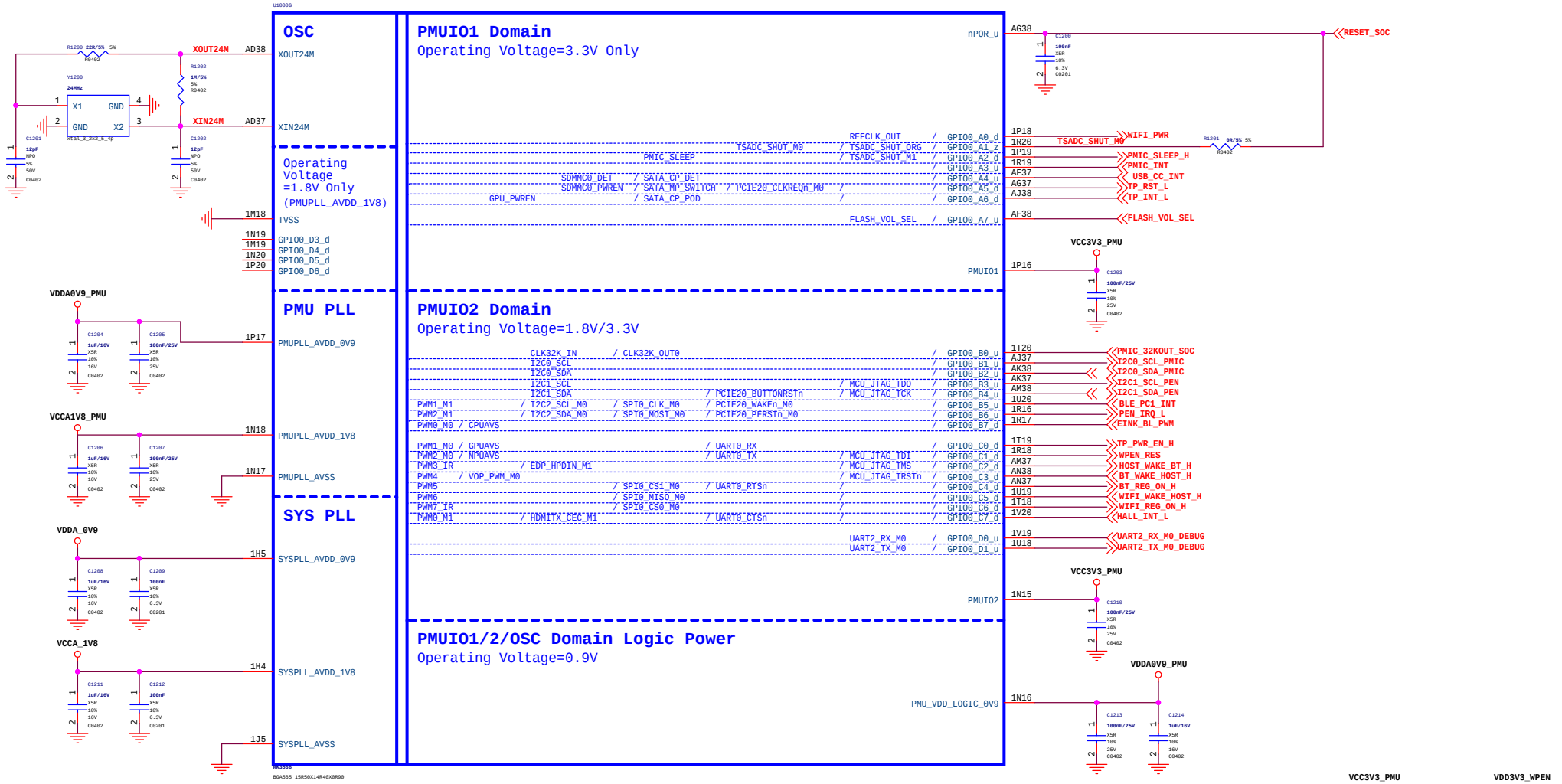
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**10.RK3566_Power/GND**				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	10 of 99

RK3566_F (DDR PHY)



PINE64	PINE64
Project:	PineNote Mainboard Schematic-20210824
File:	**11.RK3566_DDR PHY**
Date:	Tuesday, August 24, 2021
Rev:	V1.2
Designed by:	Daniel.J
Reviewed by:	Default
Sheet:	11 of 99

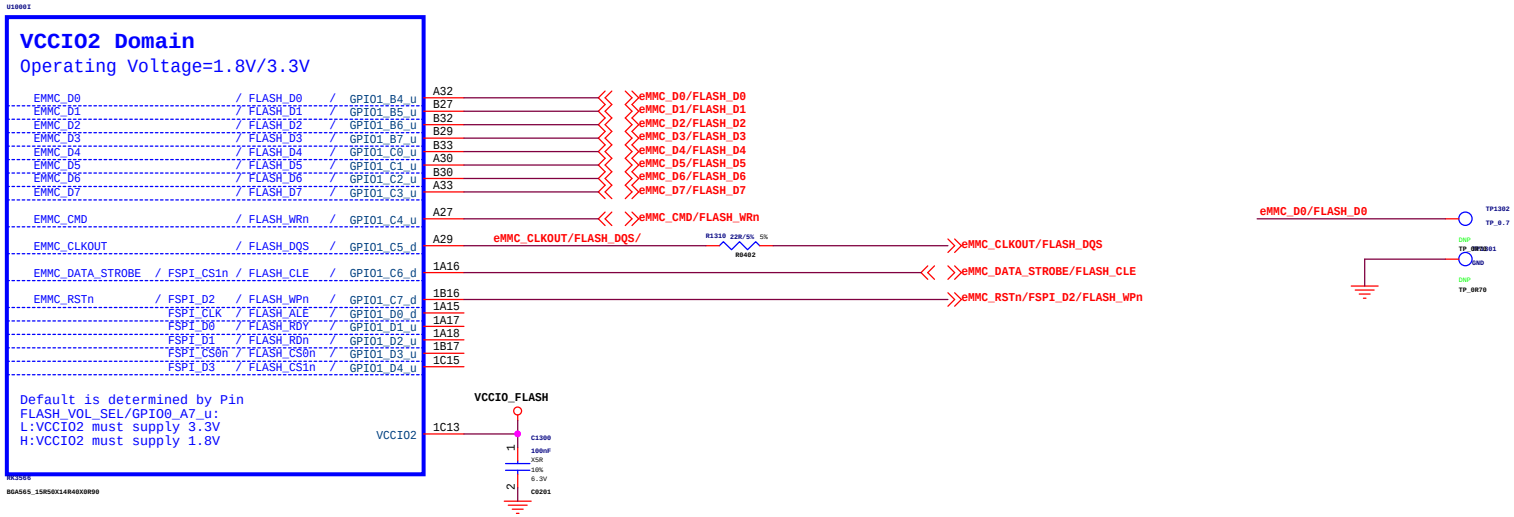
RK3566_G(OSC/PLL/PMUIO1/2)



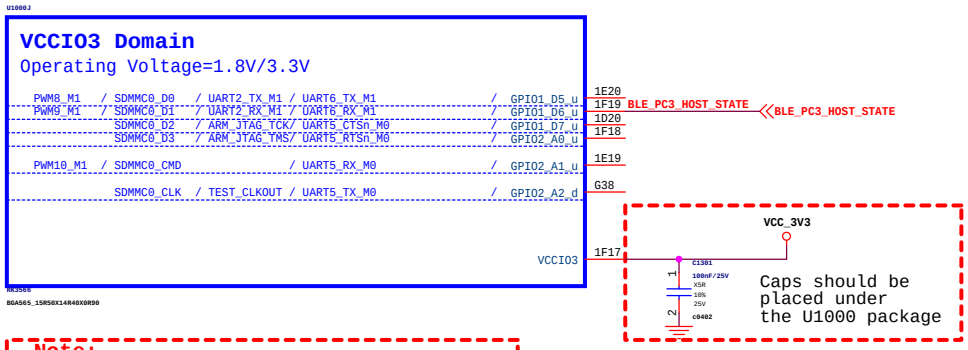
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	12.RK3566_OSC/PLL/PMUIO				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	12 of 99

RK3566_I(VCCIO2 Domain)



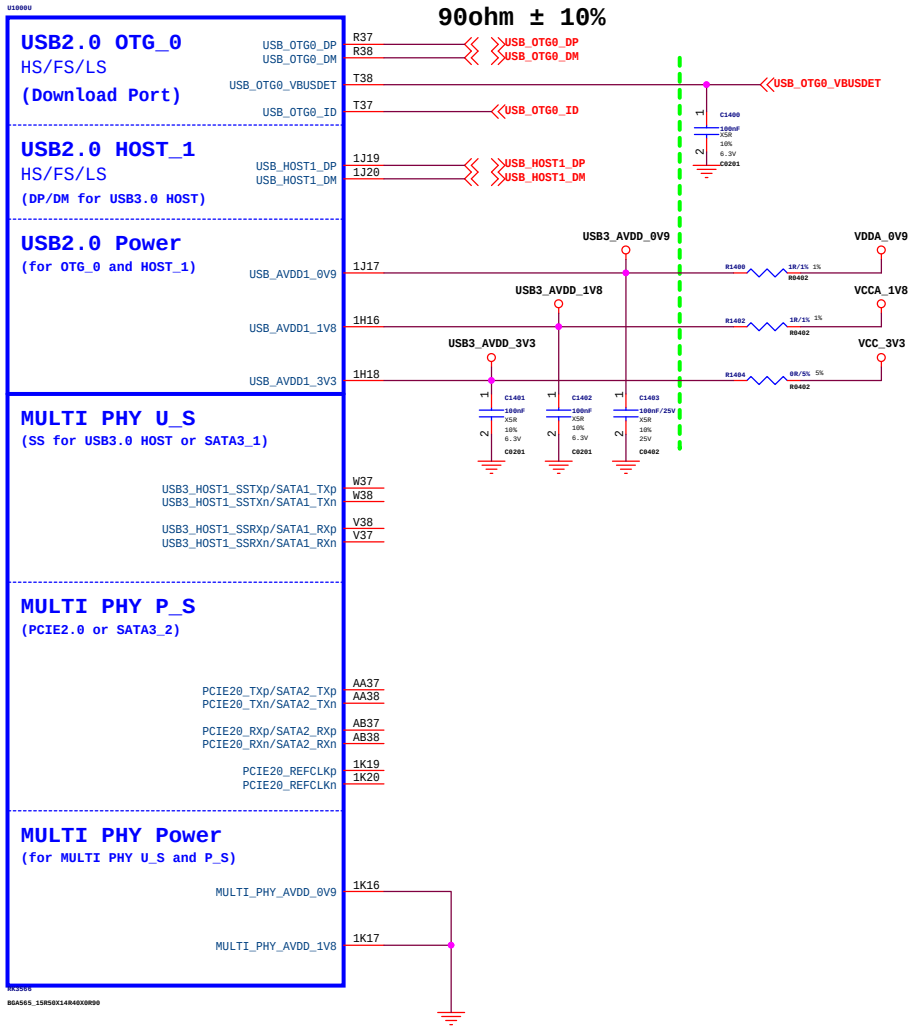
RK3566_J(VCCIO3 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

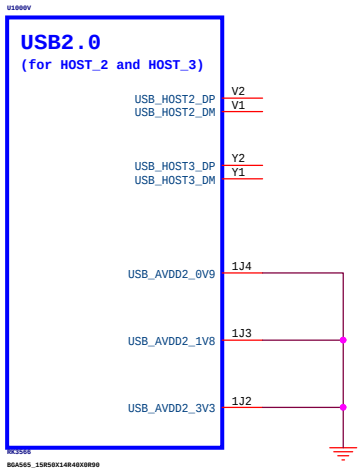
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**13.RK3566_Flash/SD Controller**				
Date:	Tuesday, August 24, 2021			**Rev:**	V1.2
Designed by:	Daniel.J	**Reviewed by:**	Default	**Sheet:**	13 of 99

RK3566_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



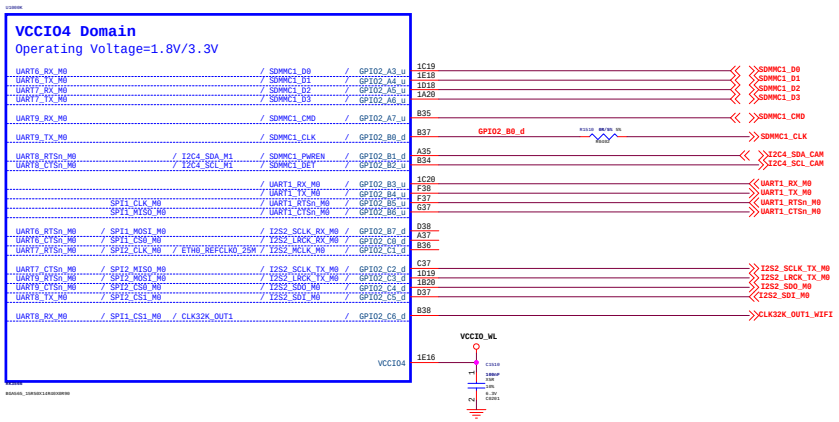
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3566_V(USB2.0 HOST)



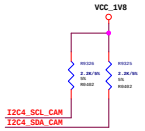
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	14.RK3566_USB/PCIe/SATA PHY				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	14 of 99

RK3566_K(VCCIO4 Domain)



For WIFI

For BT



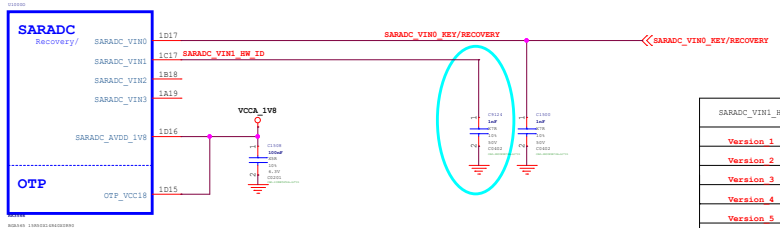
For BT

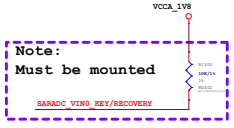
RK3566_N(VCCIO7 Domain)

For 4G

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

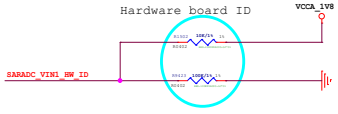
RK3566_O(SARADC/OTP)





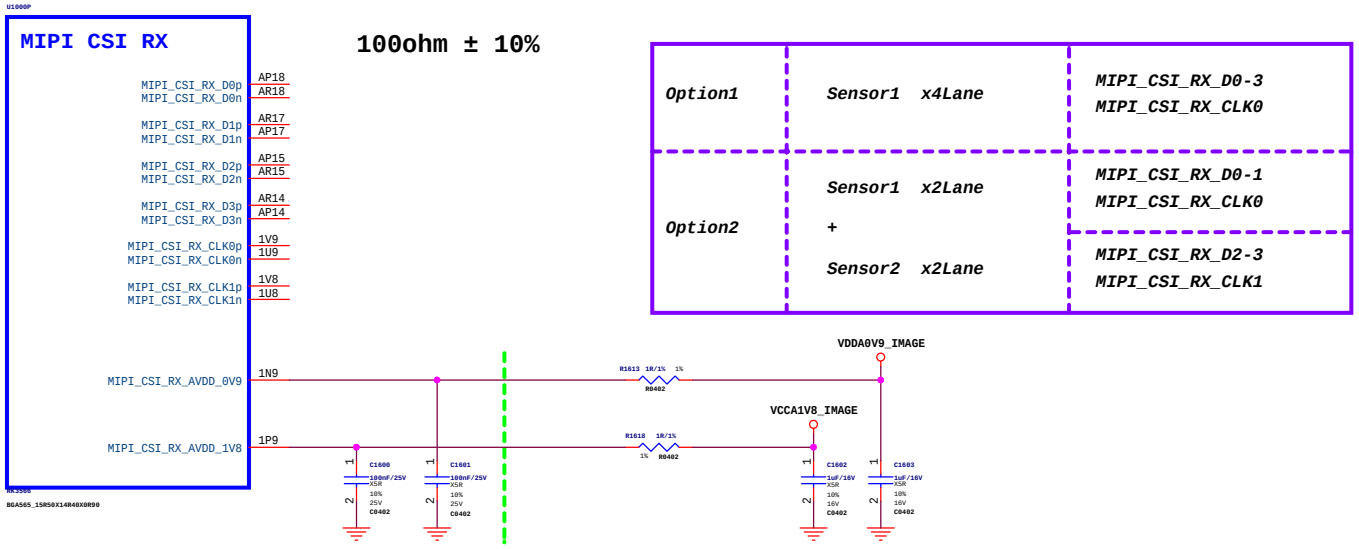
SARADC_VIN1_HW_ID	Rup	Rdown	ADC	
Version_1	10K	DNP	1023	1.8V
Version_2	20K	100K	852	1.5V
Version_3	18K	36K	681	1.2V
Version_4	51K	51K	512	0.9V
Version_5	36K	18K	340	0.6V
Version_6	100K	20K	170	0.3V
Version_7	DNP	10K	0	0V

Hardware board ID

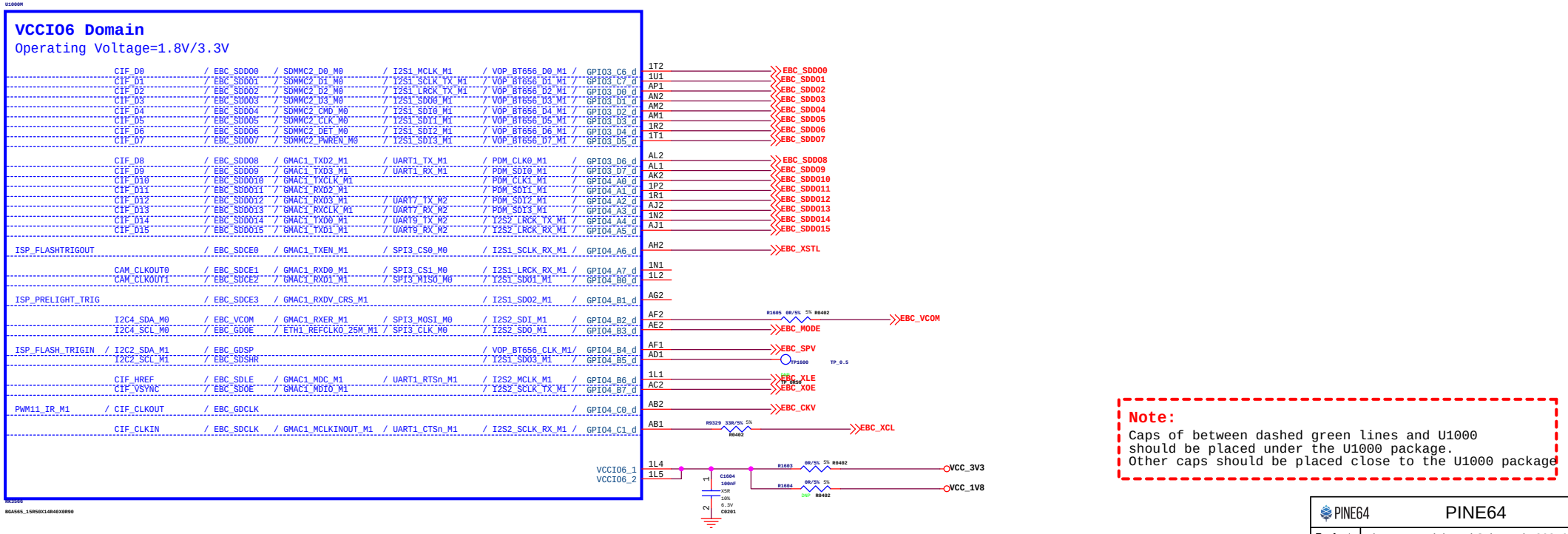


PINE64					
Project:	PineNote Mainboard Schematic-20210824				
File:	15.RK3566_SARADC/GPIO				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	15 of 99

RK3566_P(MIPI_CSI_RX)



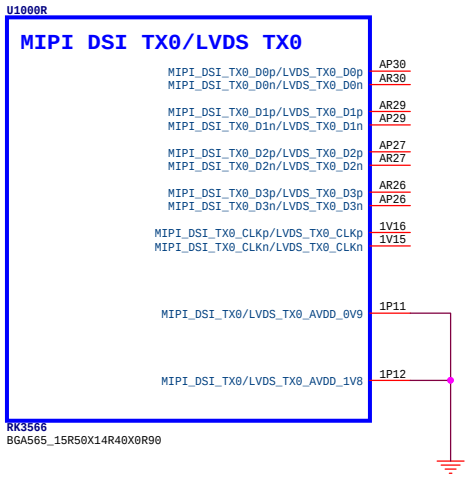
RK3566_M(VCCIO6 Domain)



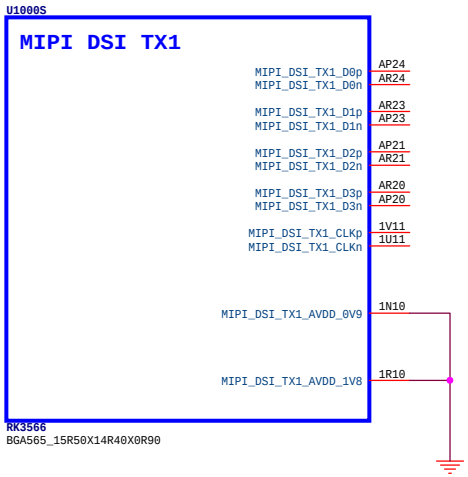
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	16.RK3566_VI Interface				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	16 of 99

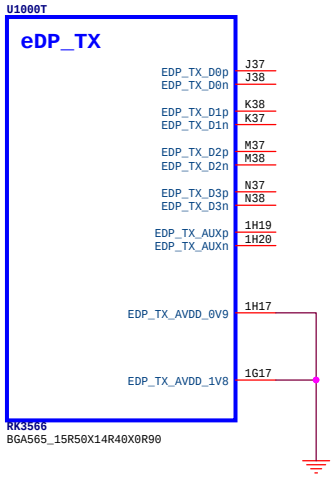
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



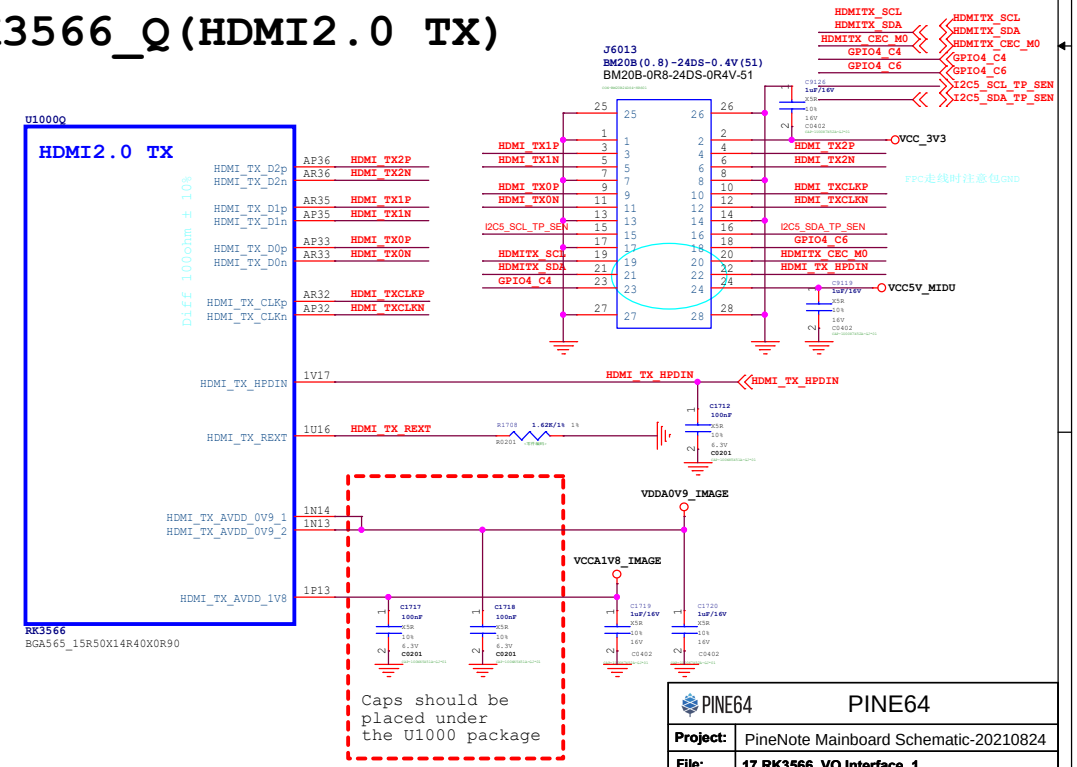
RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP/DP TX)



RK3566_Q(HDMI2.0 TX)



PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	17.RK3566_VO Interface_1				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	17 of 99

RK3566_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

	VOP_BT1120_D0	/ SPI1_CS0_M1		/ SDMMC2_D0_M1	/ GPIO3_A1_d
	VOP_BT1120_D1		/ GMAC1_TXD2_M0 / I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
	VOP_BT1120_D2		/ GMAC1_TXD3_M0 / I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
	VOP_BT1120_D3		/ GMAC1_RXD2_M0 / I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
	VOP_BT1120_D4		/ GMAC1_RXD3_M0 / I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
	VOP_BT1120_CLK		/ GMAC1_TXCLK_M0 / I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
	VOP_BT1120_D5		/ GMAC1_RXCLK_M0	/ SDMMC2_DET_M1	/ GPIO3_A7_d
	VOP_BT1120_D6		/ ETH1_REFCLKO_25M_M0	/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
PWM8_M0	/ VOP_BT1120_D7		/ GMAC1_RXD0_M0 / UART4_RX_M1		/ GPIO3_B1_d
PWM9_M0	/ VOP_BT1120_D8		/ GMAC1_RXD1_M0 / UART4_TX_M1		/ GPIO3_B2_d
	VOP_BT1120_D9	/ I2C5_SCL_M0	/ GMAC1_RXDV_CRS_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
	VOP_BT1120_D10	/ I2C5_SDA_M0	/ GMAC1_RXER_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
PWM10_M0	/ VOP_BT1120_D11	/ I2C3_SCL_M1	/ GMAC1_TXD0_M0		/ GPIO3_B5_d
PWM11_IR_M0	/ VOP_BT1120_D12	/ I2C3_SDA_M1	/ GMAC1_TXD1_M0		/ GPIO3_B6_d
PWM12_M0			/ GMAC1_TXEN_M0 / UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
PWM13_M0			/ GMAC1_MCLKINOUT_M0 / UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
	VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
	VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
	VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0		/ VOP_PWM_M1	/ GMAC1_MDC_M0 / UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0		/ SPDIF_TX_M1	/ GMAC1_MDIO_M0 / UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3566

BGA565_15R50X14R40X0R90

1U5 Enc_CLK
AR10 Enc_CS
AP10 Enc_DAT
AR9 TF_CARD_DET
AP9 EBC_PMIC_WAKEUP
1U4 EBC_PMIC_INT
1V3 EBC_PMIC_PG
AR7 EBC_PMIC_ON
AP7 EBC_PWR_EN
AR6 GSENSOR_INT_L
AP6 I2C5_SCL_TP_SEN
1U3 I2C5_SDA_TP_SEN
1T4 I2C3_SCL_EMR
1V2 I2C3_SDA_EMR
AP5 EMR_PEN_FWE
AR4 BLE_RST_N
AP4 BLE_PB2_DATA
AP3 BLE_PB0_CS
AR2 BLE_PB1_CLK
1P3 SPK_EN
1P4 LED_CTL

VCC_3V3

R1801 2.2K/5% 5% R0402
R1802 2.2K/5% 5% R0402

I2C3_SCL_EMR
I2C3_SDA_EMR

VCC_3V3

R1803 2.2K/5% 5% R0402
R1804 2.2K/5% 5% R0402

I2C5_SCL_TP_SEN
I2C5_SDA_TP_SEN

VCC_3V3

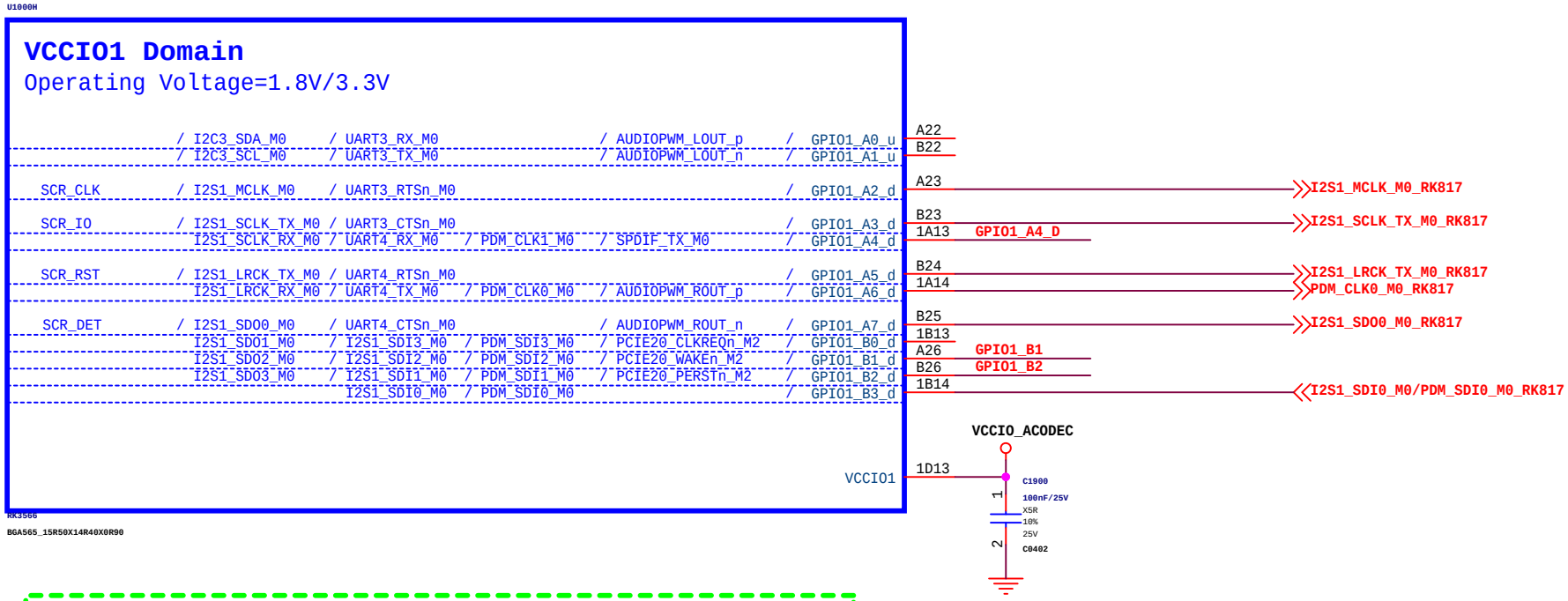
1N5
1N6

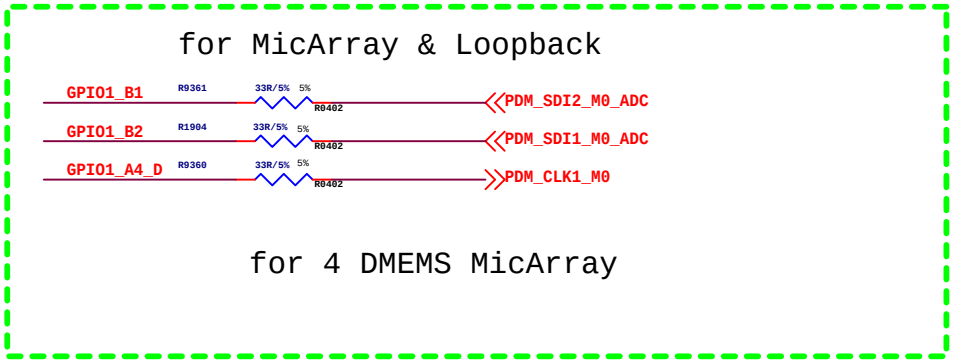
C1800 100nF/25V X5R 10% 25V C0402

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	18.RK3566_VO Interface_2				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	18 of 99

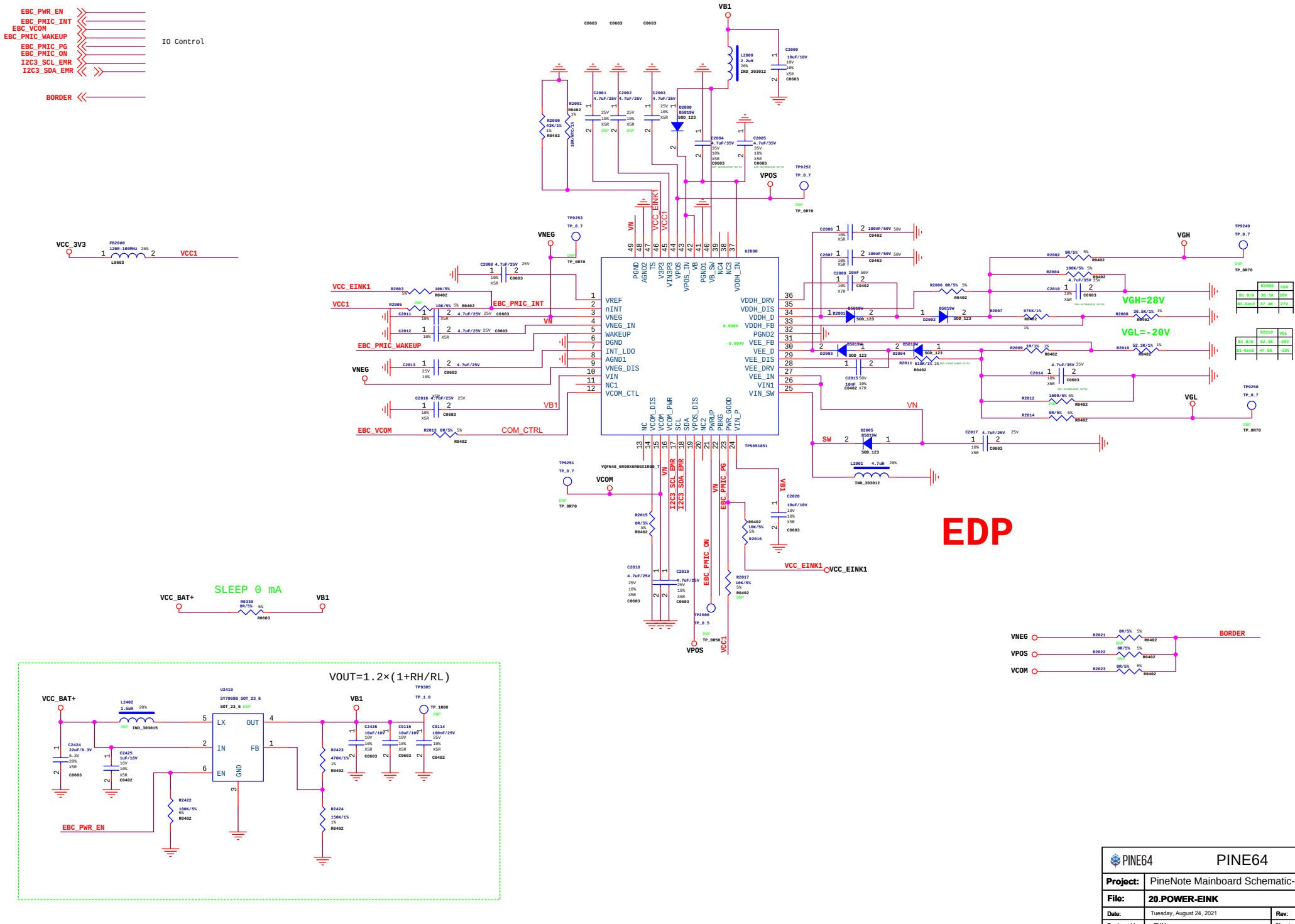
RK3566_H(VCCIO1 Domain)





Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**19.RK3566_Audio Interface**				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	19 of 99



PINE64	PINE64
Project:	PineNote Mainboard Schematic-20210824
File:	20.POWER-EINK
Date:	Tuesday, August 24, 2021
Rev:	V1.2
Designed by:	ZHM
Sheet:	20 of 99

I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_INT
PMIC_SLEEP_H
PMIC_SLEEP_PMIC
REST_KEY
PMIC_PWRON
RESET_SOC
PMIC_32KOUT_WIFI
PMIC_32KOUT_SOC
I2S1_MCLK_M0_RK817
I2S1_SCLK_TX_M0_RK817
I2S1_LRCK_TX_M0_RK817
I2S1_SDO0_M0_RK817
I2S1_SDI0_M0/PDM_SDI0_M0_RK817
PDM_CLK0_M0_RK817
SPK_P_L
SPK_N_L
HPL_OUT
HPR_OUT

PMIC RK817 DCDC

VDD_LOGIC
VDD_LOGIC_P
SLEEP OFF
Feedback from RK3566
VDD_GPU_NPU
<1sat>
<DC Resistor>
VDD Pin
OUT
FB
RK3566
BUCK1/BUCK2
BUCK4
VCC_SYS
VCC_3V3
VCC_DDR
SLEEP ON
SLEEP:2.2mA & Macron 4G BK list

DDR4	1.2V	62K 1%
LPDDR4/4x	1.1V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

Default:1.1V

PMIC RK817 Managerment

VCC5V_MIDU
VBUS
VCC3V3_PMU
VCCIO_WL
VCC_BAT
VCC_BAT+
VCC_BAT-
Page 20, Path switch
Close to BAT
PMIC_32KOUT_WIFI
PMIC_32KOUT_SOC
PMIC_CLK32KOUT
PMIC_SLEEP_PMIC
RESET_PMIC
PMIC_PWRON
I2C0_SDA_PMIC
I2C0_SCL_PMIC
PMIC_INT_PMIC
PMU SIDE
SOC SIDE
RESET_SOC

PMIC RK817 LDO

LDO1 400mA
LDO2 400mA
Low noise LDO3 100mA
Codec vddio LDO4 400mA
LDO5 400mA
LDO6 400mA
LDO7 400mA
LDO8 400mA
LDO9 400mA
VCCA1V8_PMU
VDDA_0V9_LDO
VDDA0V9_PMU
VCCIO_ACODEC
VCCIO_SD
VCC3V3_PMU
VCC_1V8_EN
4G_PWR_ON
WIFI3V3_WPEN
SLEEP_STA_CTL
SLEEP OFF
SLEEP ON
VDDA0V9_IMAGE
VDDA_0V9
VCCIO_WL
VCCA_1V8
VCCA1V8_IMAGE
VCC_1V8
VDDA_0V9_LDO

	R2149	R9408
1.8V IO WIFI	SMT	NC
3.3V IO WIFI	NC	SMT

PMIC RK817 CODEC

VCC_SPK_HP
VCC_CPVDD
VCC_CPVSS
VCC_1P8D
VCC_1P8A
I2S1_MCLK_M0_RK817
I2S1_SCLK_TX_M0_RK817
I2S1_LRCK_TX_M0_RK817
I2S1_SDO0_M0_RK817
I2S1_SDI0_M0/PDM_SDI0_M0_RK817
PDM_CLK0_M0_RK817
HPL_OUT
HP_SNS
HPR_OUT
SPK_OUTn
SPK_OUTp
MICip MIC_L
MICin MIC_R
SPK_P_L
SPK_N_L

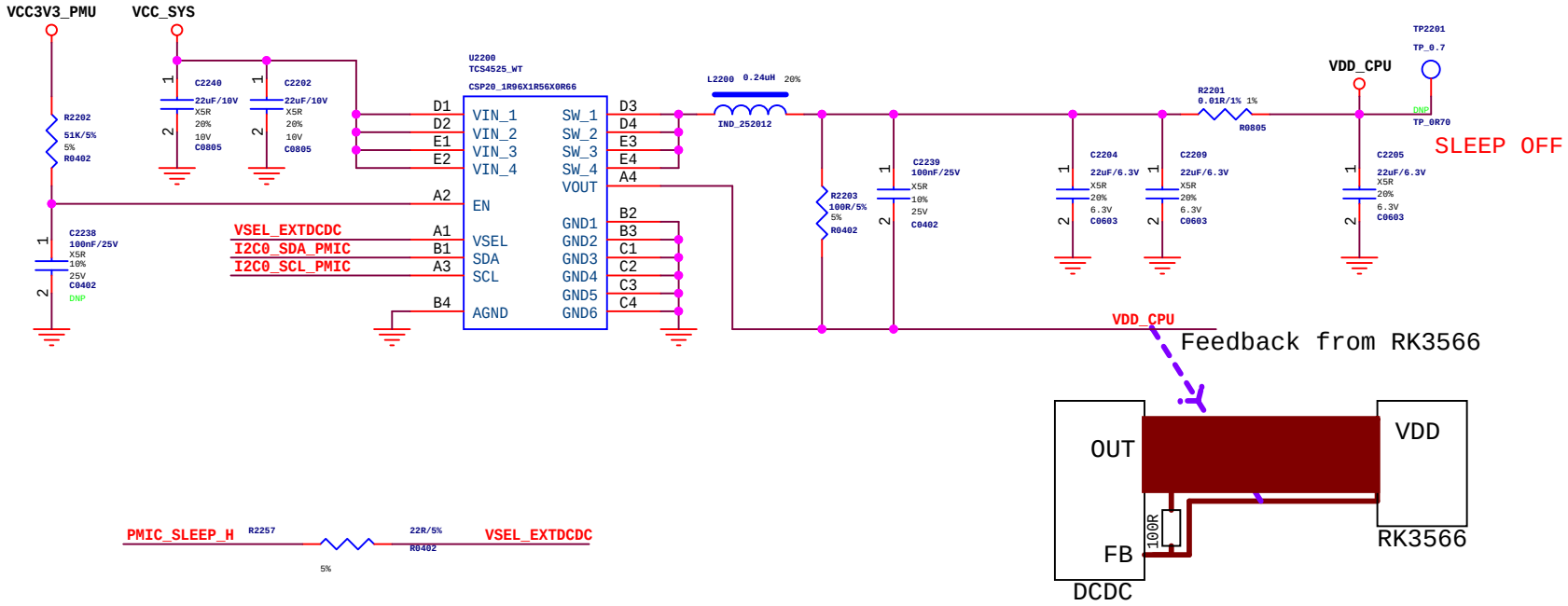
PINE64

Project:	PineNote Mainboard Schematic-20210824
File:	21.Power_PMIC
Date:	Tuesday, August 24, 2021
Rev:	V1.2
Designed by:	Daniel.J
Reviewed by:	Default
Sheet:	21 of 99

I2C0_SCL_PMIC
I2C0_SDA_PMIC

PMIC_SLEEP_H

VDD_CPU_EXT

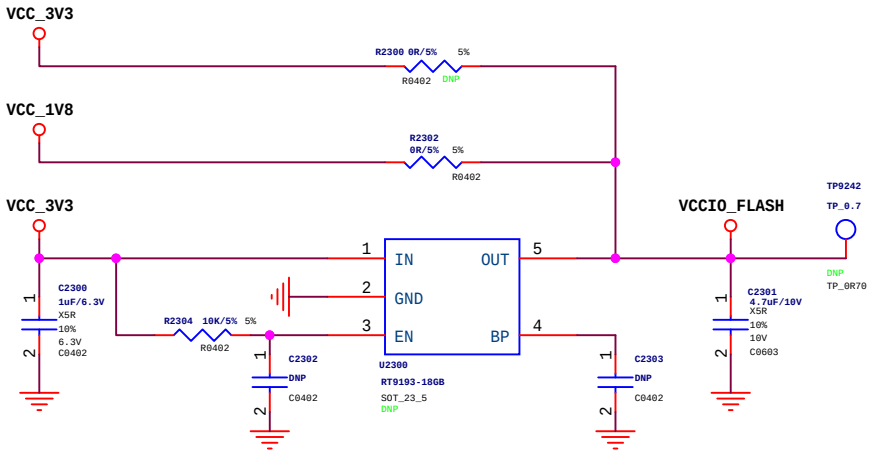


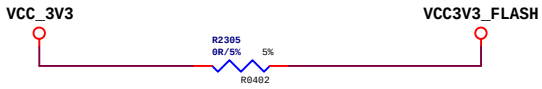
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**22.Power_other**				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	22 of 99

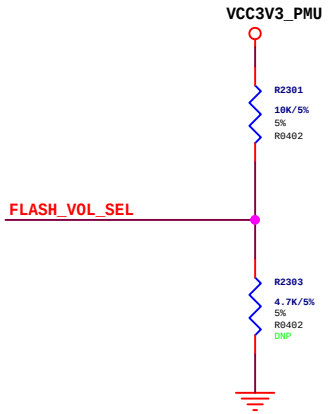
Flash Power Manage

FLASH_VOL_SEL

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)

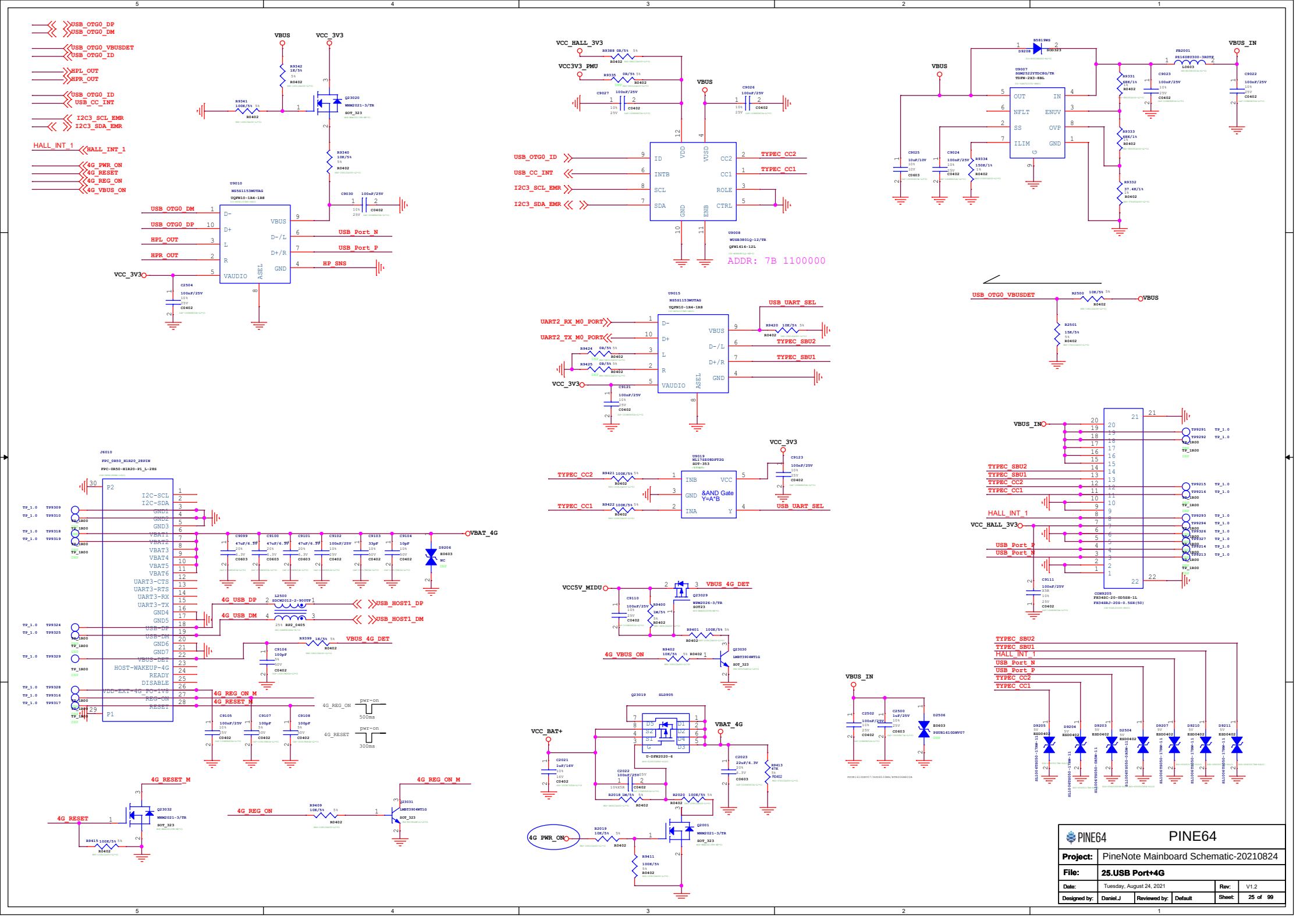




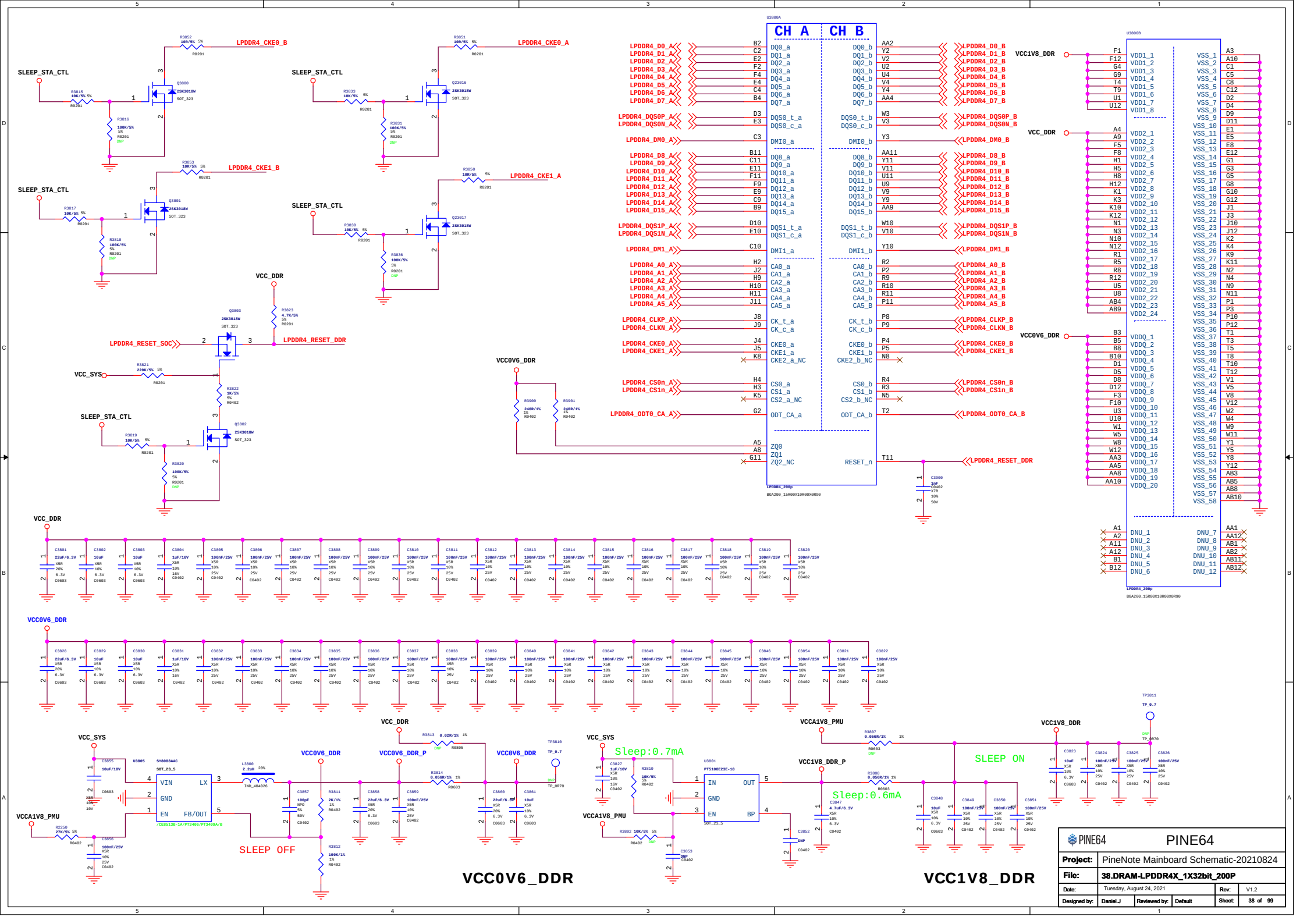


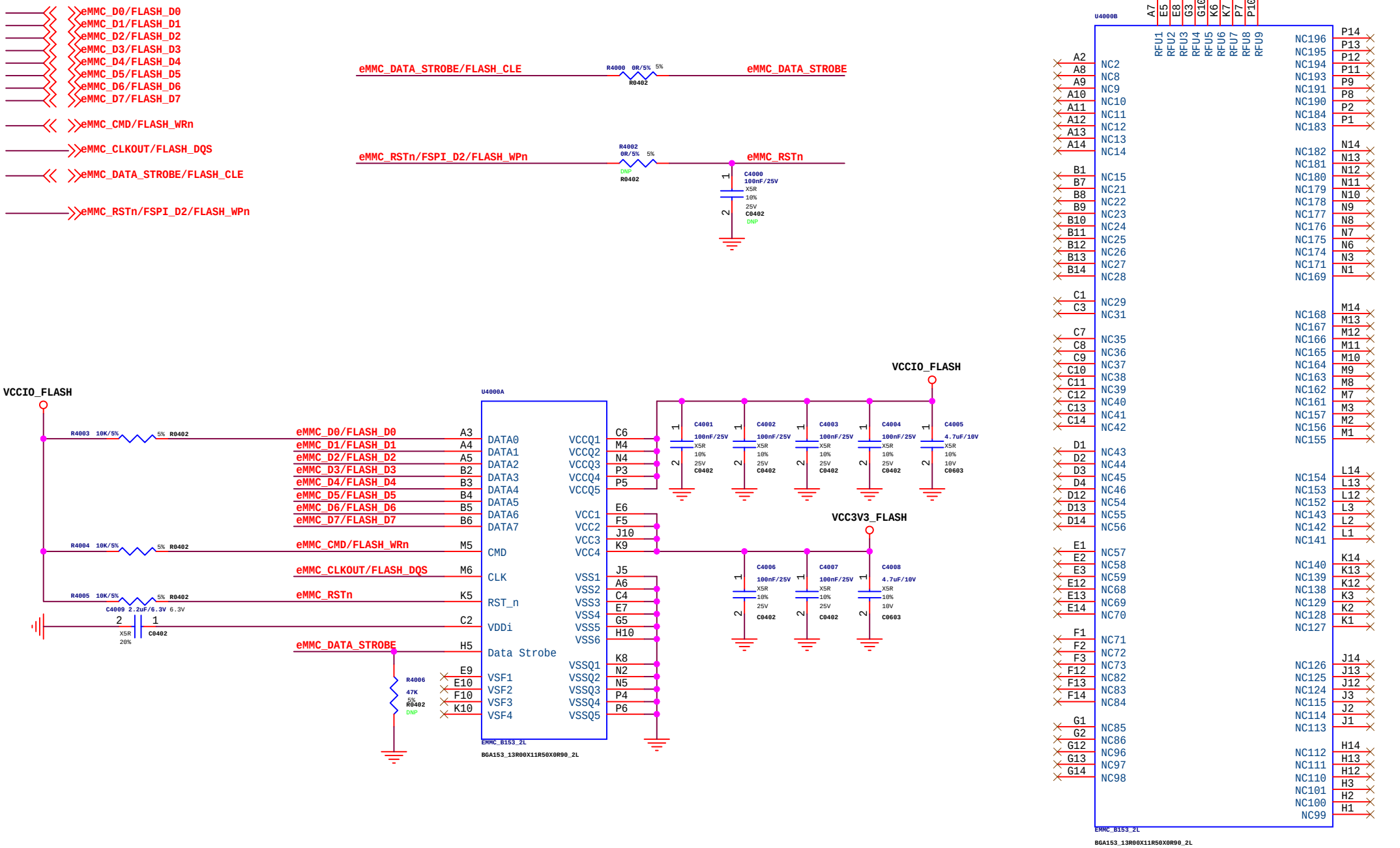
Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	23.Power_Flash Power Manage				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	23 of 99



PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**25.USB Port+4G**				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	25 of 99

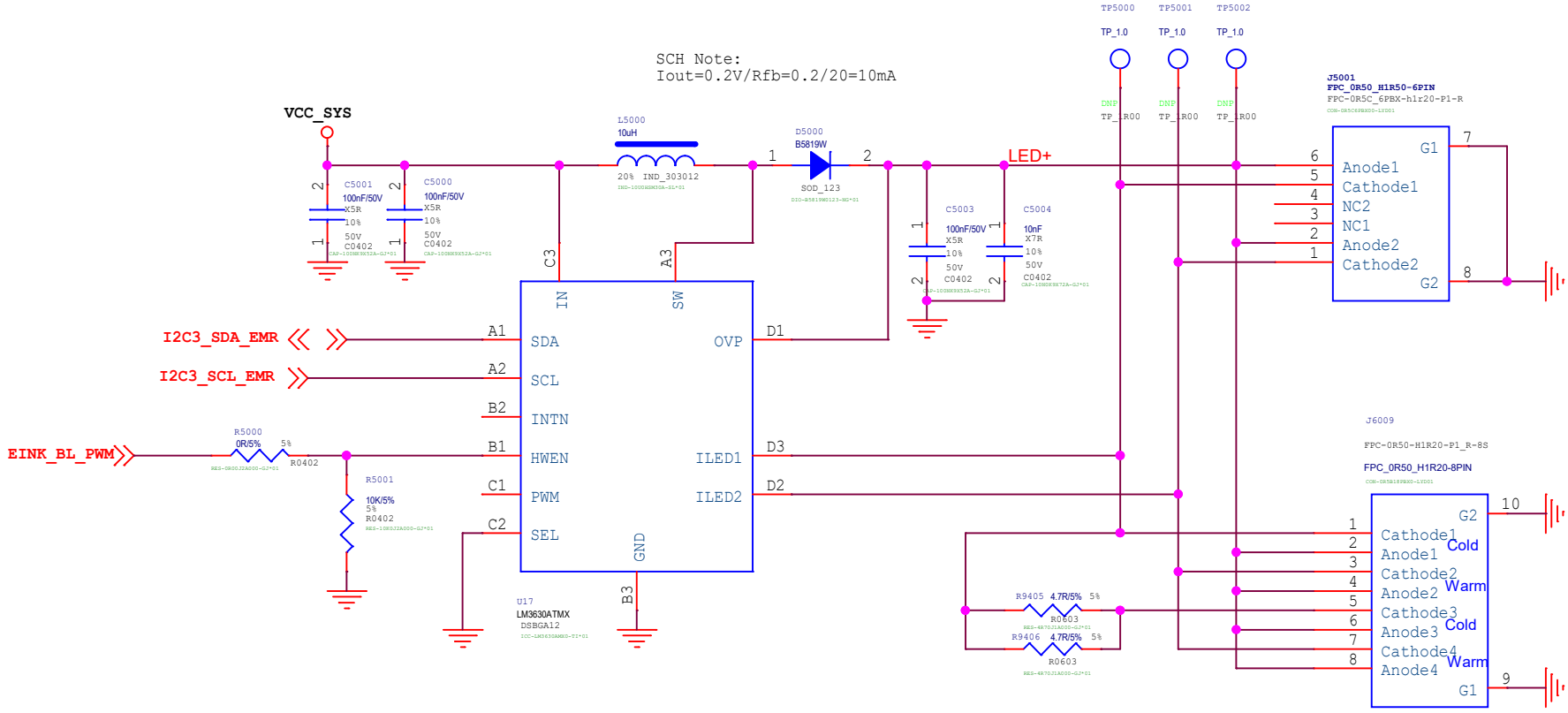

SLEEP_STA_CTL
LPDDR4_CKE0_B
LPDDR4_CKE0_A
LPDDR4_CKE1_B
LPDDR4_CKE1_A
VCC_DDR
LPDDR4_RESET_SOC
LPDDR4_RESET_DDR
VCC_SYS
VCC0V6_DDR
CH A
CH B
LPDDR4_200p
VCC1V8_DDR
VCC0V6_DDR_P
VCCA1V8_PMU
SLEEP OFF
SLEEP ON
Sleep:0.7mA
Sleep:0.6mA
VCC0V6_DDR
VCC1V8_DDR
PINE64
Project: PineNote Mainboard Schematic-20210824
File: 38.DRAM-LPDDR4X_1X32bit_200P
Date: Tuesday, August 24, 2021
Rev: V1.2
Designed by: Daniel.J
Reviewed by: Default
Sheet: 38 of 99



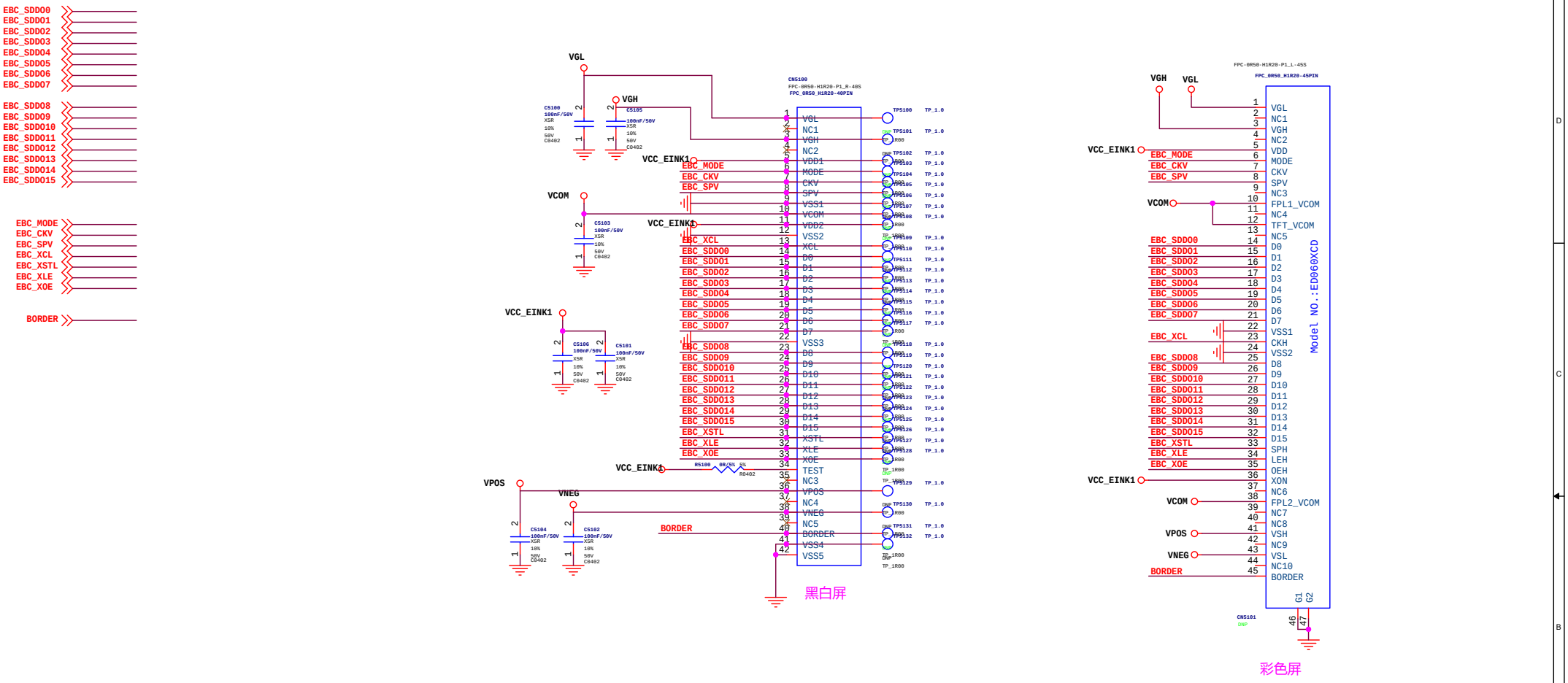
Rockchip Confidential

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**40.Flash-eMMC Flash**				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	40 of 99

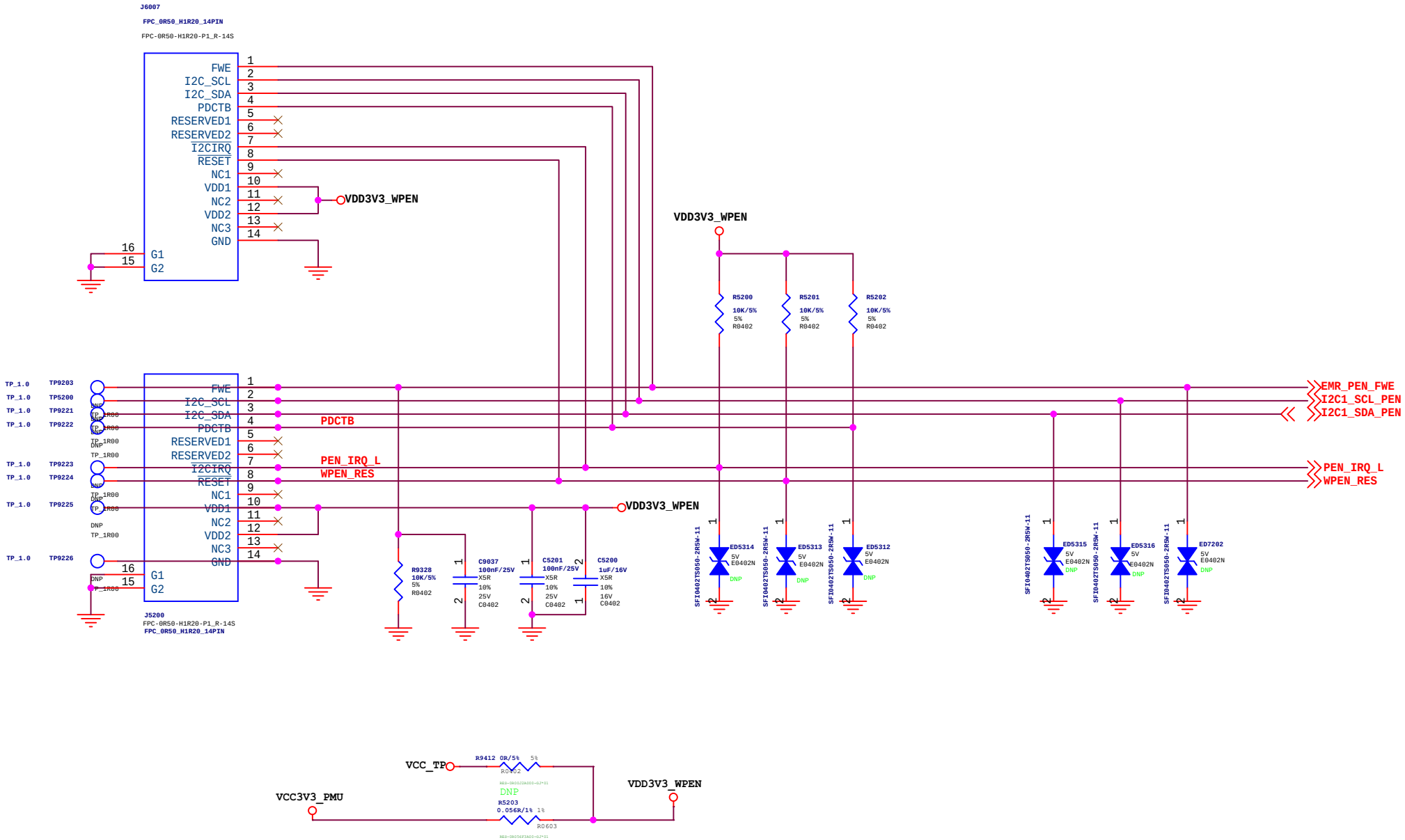
Dual Cod/Warm light control, Front Light IC at FPC cable.



PINE64	PINE64		
Project:	PineNote Mainboard Schematic-20210824		
File:	**50.Front Light**		
Date:	Tuesday, August 24, 2021	**Rev:**	V1.2
Designed by:	ZHM	**Sheet:**	50 of 99



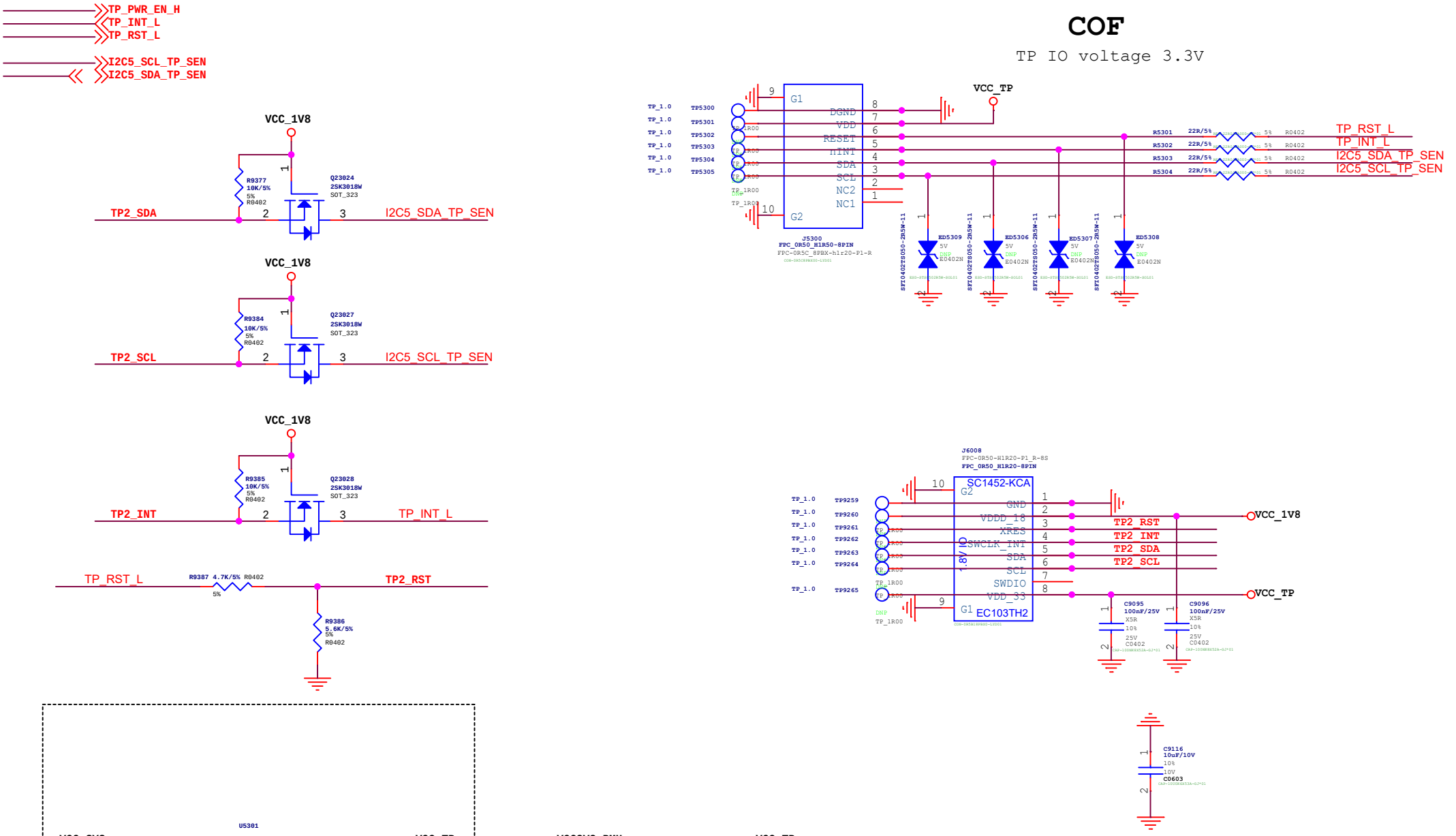
PINE64	PINE64		
Project:	PineNote Mainboard Schematic-20210824		
File:	**51.ED103_EPD**		
Date:	Tuesday, August 24, 2021	**Rev:**	V1.2
Designed by:	ZHM	**Sheet:**	51 of 99



PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**52.EMR**				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	52 of 99

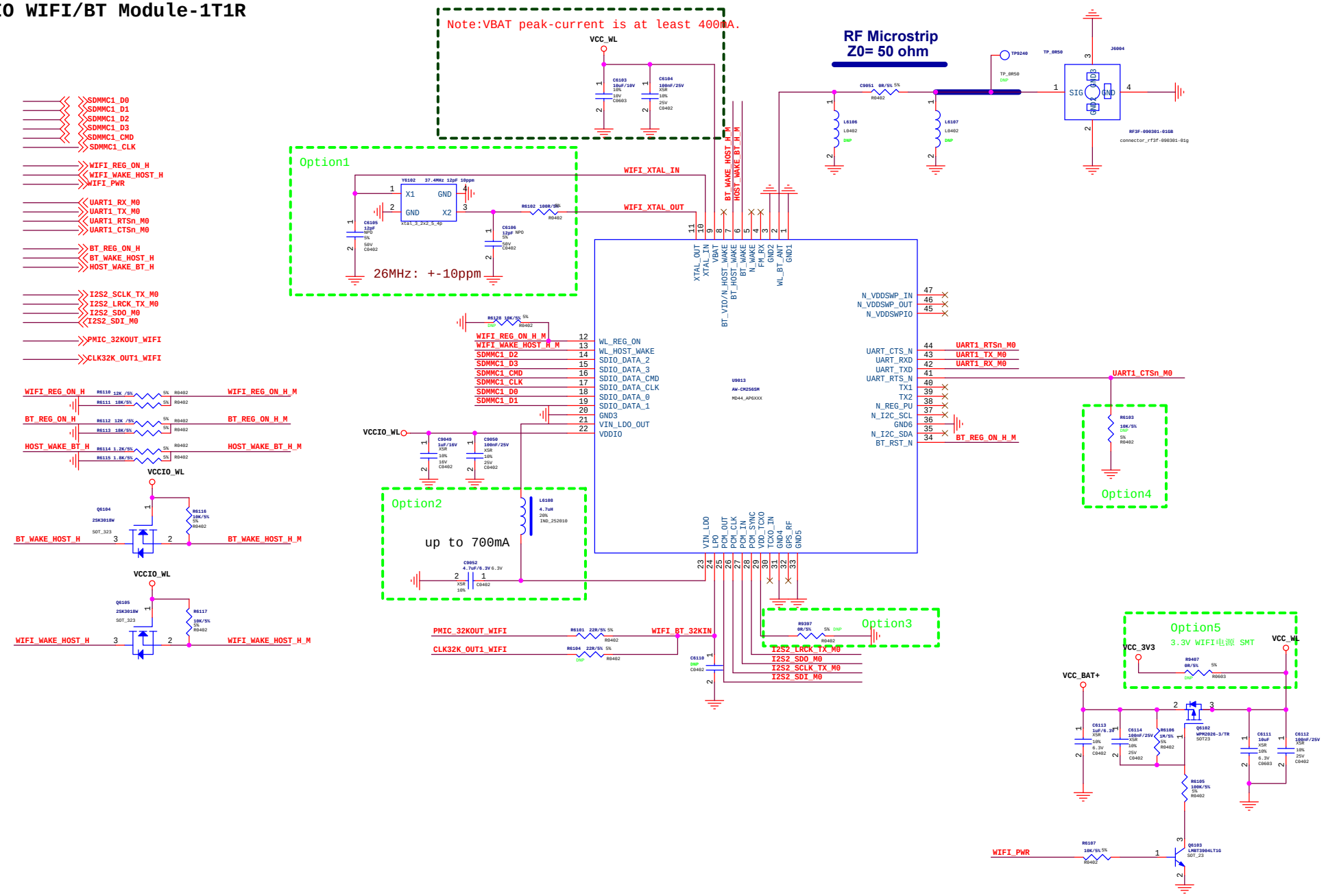
COF

TP IO voltage 3.3V

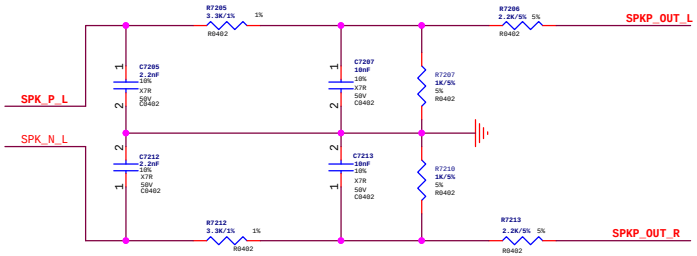


PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**53.TP**				
Date:	Tuesday, August 24, 2021			**Rev:**	V1.2
Designed by:	Daniel.J	**Reviewed by:**	Default	**Sheet:**	53 of 99

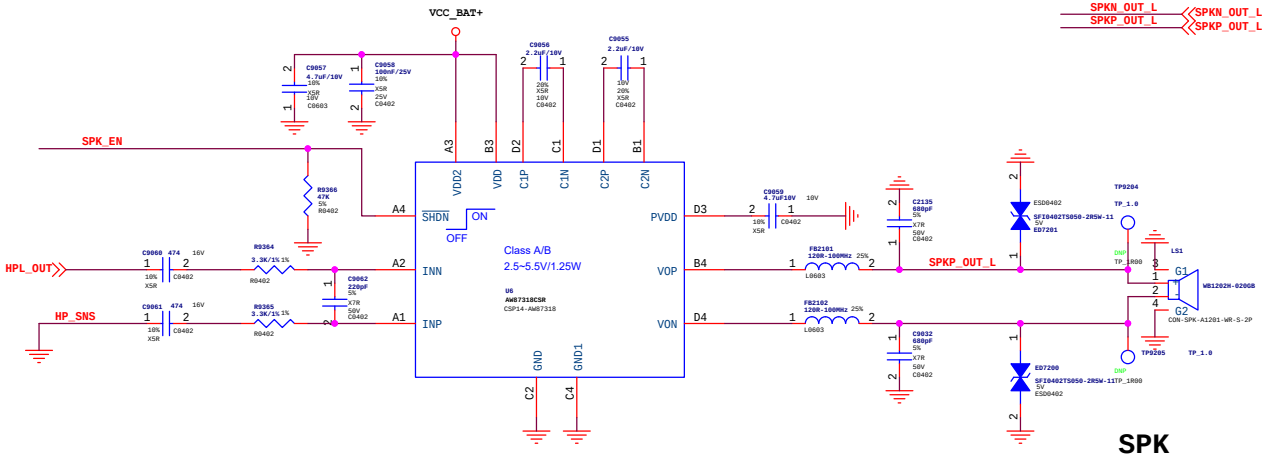
SDIO WIFI/BT Module-1T1R

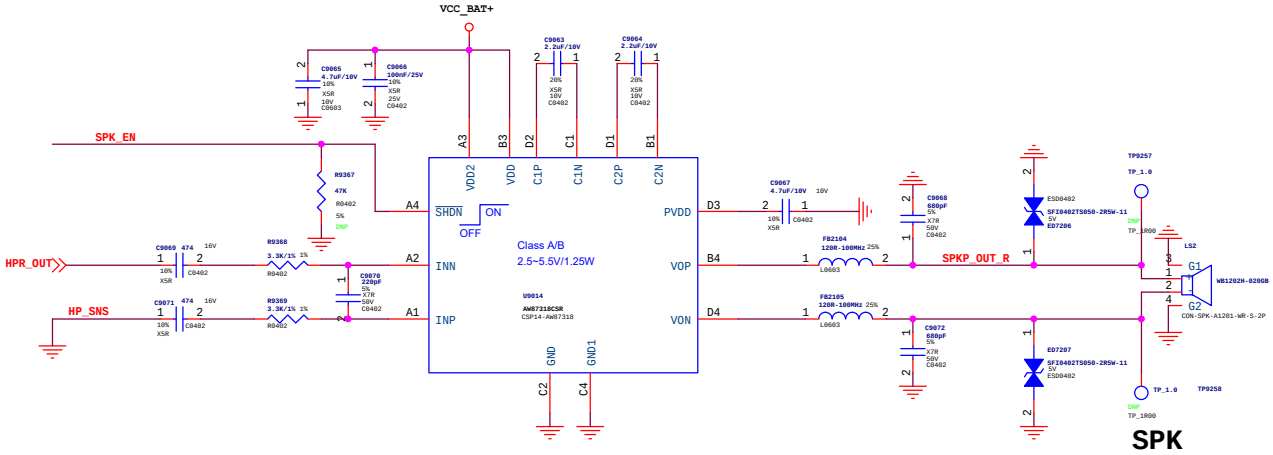


PINE64	PINE64		
Project:	PineNote Mainboard Schematic-20210824		
File:	**61.WIFI/BT-SDIO_1T1R**		
Date:	Tuesday, August 24, 2021	**Rev:**	V1.2
Designed by:	Linus.Lin	**Reviewed by:**	**Sheet:** 61 of 99



Loopback for Stereo Speaker





SPK_P_L
SPK_N_L
HPL_OUT
HPR_OUT
SPKN_OUT
SPKP_OUT
SPK_EN

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	70.Audio-SPK				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	70 of 99

PMIC_SLEEP_PMIC

I2C5_SCL_TP_SEN
I2C5_SDA_TP_SEN

GSENSOR_INT_L

HALL_INT_L

VCC_3V3

C9007
100nF/25V
X5R 25V
10%
C0402

I2C5_SCL_TP_SEN

R4
NC
R0402
DNP

GND

I2C5_SDA_TP_SEN

VCC_3V3

C3
100nF/25V
X5R
10%
25V
C0402

SDO
SDI
VDIO
NC
SCX
PS
CSB
GND
GNDIO
VDD
INT1
INT2

R2 10K/5% 5%
R0402

GND

VCC_3V3

C1
NC
C0402
DNP

GND

U1
LGA_2X2X0R9
SC7A20

GSENSOR_INT_L

7bit address :0x18H

R5
47K
5%
R0402

VCC_3V3

VCC_HALL_3V3

R9003
10K/5% 5%
R0402

HALL_INT_1

C9005
2.2uF/6.3V 20%
X5R
6.3V
C0402

D9001
BS819WS
SOD323

R9000 10R/5% 5%
R0402

R9002
1M/5%
5%
R0402

D9002
BS819WS
SOD323

C9010
220nF
X5R
16V
10%
C0402

R9001
1M/5%
5%
R0402

U9000
SOT_23_5
SN74LVC1G17DBVR

NC
A
GND
VCC
Y

VCC_HALL_3V3

C9002
100nF/25V
X5R 25V
10%
C0402

R9004 100K/5% 5%
R0402

PMIC_SLEEP_PMIC

Q9000
LMBT3904LT1G
SOT_23

C9006
2.2uF/6.3V
X5R 6.3V
C0402
20%

D9000 BS819WS
SOD323

HALL_INT_L

Cover open HALL_INT Hi
Cover Close HALL_INT Lo

SLEEP ON

VCC_SYS

SLEEP:0.07mA

C9000
2.2uF/10V
X5R
10V
20%
C0402

R9005
10K/5%
5%
R0402

U9004
PT5108E23E-33
SOT_23_5

IN
GND
EN
OUT
BP

VCC_HALL_3V3

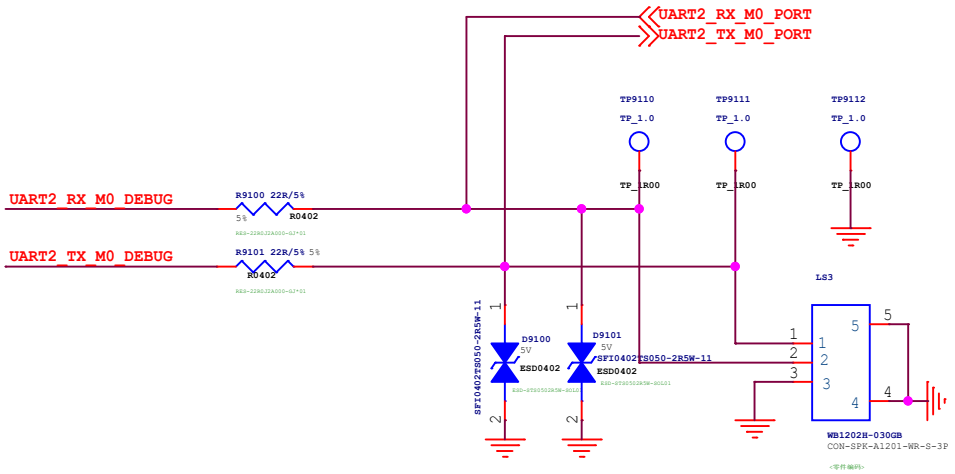
C9003
2.2uF/6.3V
X5R
6.3V
C0402

C9001
100nF/25V
X5R
25V
20%
C0402

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**90.Sensor/HALL**				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	90 of 99

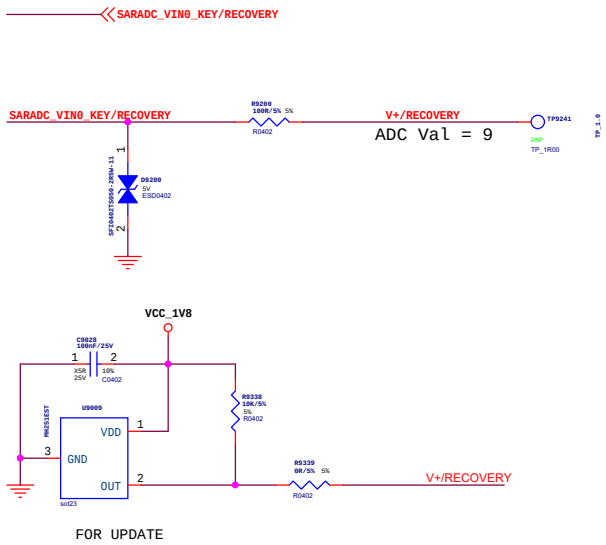
UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG

Debug UART2



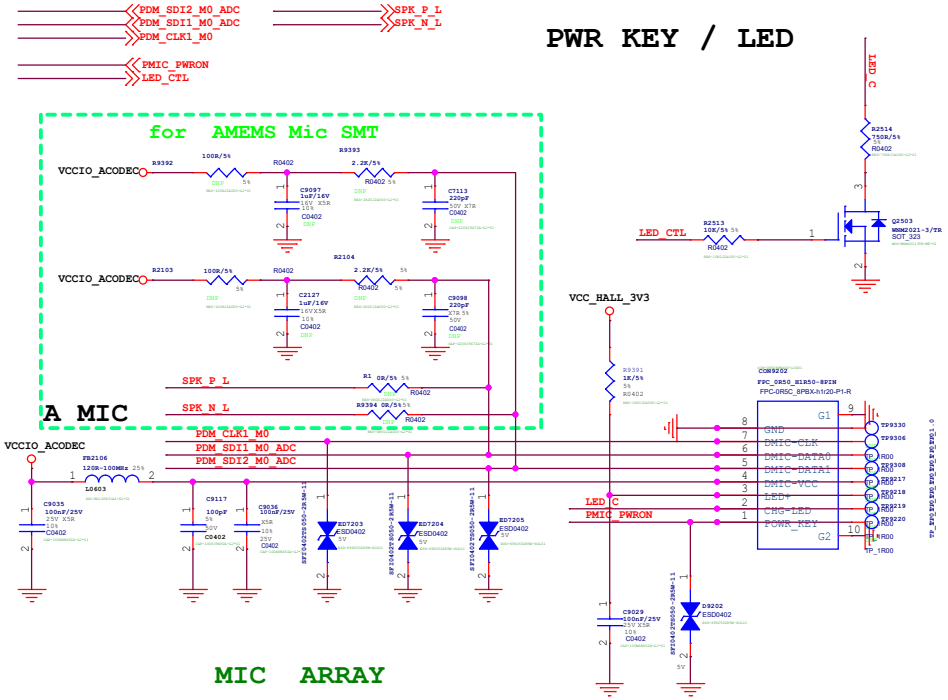
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**91.Debug UART**				
Date:	Tuesday, August 24, 2021			**Rev:**	V1.2
Designed by:	Daniel.J	**Reviewed by:**	Default	**Sheet:**	91 of 99

ADC KEY



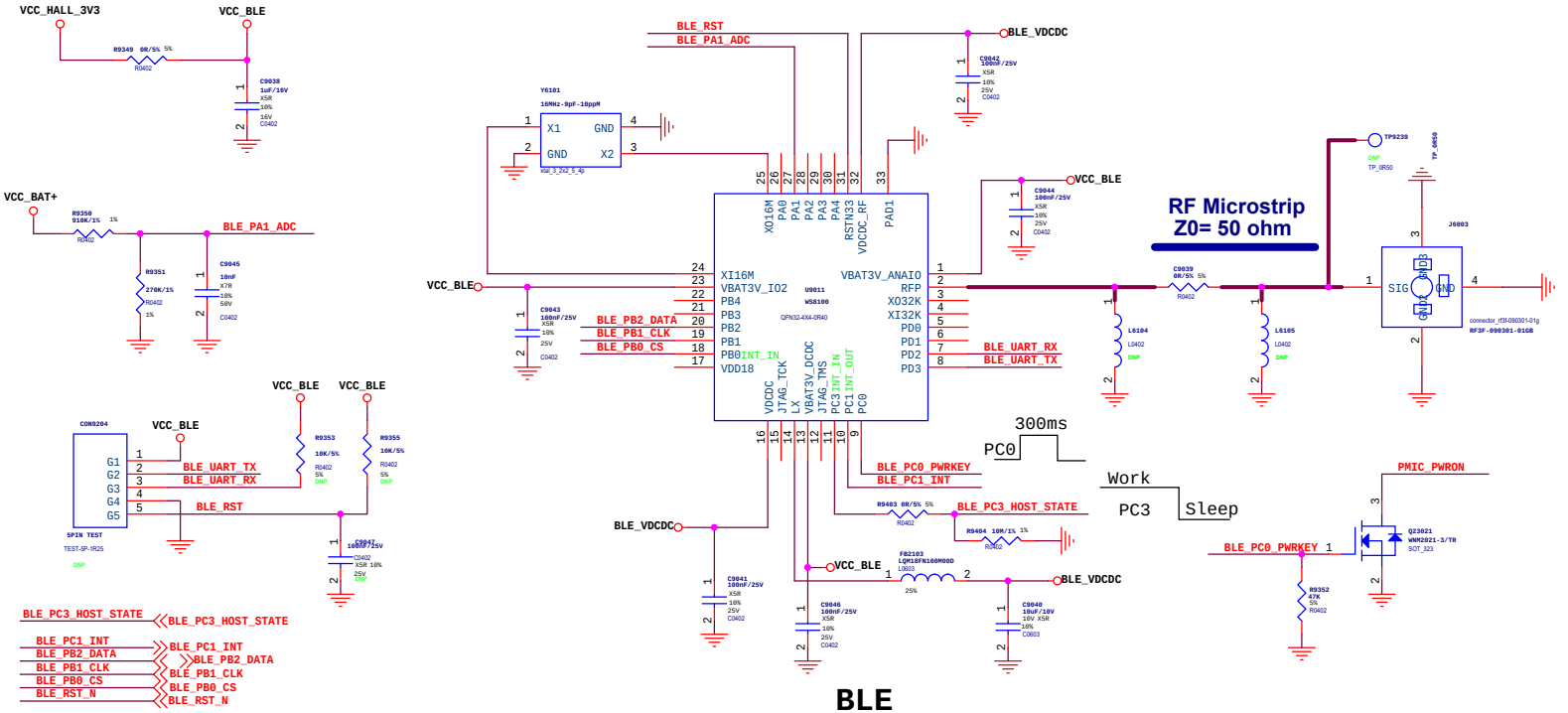
Update

PWR KEY / LED



MIC ARRAY

Default DMIC

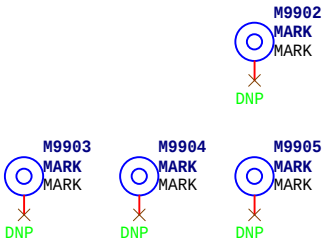


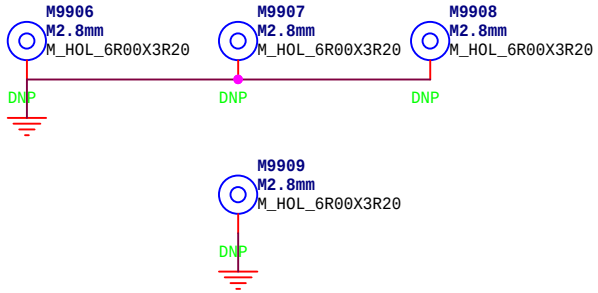
BLE

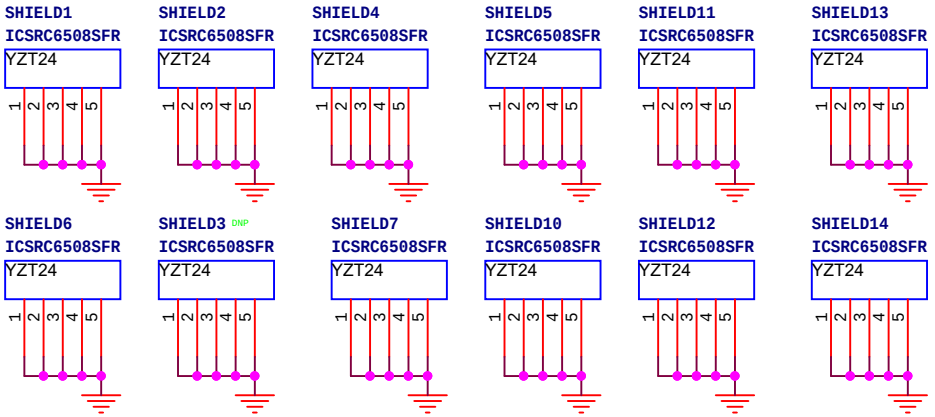
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**92.KEY Array+BLE+MIC**				
Date:	Tuesday, August 24, 2021			**Rev:**	V1.2
Designed by:	Daniel.J	**Reviewed by:**	Default	**Sheet:**	92 of 99

Page of Accessories

PCB Mark Point







Heatsink

When use socket,
NO Heatsink holes is reserved.

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210824				
File:	**99.Mark/Hole/Heatsink**				
Date:	Tuesday, August 24, 2021			Rev:	V1.2
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	99 of 99