PineNote Schematics v1.1

Main Functions Introduction

1) PMIC: RK817-5+Charger+DiscretePower
2) RAM: LPDDR4 1x32Bit(Default:4GB)
3) ROM: eMMC5.1(Default:128GB)
4) Support: Support: 1 x USB2.0 OTG
5) Support: 8Bit/16Bit E-Paper
6) Support: a/b/g/n/ac WIFI, BT5.0
7) Support: Gyroscope-sensor G-sensor M-sensor PS-sensor
8) Support: Speaker out(1.3W@8ohm)

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**00.Cover Page**				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	0 of 99

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Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

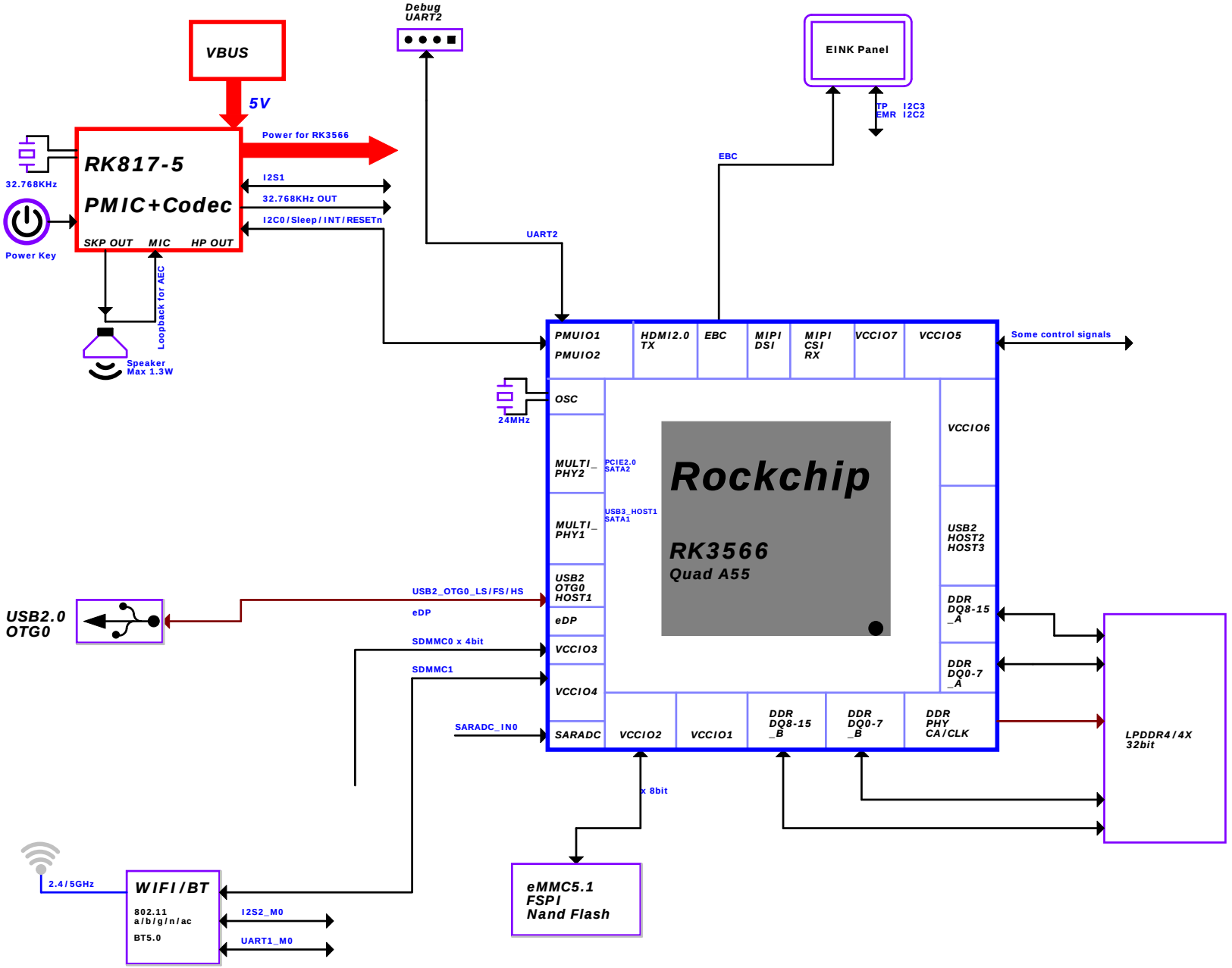
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	01.Index and Notes				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	1 of 99

Revision History

Version	Date	By	Change Dsecription	Approved
V0.1	2020-10-26	ZHM	1: Revision preliminary version	
V1.1	2021-07-26	Pine64	1: PineNote schematic released	

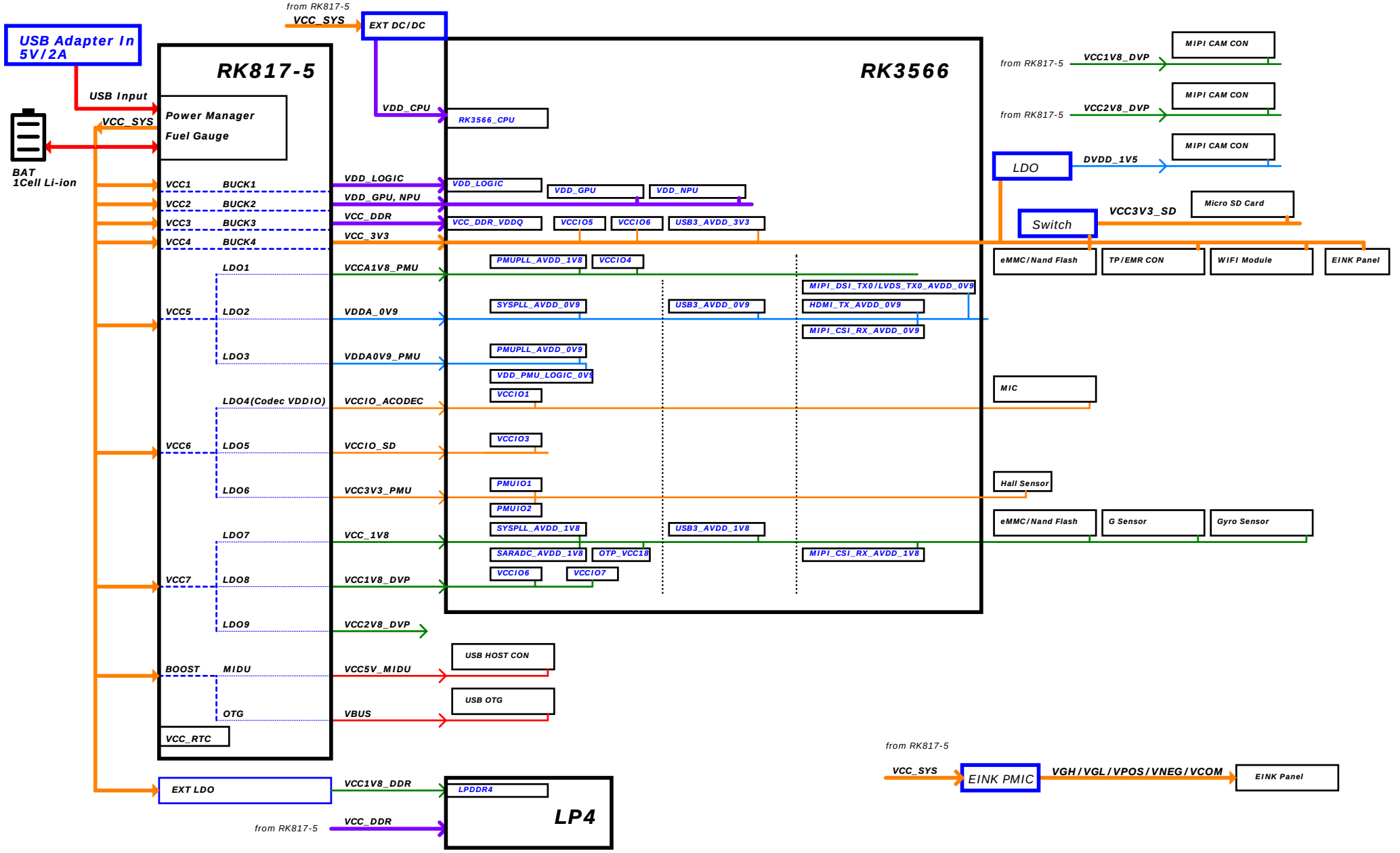
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**02.Revision History**				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	2 of 99

RK3566 Ref Block Diagram



PINE64	
Project:	PineNote Mainboard Schematic-20210726
File:	03.Block Diagram
Date: Monday, July 26, 2021	Rev: V1.1
Designed by: Daniel.J	Reviewed by: Default
	Sheet: 3 of 99

Power Diagram



PINE64	
Project:	PineNote Mainboard Schematic-20210726
File:	04.Power Diagram
Date:	Monday, July 26, 2021
Rev:	V1.1
Designed by:	Daniel.J
Reviewed by:	Default
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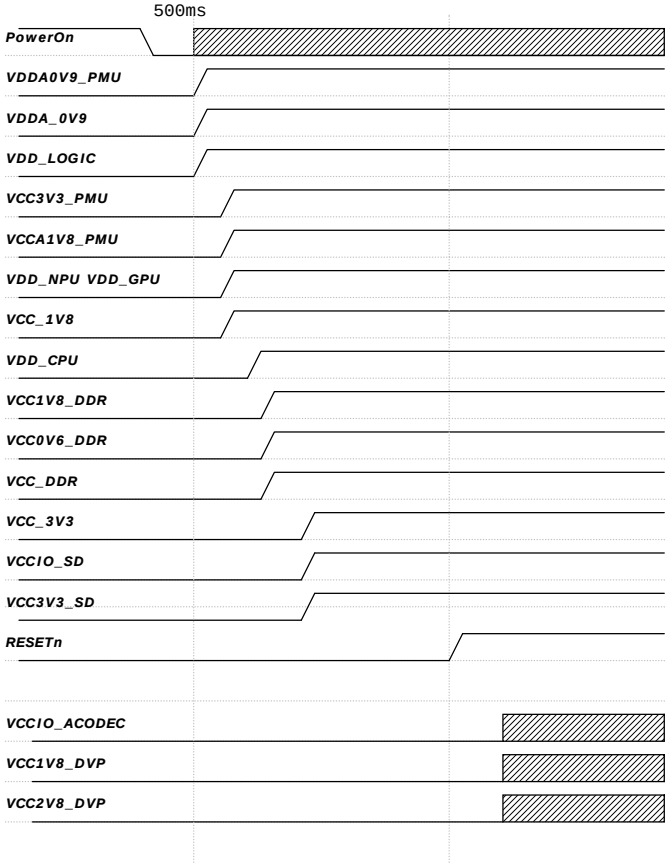
Power Sequence &Power Path assignment



Power Source	PMIC Channel	Supply Limit	Power Supply Name	Time Slot	Default Voltage	Work Status	Sleep Status
VCC_SYS	RK817-5_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_BUCK2	2.5A	VDD_NPU,VDD_GPU	Slot:2	0.9V	ON	OFF
VCC_SYS	RK817-5_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON
VCC_SYS	RK817-5_BUCK4	1.5A	VCC_3V3	Slot:4	3.3V	ON	OFF
VCC_SYS	RK817-5_LDO1	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON
	RK817-5_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF
	RK817-5_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_LDO4	0.4A	VCCIO_ACODEC	N/A	1.8V	ON	OFF
	RK817-5_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF
	RK817-5_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON
VCC_SYS	RK817-5_LDO7	0.4A	VCC_1V8	Slot:2	1.8V	ON	OFF
	RK817-5_LDO8	0.4A	VCC1V8_DVP	N/A	1.8V	ON	OFF
	RK817-5_LDO9	0.4A	VCC2V8_DVP	N/A	2.8V	ON	OFF
VCC_BAT	RK817-5_RESETn			Slot:4+5			
VCC_BAT	RK817-5_BOOST RK817-5_OTG	1.5A	VCC5V_MIDU VBUS	N/A	5.0V	ON	OFF
VCC_3V3	Switch		VCC3V3_SD	Slot:4	3.3V	ON	OFF
VCC_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF

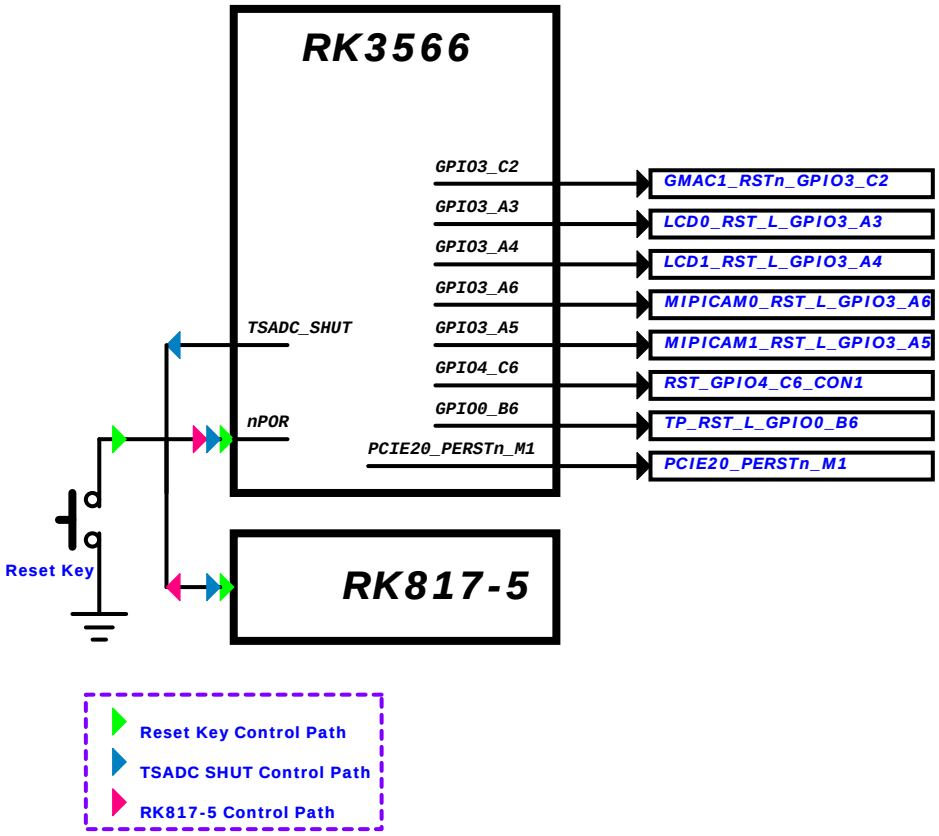
IO Power Domain Map

Refer to the actual design!

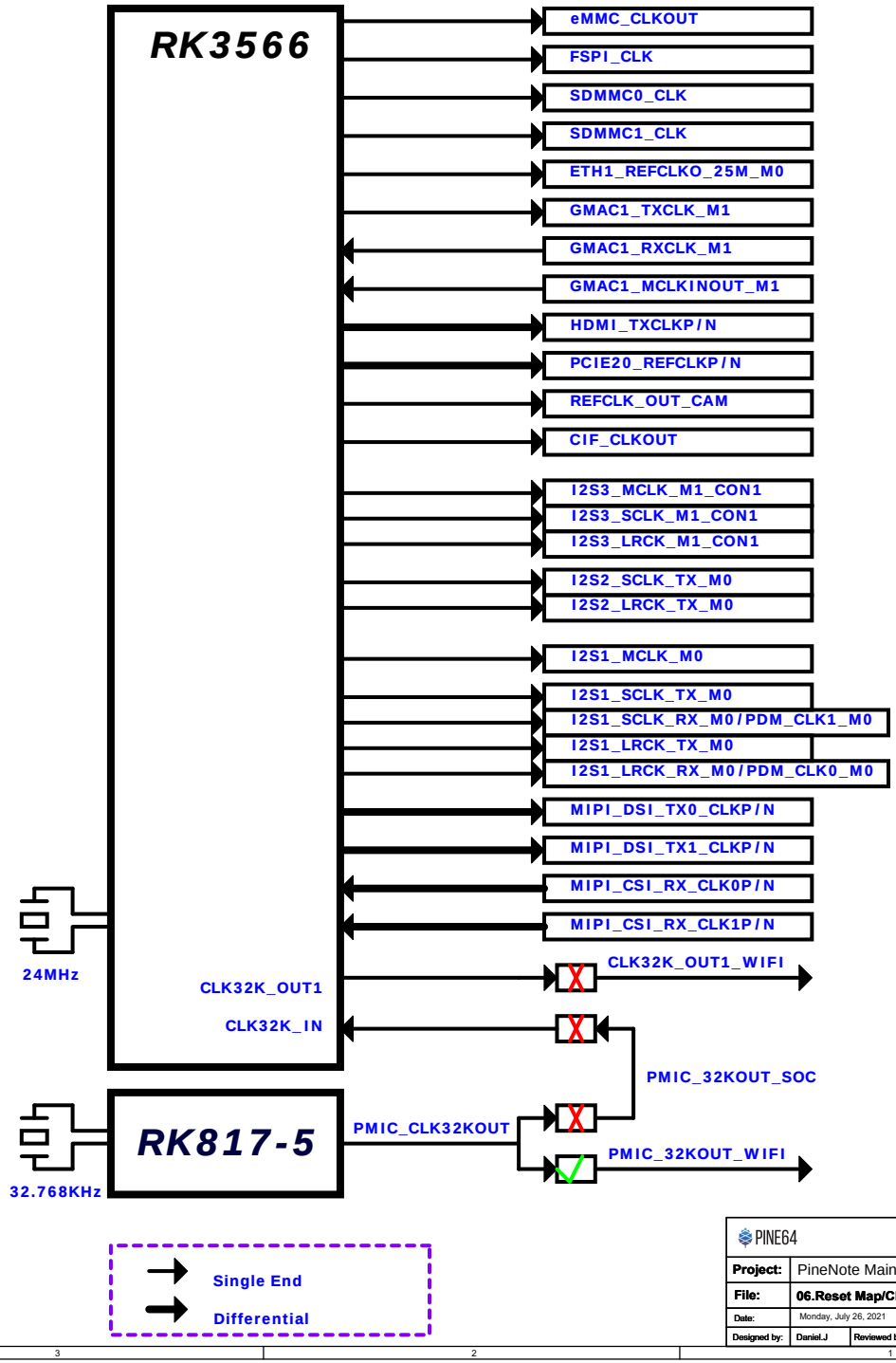
IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO4	VCC1V8_PMU	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_3V3	3.3V	
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC_3V3	3.3V	
VCCIO7	1N8	YES	YES	VCCIO7	VCC1V8_DVP	1.8V	

PINE64	PINE64		
Project:	PineNote Mainboard Schematic-20210726		
File:	05.Power Sequence/IO Domain Map		
Date:	Monday, July 26, 2021	Rev:	V1.1
Designed by:	Daniel.J / Reviewed by: Default	Sheet:	5 of 99

RESET Signal MAP

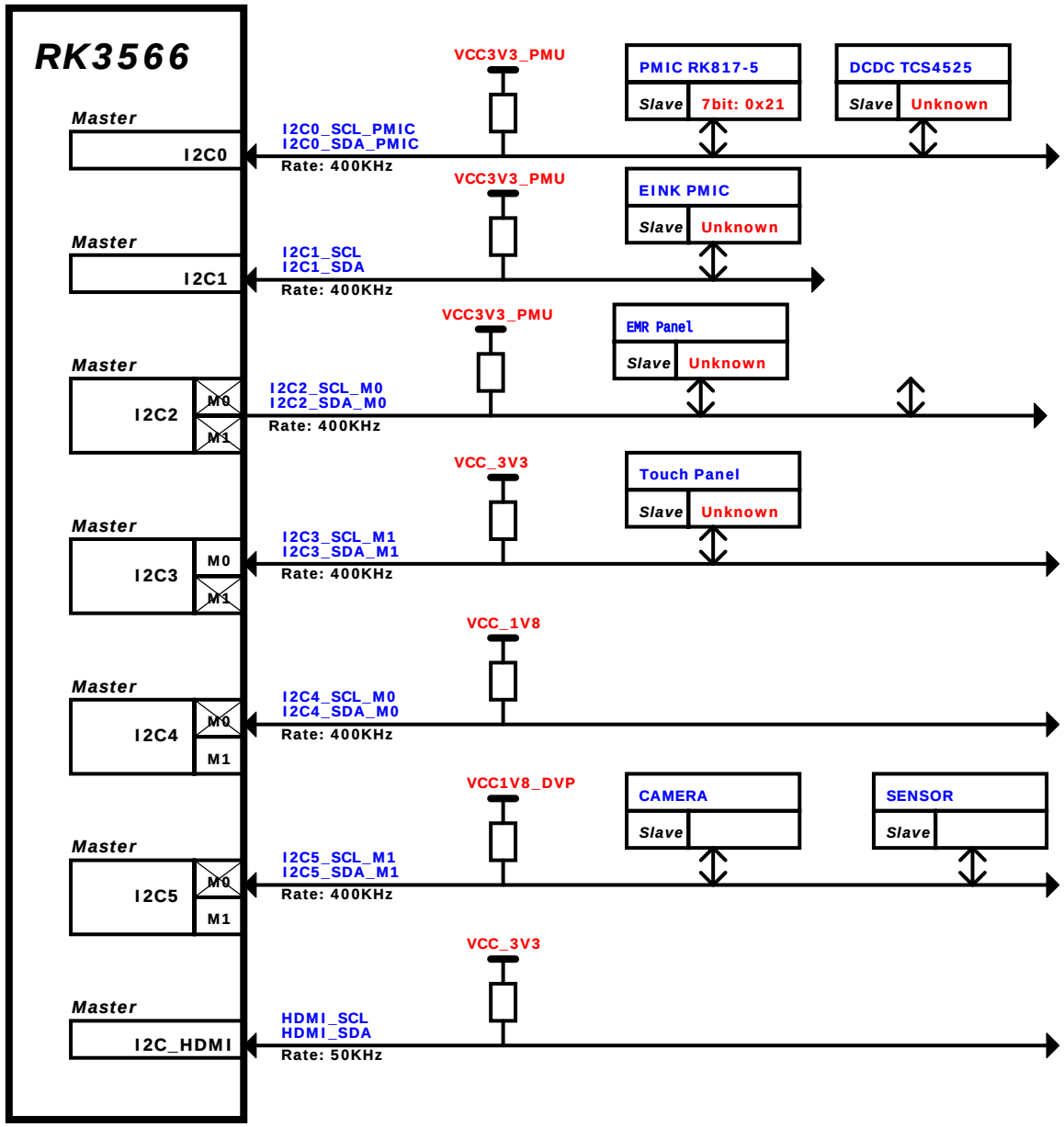


Clock Map



PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	06.Reset Map/Clock Map				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	6 of 99

I2C MAP

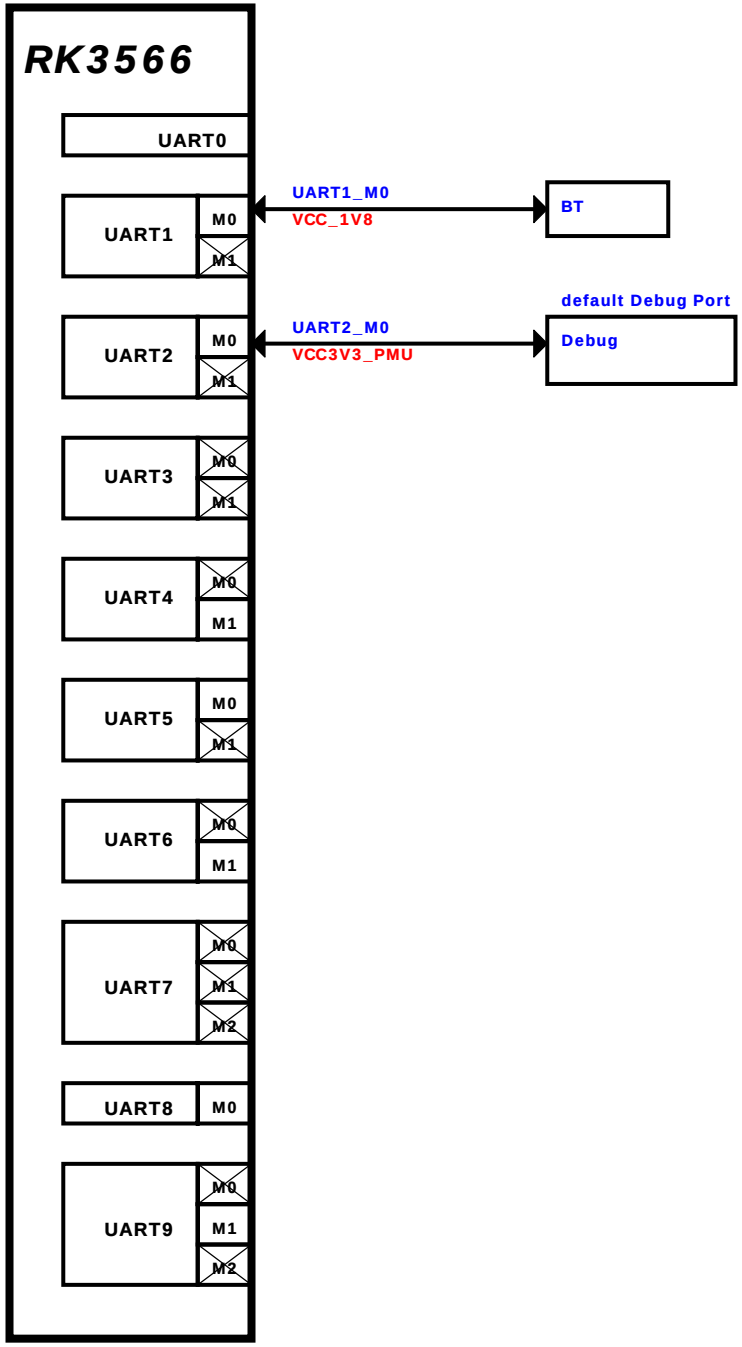


M0 Unselected IOmux path

M1 IOmux path in use

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	07.I2C Bus Map				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	7 of 99

UART MAP

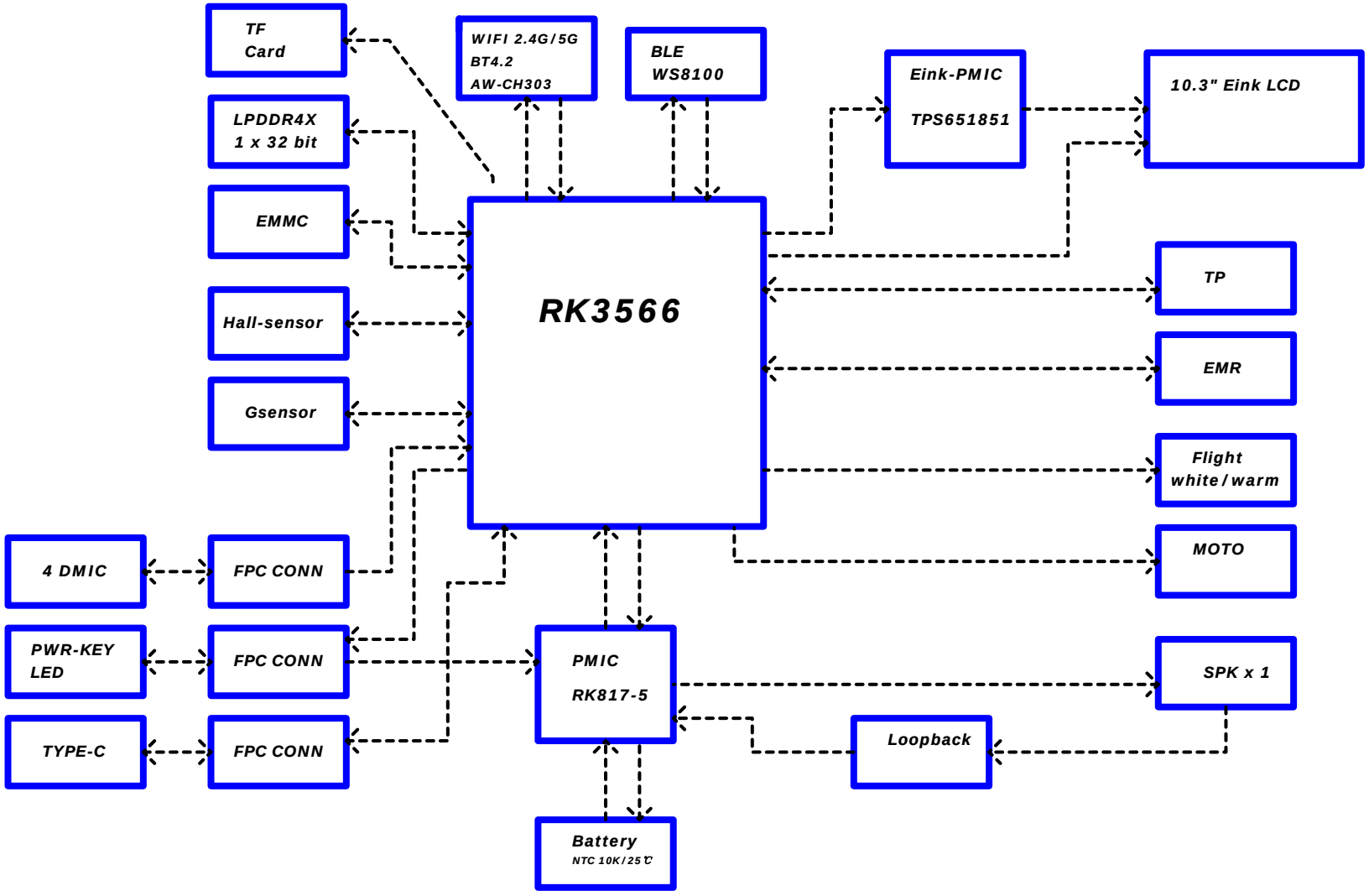


UART1_M0
VCC_1V8
BT

default Debug Port
UART2_M0
VCC3V3_PMU
Debug

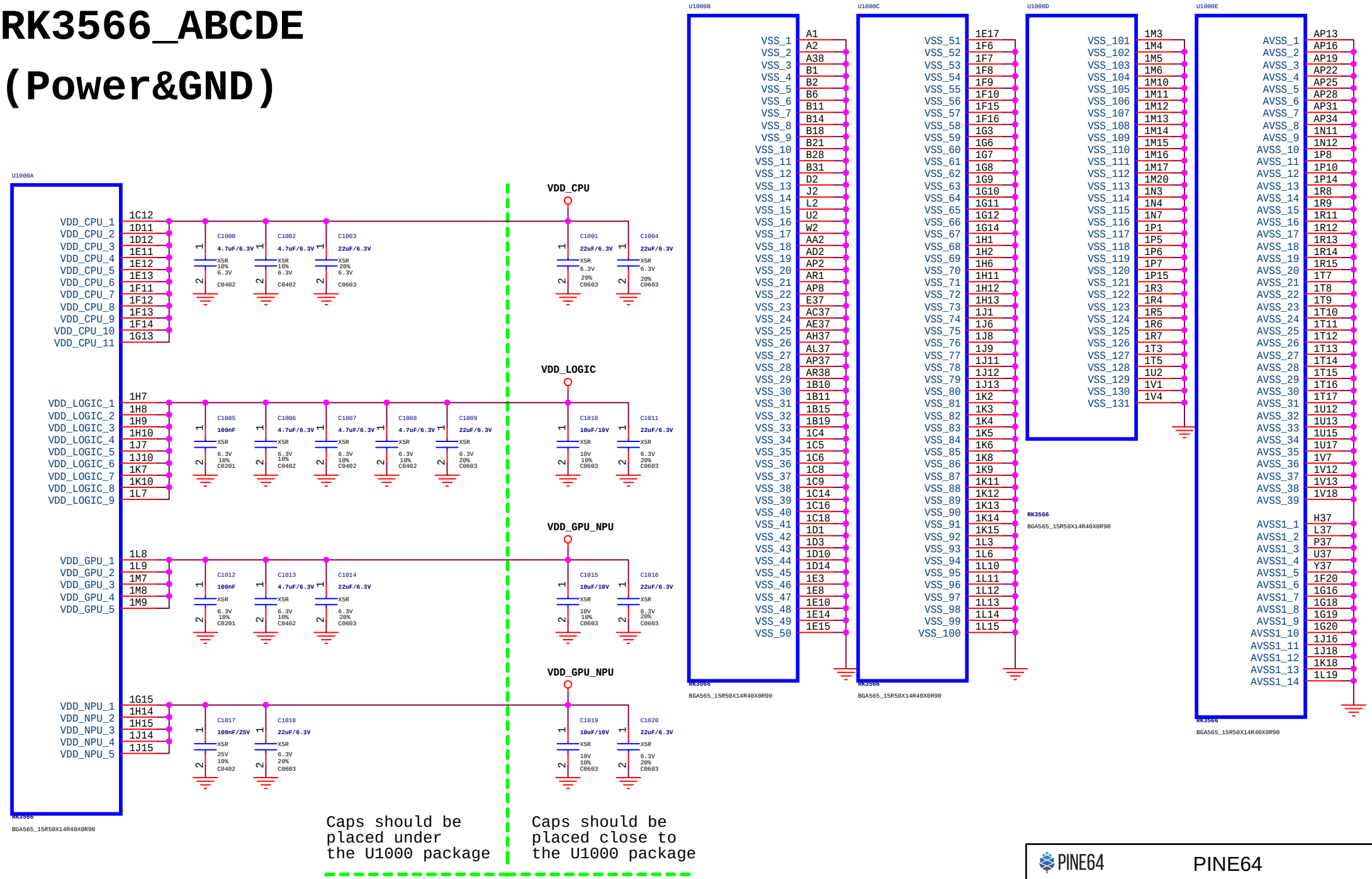
M0 Unselected IOmux path
M1 IOmux path in use

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	08.UART Map				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	8 of 99



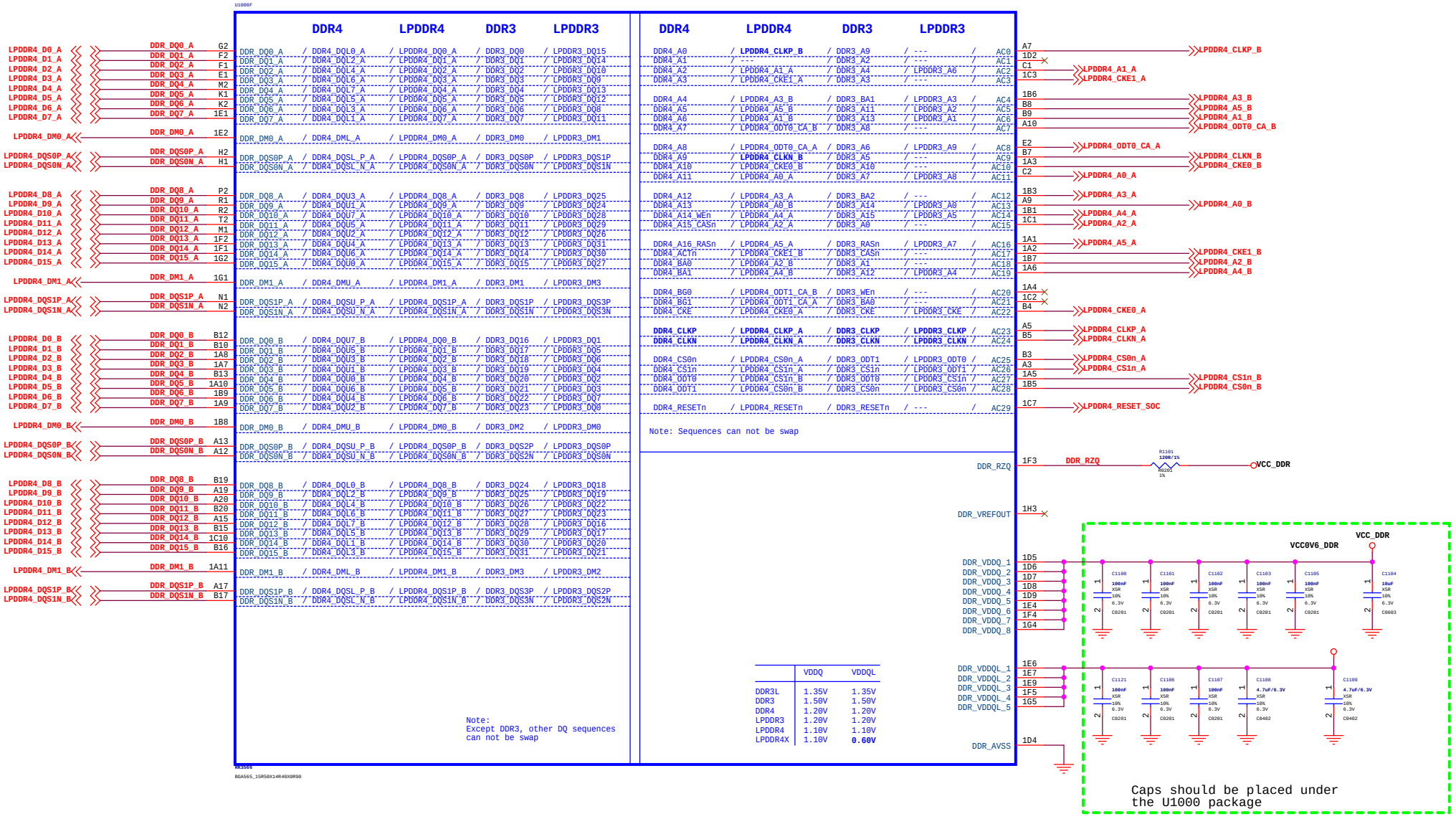
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	09. Diangram				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	9 of 99

RK3566_ABCDE (Power&GND)



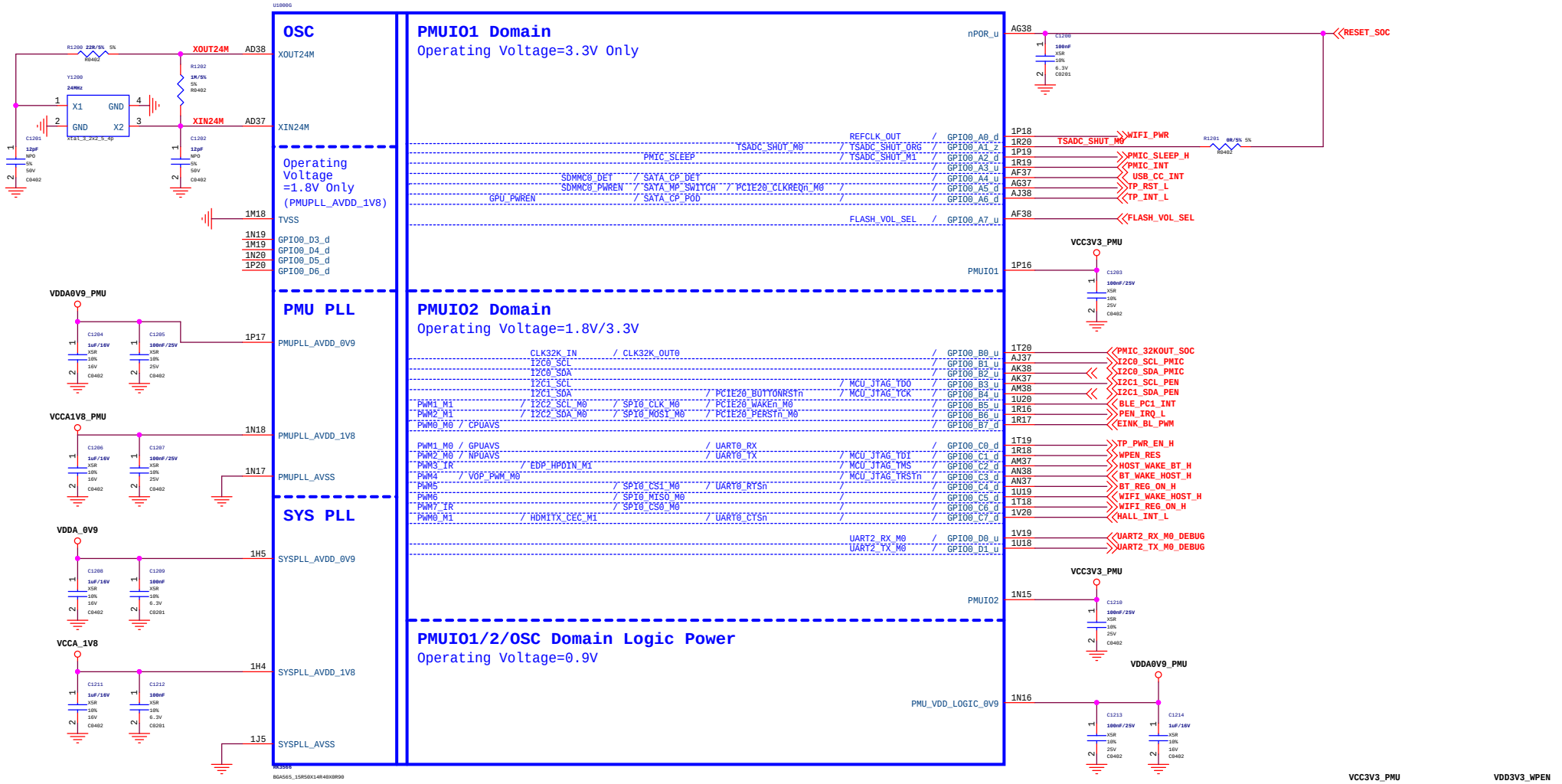
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**10.RK3566_Power/GND**				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	10 of 99

RK3566_F (DDR PHY)



PINE64	PINE64		
Project:	PineNote Mainboard Schematic-20210726		
File:	**11.RK3566_DDR PHY**		
Date:	Monday, July 26, 2021	**Rev:**	V1.1
Designed by:	Daniel.J	**Reviewed by:** Default	**Sheet:** 11 of 99

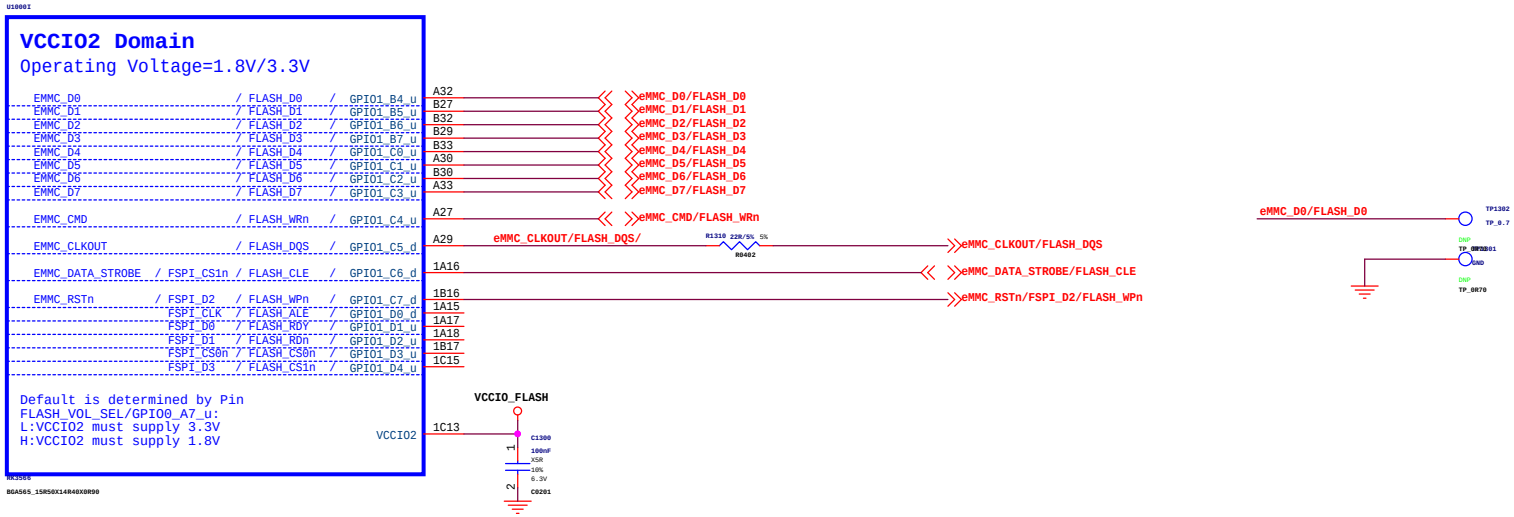
RK3566_G(OSC/PLL/PMUIO1/2)



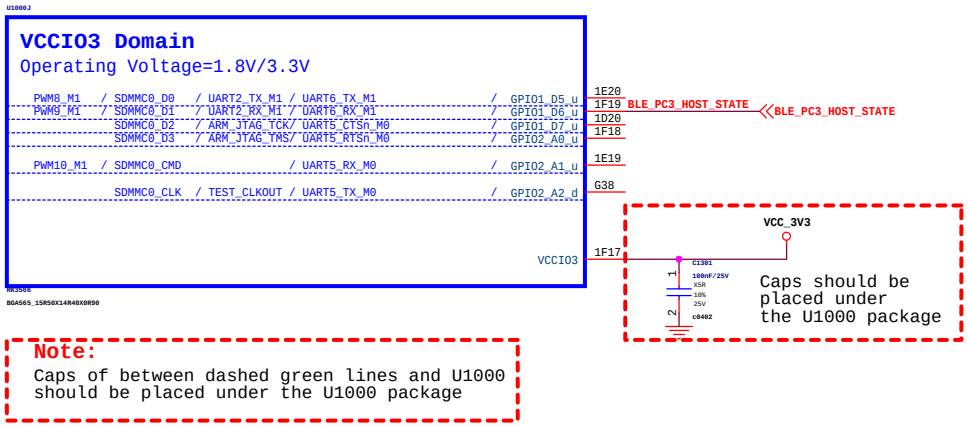
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	12.RK3566_OSC/PLL/PMUIO				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	12 of 99

RK3566_I(VCCIO2 Domain)



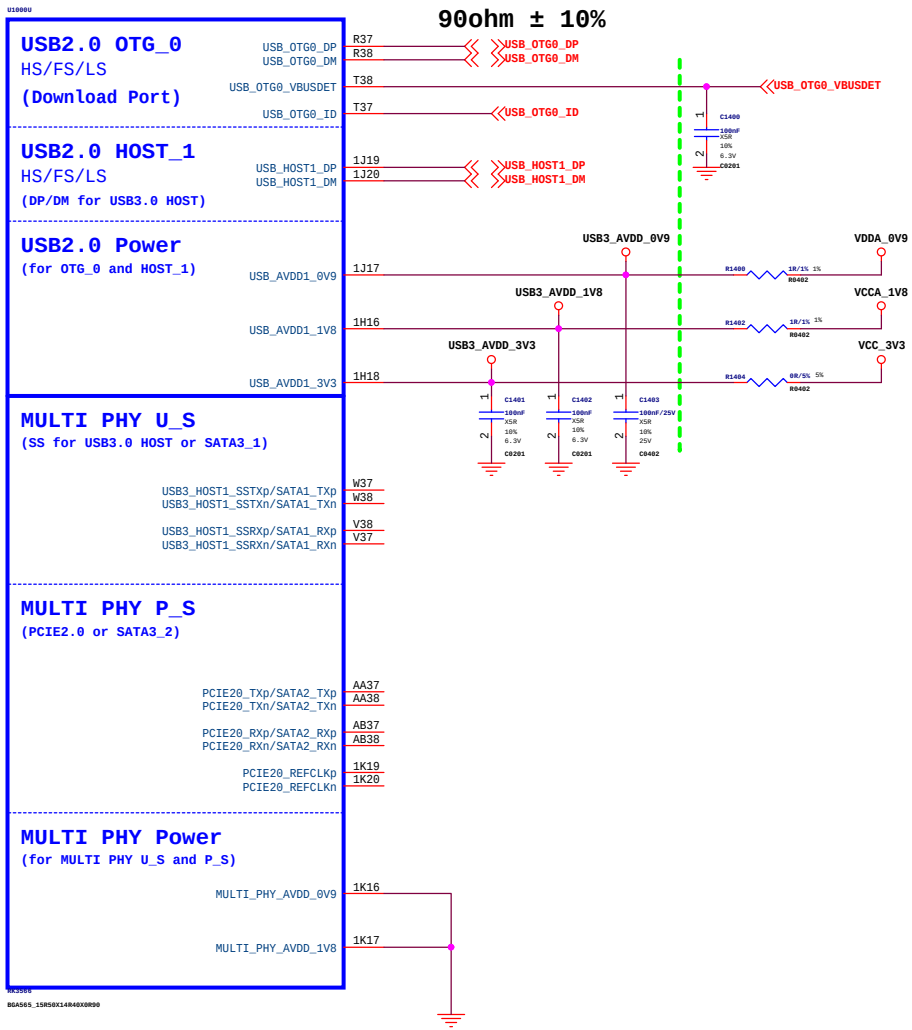
RK3566_J(VCCIO3 Domain)

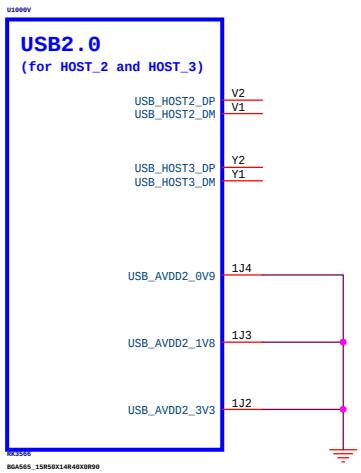


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**13.RK3566_Flash/SD Controller**				
Date:	Monday, July 26, 2021			**Rev:**	V1.1
Designed by:	Daniel.J	**Reviewed by:**	Default	**Sheet:**	13 of 99

RK3566_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



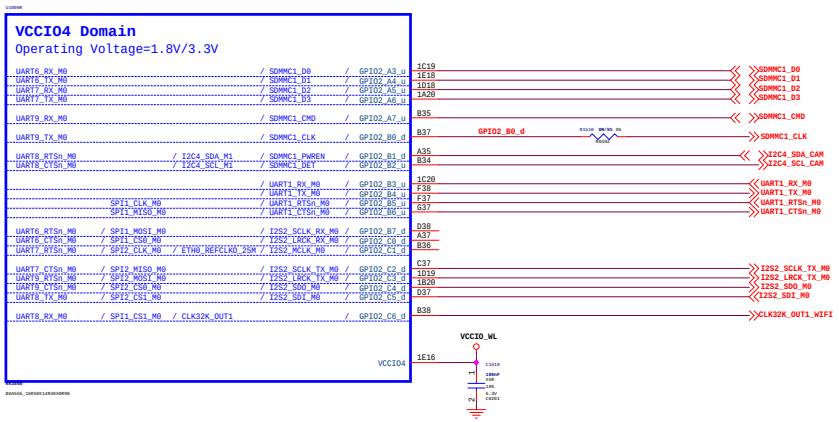


Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3566_V(USB2.0 HOST)

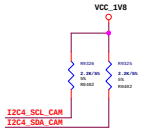
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	14.RK3566_USB/PCIe/SATA PHY				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	14 of 99

RK3566_K(VCCIO4 Domain)



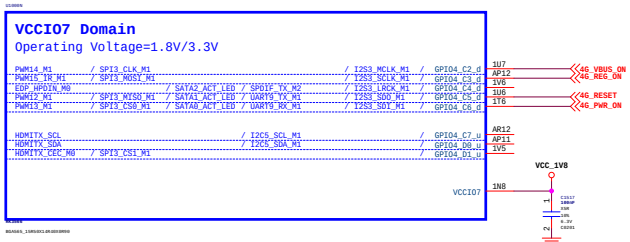
For WIFI

For BT



For BT

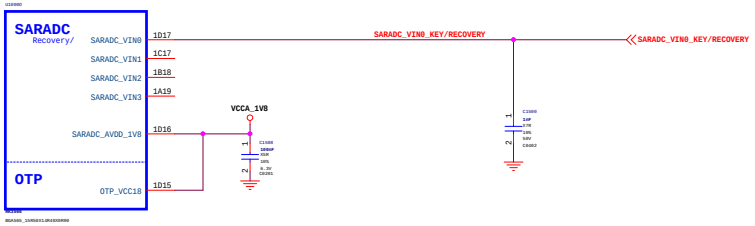
RK3566_N(VCCIO7 Domain)

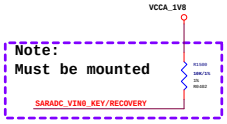


For 4G

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

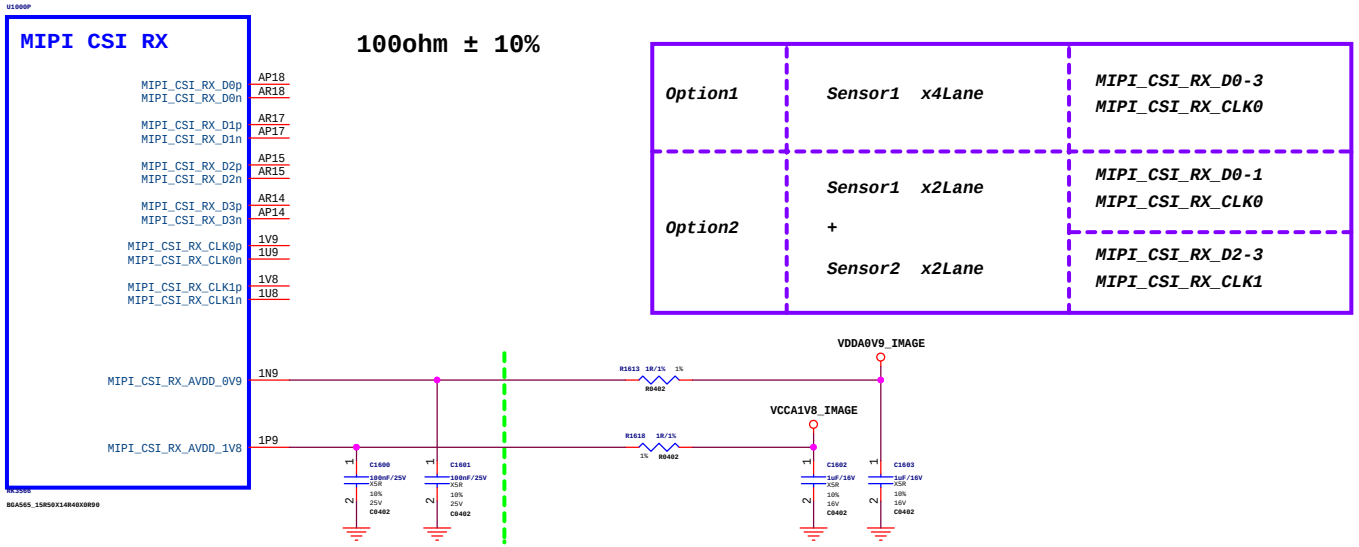
RK3566_O(SARADC/OTP)



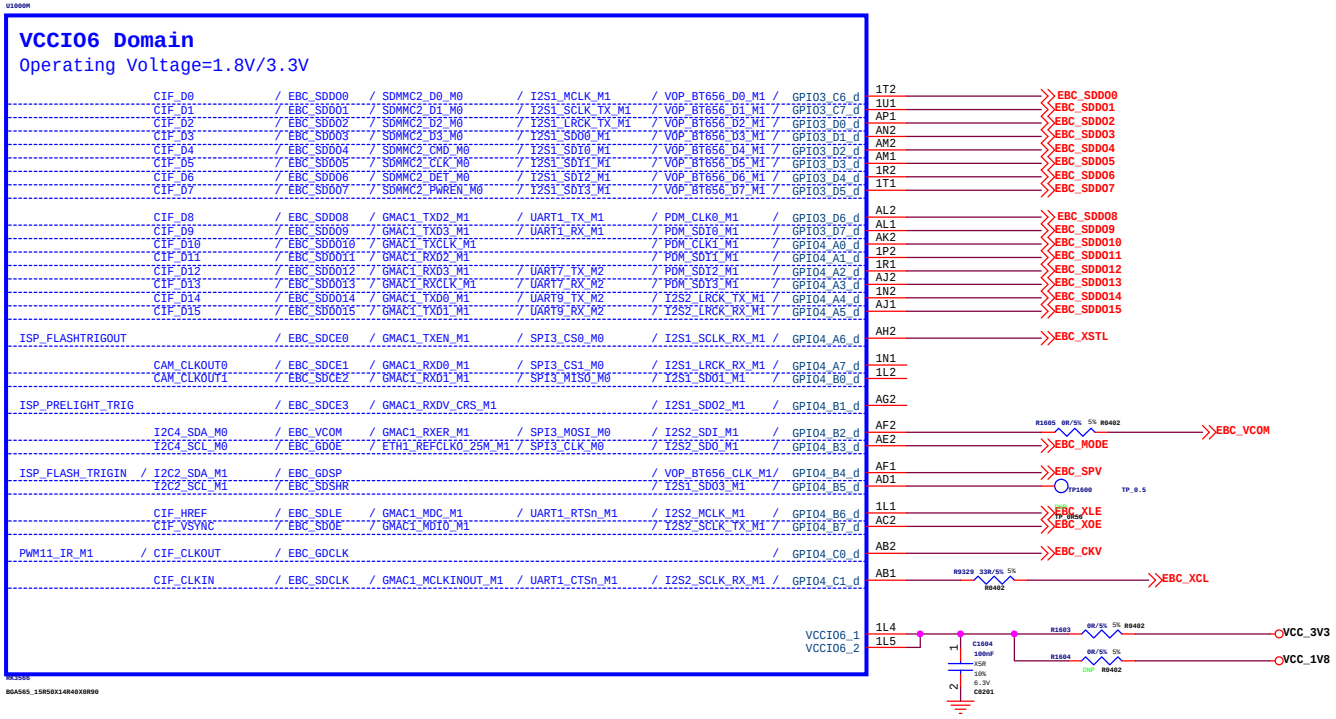


PINE64					
Project:	PineNote Mainboard Schematic-20210726				
File:	15.RK3566_SARADC/GPIO				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	DanielJ	Reviewed by:	Default	Sheet:	15 of 99

RK3566_P(MIPI_CSI_RX)



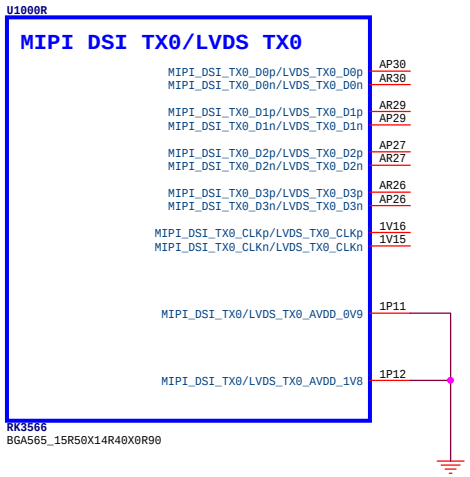
RK3566_M(VCCIO6 Domain)



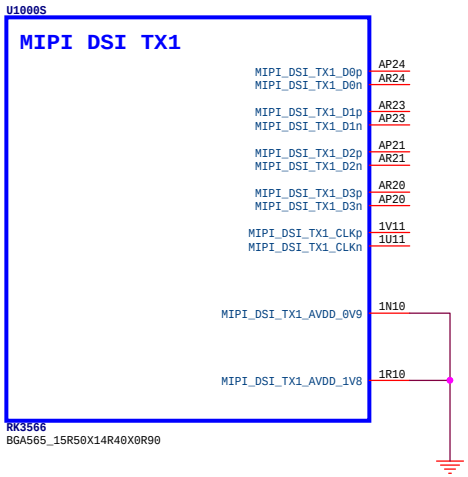
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

PINE64	PINE64			
Project:	PineNote Mainboard Schematic-20210726			
File:	16.RK3566_VI Interface			
Date:	Monday, July 26, 2021		Rev:	V1.1
Designed by:	Daniel.J	Reviewed by: Default	Sheet:	16 of 99

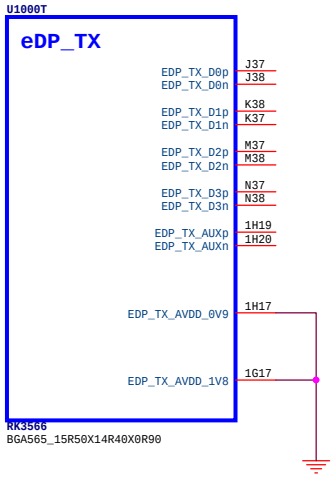
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



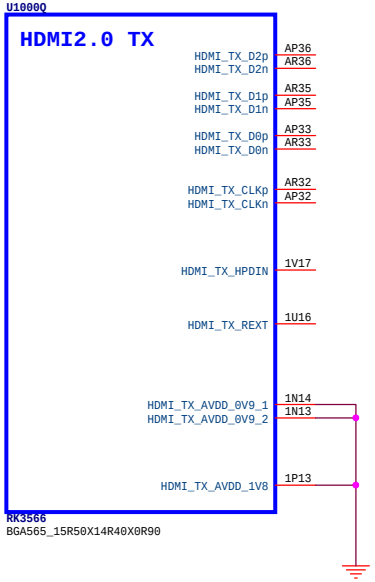
RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP/DP TX)



RK3566_Q(HDMI2.0 TX)



PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	17.RK3566_VO Interface_1				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	17 of 99

RK3566_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

	VOP_BT1120_D0	/ SPI1_CS0_M1			/ SDMMC2_D0_M1	/ GPIO3_A1_d
	VOP_BT1120_D1		/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
	VOP_BT1120_D2		/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
	VOP_BT1120_D3		/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
	VOP_BT1120_D4		/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
	VOP_BT1120_CLK		/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
	VOP_BT1120_D5		/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
	VOP_BT1120_D6		/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
PWM8_M0	/ VOP_BT1120_D7		/ GMAC1_RXD0_M0	/ UART4_RX_M1		/ GPIO3_B1_d
PWM9_M0	/ VOP_BT1120_D8		/ GMAC1_RXD1_M0	/ UART4_TX_M1		/ GPIO3_B2_d
	VOP_BT1120_D9	/ I2C5_SCL_M0	/ GMAC1_RXDV_CRS_M0		/ PDM_SDI0_M2	/ GPIO3_B3_d
	VOP_BT1120_D10	/ I2C5_SDA_M0	/ GMAC1_RXER_M0		/ PDM_SDI1_M2	/ GPIO3_B4_d
PWM10_M0	/ VOP_BT1120_D11	/ I2C3_SCL_M1	/ GMAC1_TXD0_M0			/ GPIO3_B5_d
PWM11_IR_M0	/ VOP_BT1120_D12	/ I2C3_SDA_M1	/ GMAC1_TXD1_M0			/ GPIO3_B6_d
PWM12_M0			/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
PWM13_M0			/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
	VOP_BT1120_D13	/ SPI1_MOSI_M1		/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
	VOP_BT1120_D14	/ SPI1_MISO_M1		/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
	VOP_BT1120_D15	/ SPI1_CLK_M1		/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0		/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0		/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

RK3566

BGA565_15R50X14R40X0R90

1U5 Enc_CLK
AR10 Enc_CS
AP10 Enc_DAT
AR9 — R1800 0R/5% 5% DNP R0402 — EBC_VCOM
AP9 — EBC_PMIC_WAKEUP
1U4 — EBC_PMIC_INT
1V3 — EBC_PMIC_PG

AR7 — EBC_PMIC_ON
AP7 — EBC_PWR_EN
AR6 — GSENSOR_INT_L
AP6 — I2C5_SCL_TP_SEN
1U3 — I2C5_SDA_TP_SEN
1T4 — I2C3_SCL_EMR
1V2 — I2C3_SDA_EMR
AP5 — EMR_PEN_FWE

AR4 BLE_RST_N — BLE_RST_N
AP4 BLE_PB2_DATA — BLE_PB2_DATA
AP3 BLE_PB0_CS — BLE_PB0_CS
AR2 BLE_PB1_CLK — BLE_PB1_CLK

1P3 — SPK_EN
1P4 — LED_CTL

VCCIO5_1 1N5
VCCIO5_2 1N6

VCC_3V3
C1800 100nF/25V X5R 10% 25V C0402

VCC_3V3
R1801 2.2K/5% 5% R0402
R1802 2.2K/5% 5% R0402
I2C3_SCL_EMR
I2C3_SDA_EMR

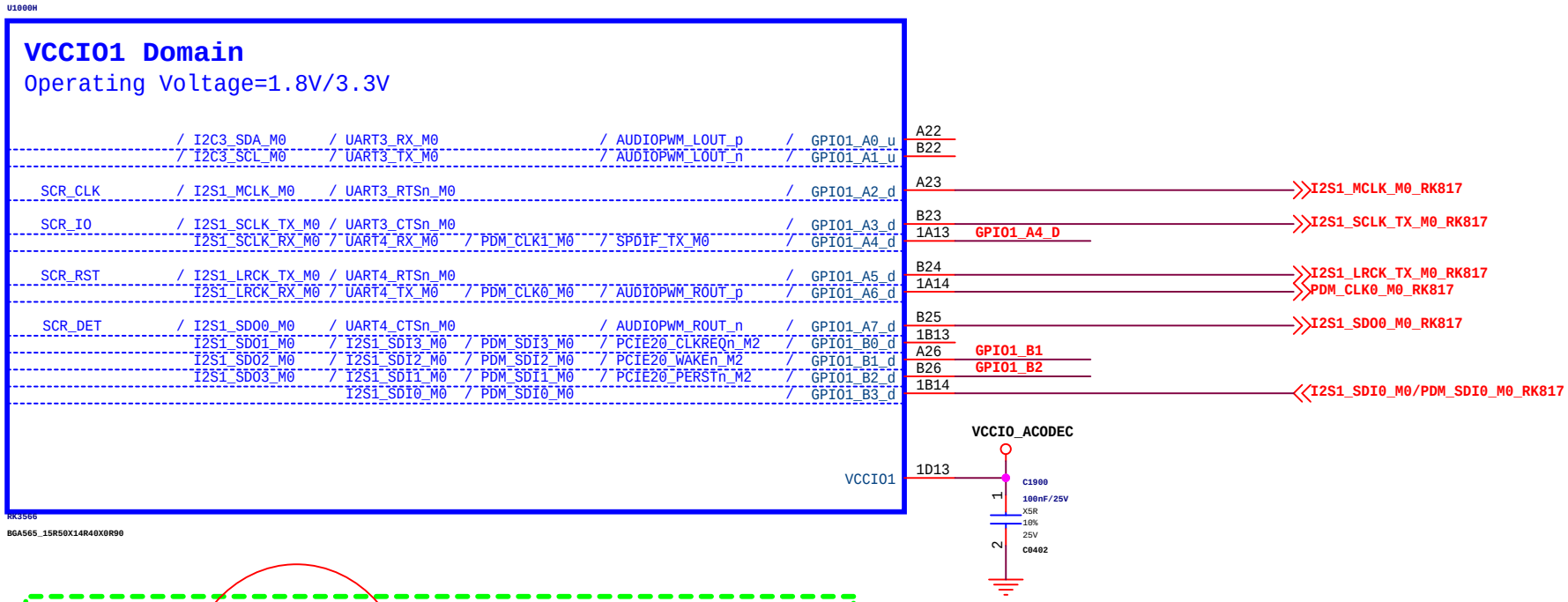
VCC_3V3
R1803 2.2K/5% 5% R0402
R1804 2.2K/5% 5% R0402
I2C5_SCL_TP_SEN
I2C5_SDA_TP_SEN

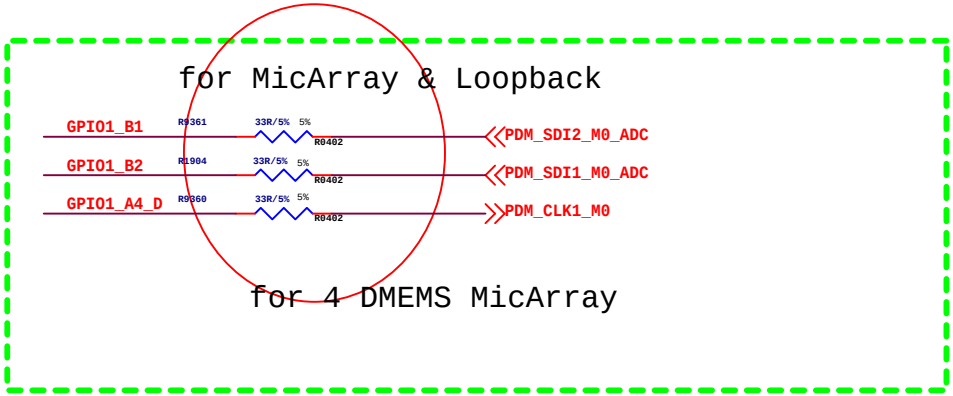
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

VCC_3V3
R9359 47K 5% R0402
R9357 47K 5% R0402
R9358 47K 5% R0402
U9012 XRZ_NX-003(B300) SOT_23_6 DNP
Enc_CLK — 1 CLK
2 GND
Enc_CS — 3 CS
6 DAT — Enc_DAT
5 VDD — VCC_3V3
4 RB3
C9048 100nF/25V X5R 10% 25V C0402

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	18.RK3566_VO Interface_2				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	18 of 99

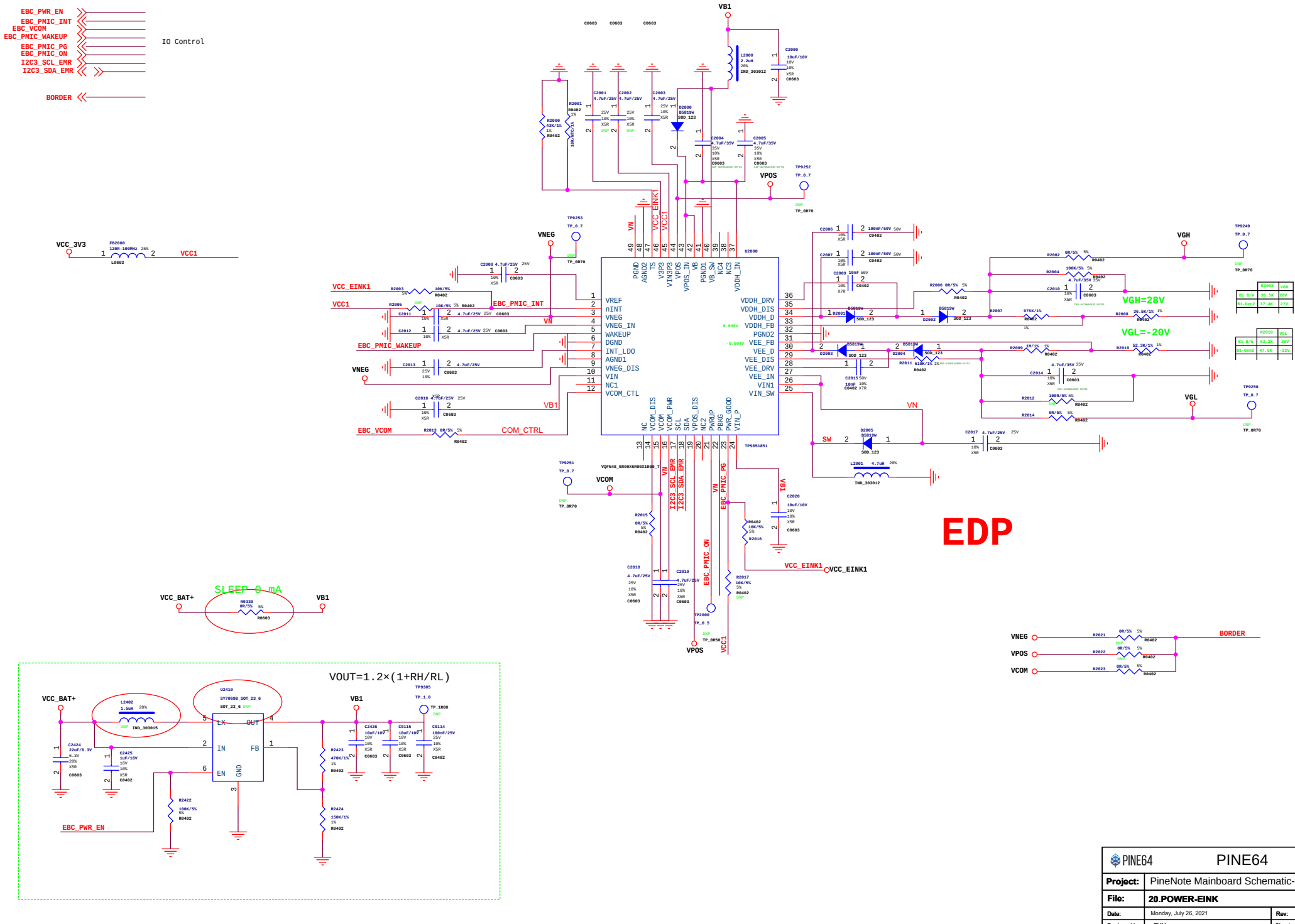
RK3566_H(VCCIO1 Domain)





Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

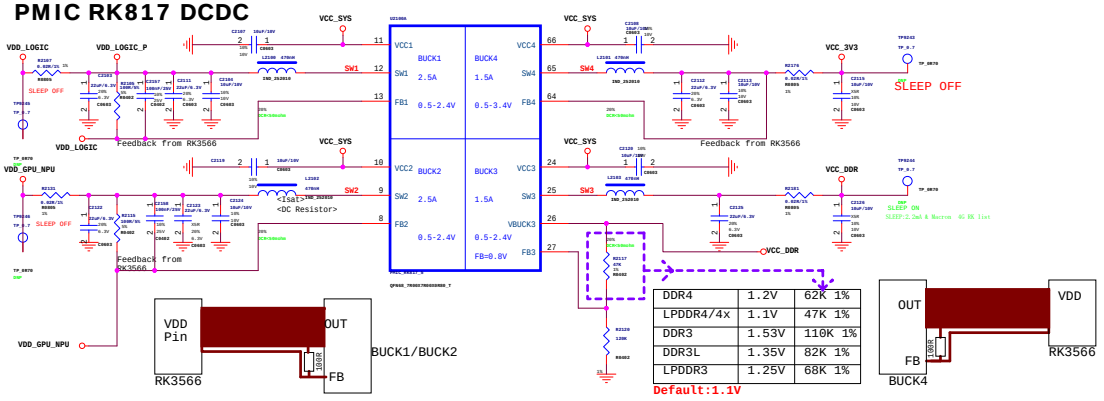
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**19.RK3566_Audio Interface**				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	19 of 99



PINE64	PINE64
Project:	PineNote Mainboard Schematic-20210726
File:	20.POWER-EINK
Date:	Monday, July 26, 2021
Rev:	V1.1
Designed by:	ZHM
Sheet:	20 of 99

I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_INT
PMIC_SLEEP_H
PMIC_SLEEP_PMIC
REST_KEY
PMIC_PWRON
RESET_SOC
PMIC_32KOUT_WIFI
PMIC_32KOUT_SOC
I2S1_MCLK_M0_RK817
I2S1_SCLK_TX_M0_RK817
I2S1_LRCK_TX_M0_RK817
I2S1_SDO0_M0_RK817
SPK_P_L
SPK_N_L
I2S1_SDI0_M0/PDM_SDI0_M0_RK817
PDM_CLK0_M0_RK817
HPL_OUT
HPR_OUT

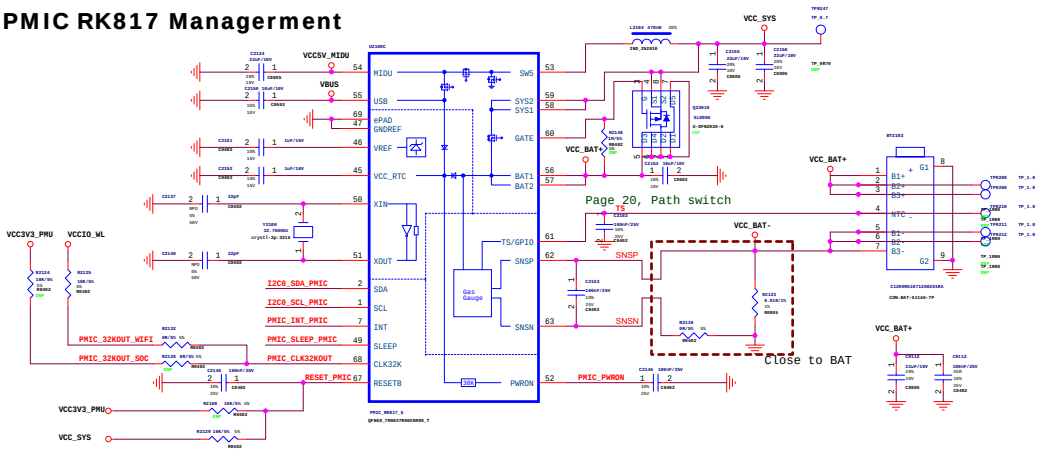
PMIC RK817 DCDC

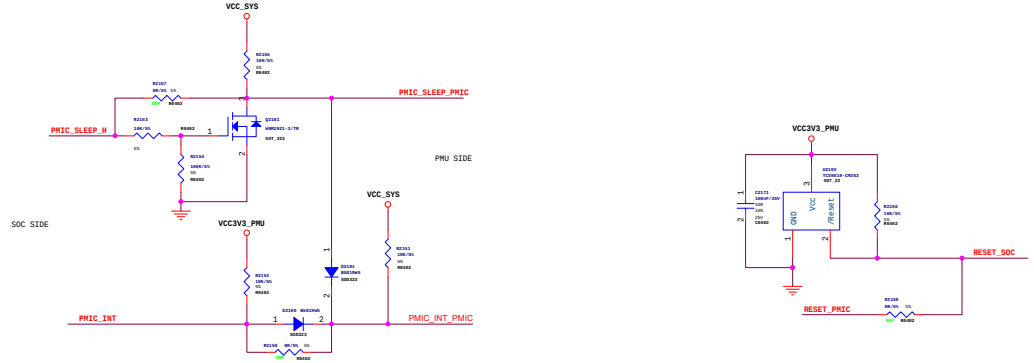


DDR4	1.2V	62K 1%
LPDDR4/4x	1.1V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

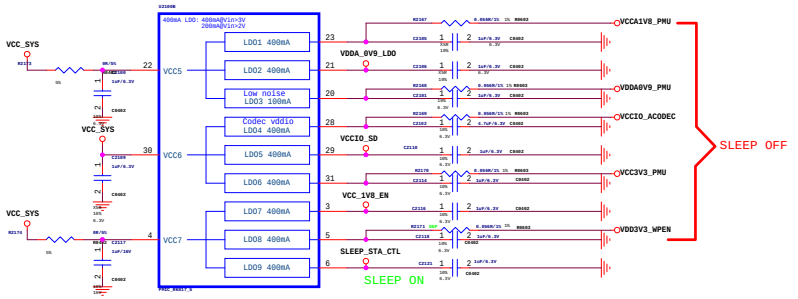
Default:1.1V

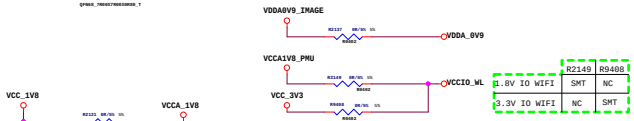
PMIC RK817 Managerment

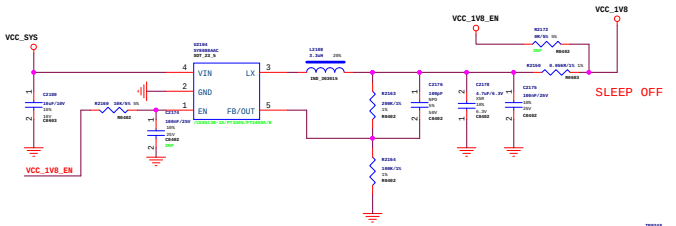


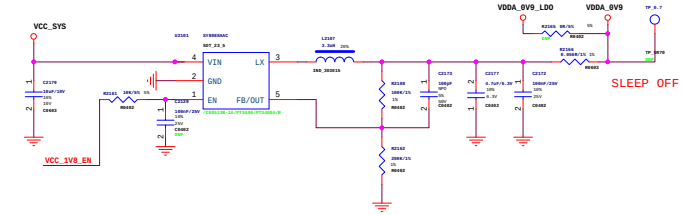


PMIC RK817 LDO

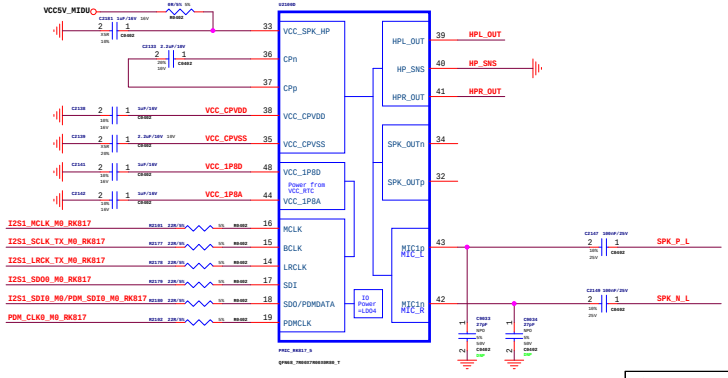








PMIC RK817 CODEC



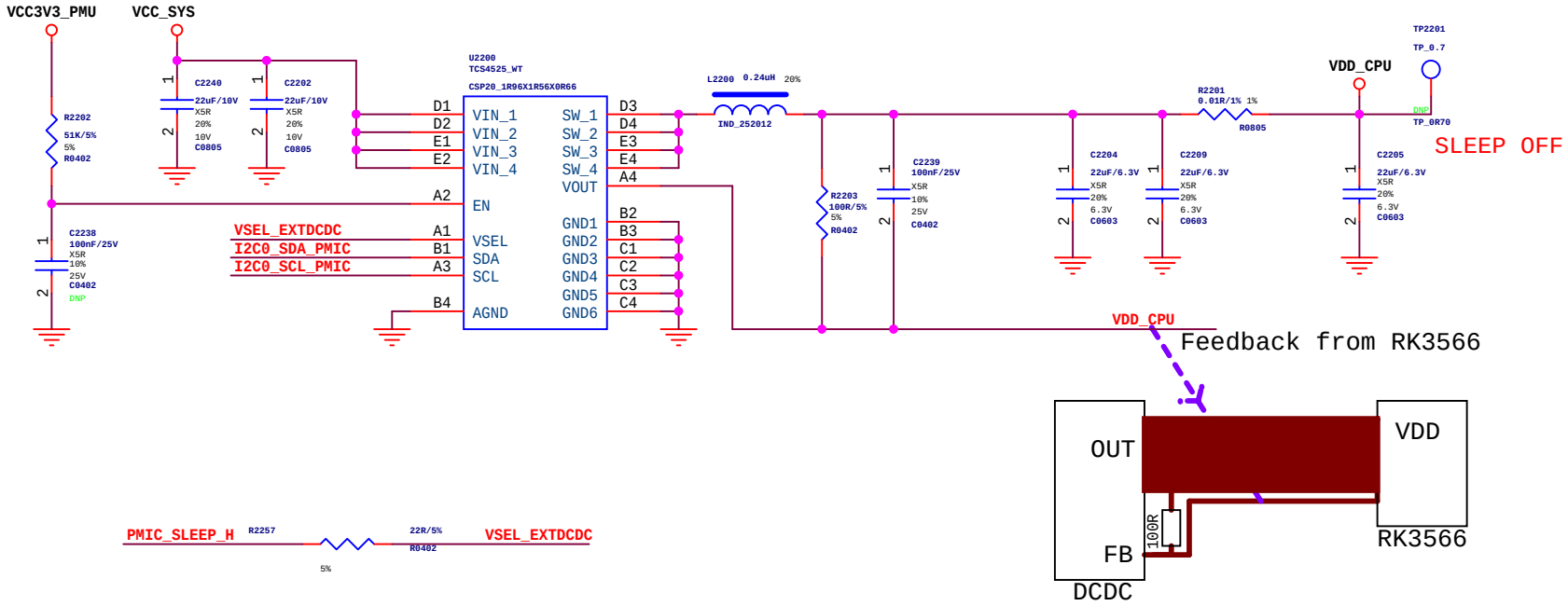
PINE64

Project:	PineNote Mainboard Schematic-20210726
File:	21.Power_PMIC
Date:	Monday, July 26, 2021
Rev:	V1.1
Designed by:	DanielJ
Reviewed by:	Default
Sheet:	21 of 99

I2C0_SCL_PMIC
I2C0_SDA_PMIC

PMIC_SLEEP_H

VDD_CPU_EXT

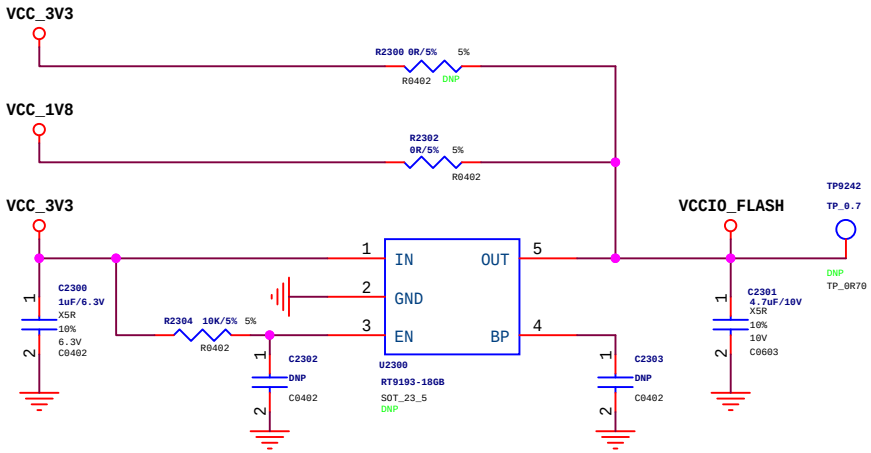


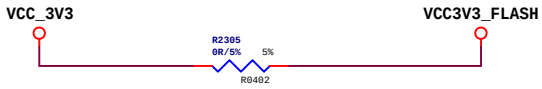
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**22.Power_other**				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	22 of 99

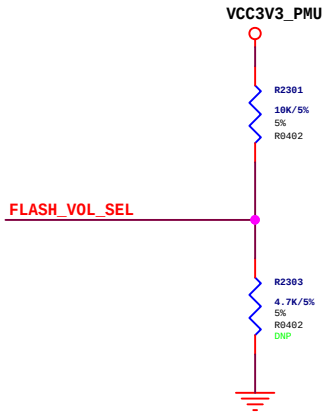
Flash Power Manage

FLASH_VOL_SEL

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)

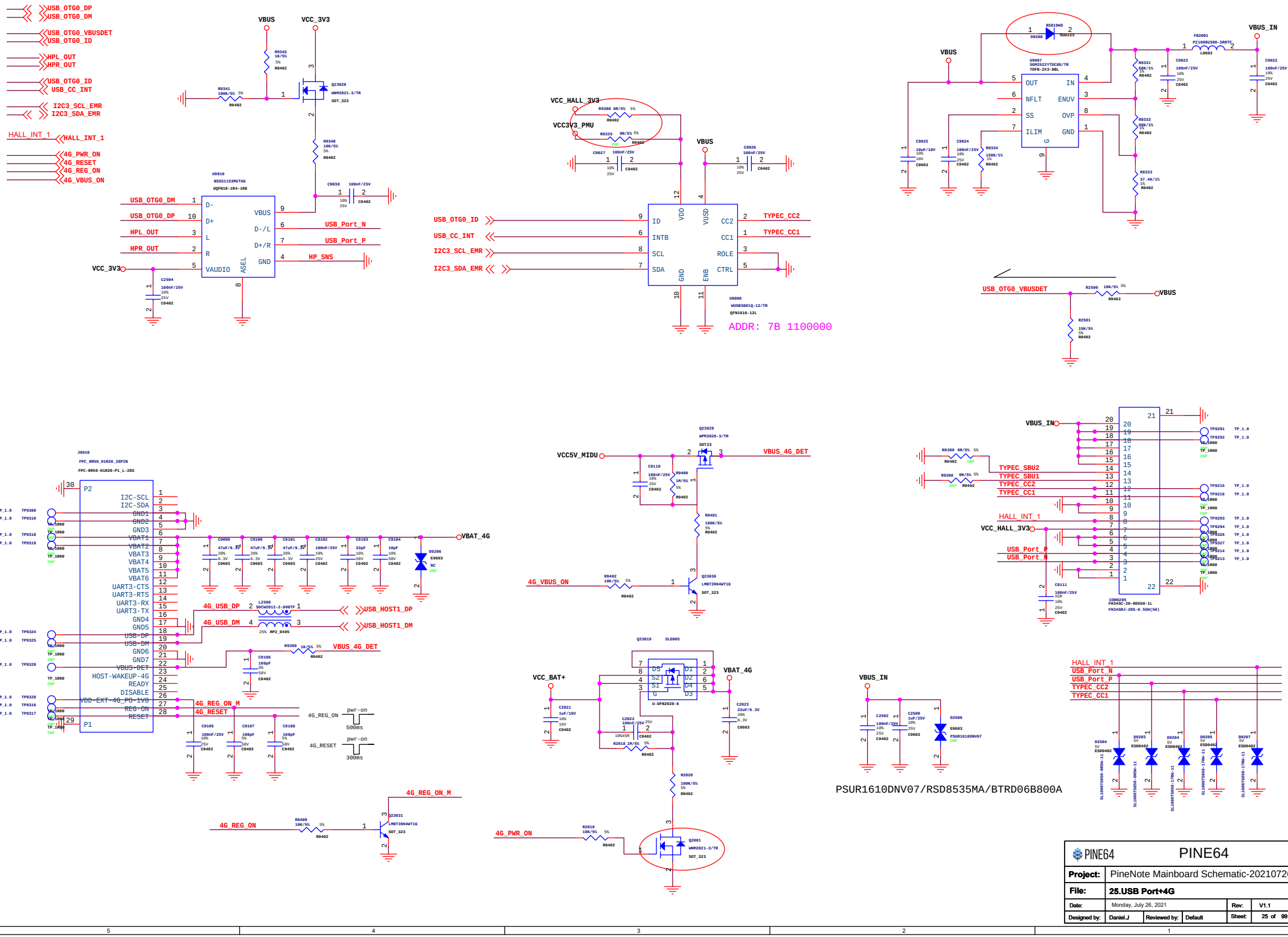


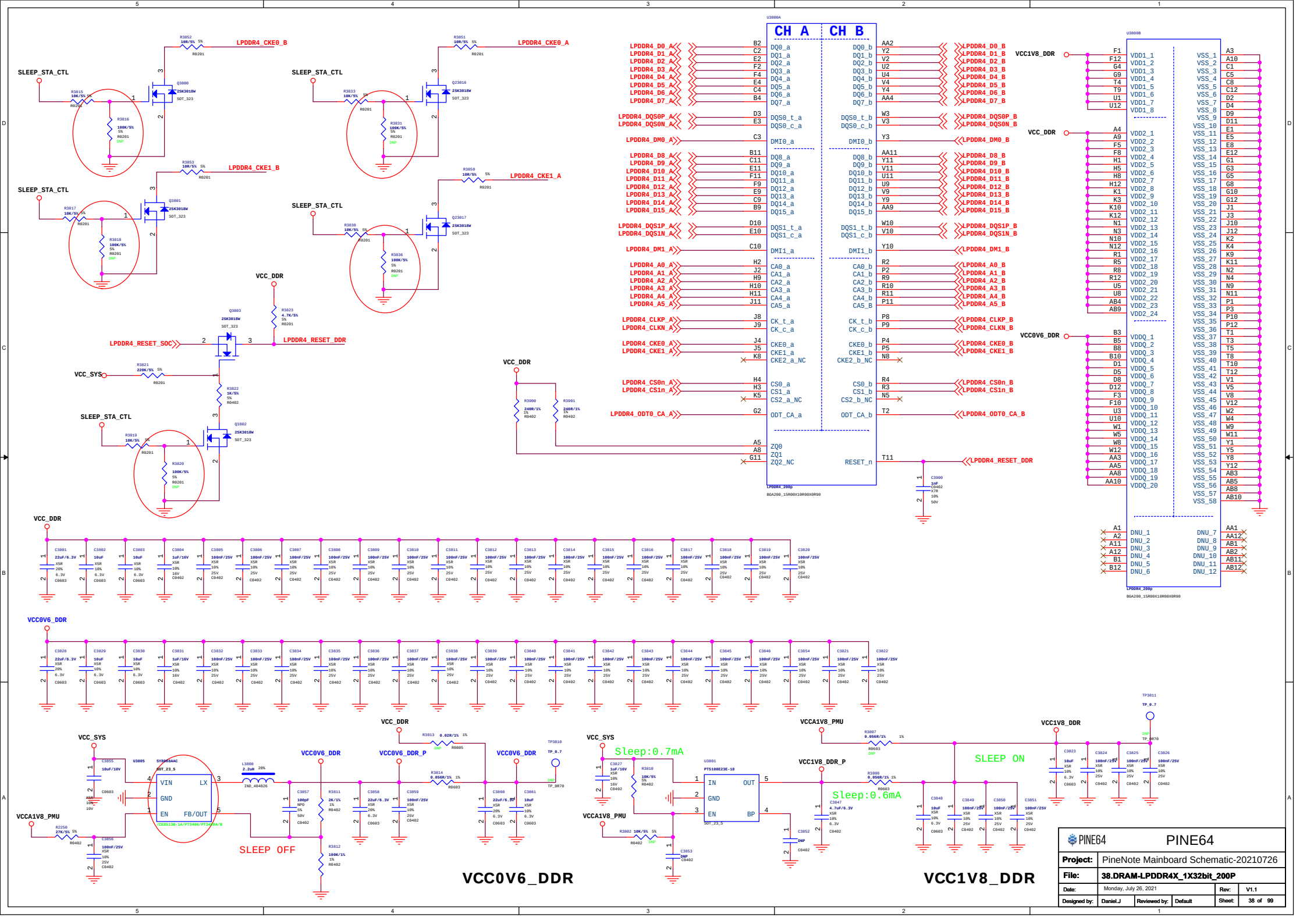


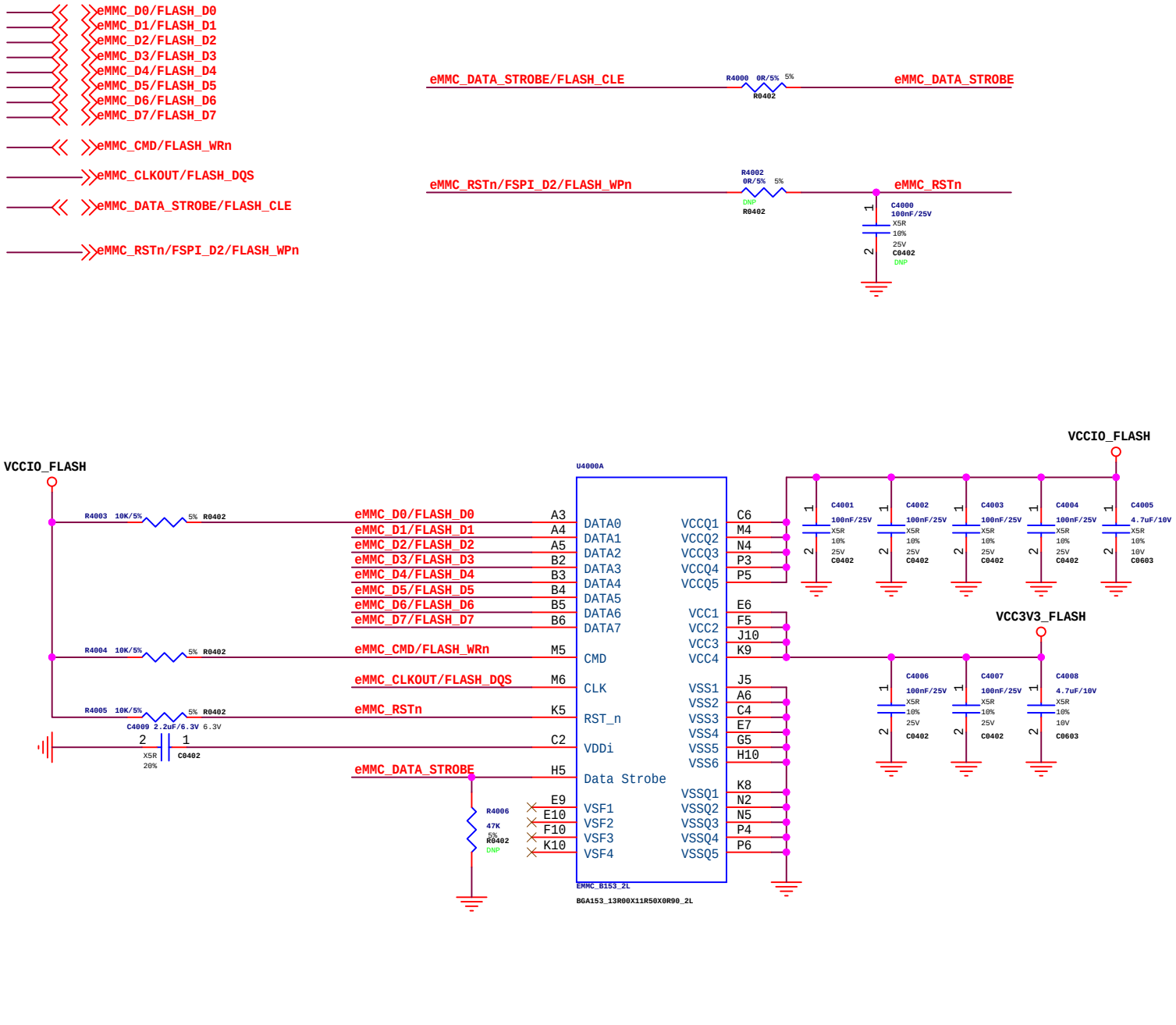


Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	23.Power_Flash Power Manage				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	23 of 99


USB_OTG0_DP
USB_OTG0_DM
USB_OTG0_VBUSDET
USB_OTG0_ID
HPL_OUT
HPR_OUT
USB_OTG0_ID
USB_CC_INT
I2C3_SCL_EMR
I2C3_SDA_EMR
HALL_INT_1
HALL_INT_1
4G_PWR_ON
4G_RESET
4G_REG_ON
4G_VBUS_ON
VBUS
VCC_3V3
R9342 1K/5% R0402
R9341 100K/5% R0402
Q23020 WNM2021-3/TR SOT_323
R9340 10K/5% R0402
C9030 100nF/25V C0402
U9010 NS5511S3MUTAG UQFN10-1R4-1R8
D- D+ L R VAUDIO VBUS D-/L D+/R GND ASEL
USB_OTG0_DM
USB_OTG0_DP
HPL_OUT
HPR_OUT
VCC_3V3
USB_Port_N
USB_Port_P
HP_SNS
C2504 100nF/25V C0402
VCC_HALL_3V3
VCC3V3_PMU
R9388 0R/5% R0402
R9335 0R/5% R0402 DNP
C9027 100nF/25V C0402
C9026 100nF/25V C0402
VBUS
U9008 WUSB3801Q-12/TR QFN1616-12L
ID INTB SCL SDA VDD VUSD GND ENB CC2 CC1 ROLE CTRL
USB_OTG0_ID
USB_CC_INT
I2C3_SCL_EMR
I2C3_SDA_EMR
TYPEC_CC2
TYPEC_CC1
ADDR: 7B 1100000
D9208 BS819WS SOD323
VBUS
U9007 SGM2522YTDC8G/TR TDFN-2X3-8BL
OUT NFLT SS ILIM IN ENUV OVP GND
R9331 68K/1% R0402
R9333 68K/1% R0402
R9332 97.4K/1% R0402
R9334 150K/1% R0402
C9025 10uF/10V C0603
C9024 100nF/25V C0402
C9023 100nF/25V C0402
FB2001 PZ1608U300-3R0TF L0603
VBUS_IN
C9022 100nF/25V C0402
USB_OTG0_VBUSDET
R2500 10K/5% R0402
R2501 15K/5% R0402
VBUS
J6010 FPC_0R50_H1R20_28PIN FPC-0R50-H1R20-P1_L-28S
P2 P1
I2C-SCL I2C-SDA GND1 GND2 GND3 VBAT1 VBAT2 VBAT3 VBAT4 VBAT5 VBAT6 UART3-CTS UART3-RTS UART3-RX UART3-TX GND4 GND5 USB-DP USB-DM GND6 GND7 VBUS-DET HOST-WAKEUP-4G READY DISABLE VDD_EXT_4G_PD_1V8 REG-ON RESET
C9099 47uF/6.3V C0603
C9100 47uF/6.3V C0603
C9101 47uF/6.3V C0603
C9102 100nF/25V C0402
C9103 33pF C0402
C9104 10pF C0402
D9206 E0603 NC DNP
VBAT_4G
4G_USB_DP
4G_USB_DM
L2500 SDCW2012-2-900TF
RP2_0405
USB_HOST1_DP
USB_HOST1_DM
R9399 1K/5% R0402
VBUS_4G_DET
C9106 100pF C0402
4G_REG_ON_M
4G_RESET
C9105 100nF/25V C0402
C9107 100pF C0402
C9108 100pF C0402
4G_REG_ON pwr-on 500ms
4G_RESET pwr-on 300ms
4G_REG_ON_M
4G_REG_ON
R9409 10K/5% R0402
Q23031 LMBT3904WT1G SOT_323
VCC5V_MIDU
Q23029 WPM2026-3/TR SOT23
C9110 100nF/25V C0402
R9400 1M/5% R0402
R9401 100K/5% R0402
4G_VBUS_ON
R9402 10K/5% R0402
Q23030 LMBT3904WT1G SOT_323
VBUS_4G_DET
VCC_BAT+
Q23019 SLD905
U-DFN2020-6
C2021 1uF/16V C0402
C2022 100nF/25V C0402
R2018 1K/5% R0402
R2020 100K/5% R0402
C2023 22uF/6.3V C0603
VBAT_4G
4G_PWR_ON
R2019 10K/5% R0402
Q2001 WNM2021-3/TR SOT_323
VBUS_IN
C2502 100nF/25V C0402
C2500 1uF/25V C0603
D2506 E0603 PSUR1610DNV07 DNP
PSUR1610DNV07/RSD8535MA/BTRD06B800A
VBUS_IN
R9389 0R/5% R0402 DNP
R9390 0R/5% R0402 DNP
TYPEC_SBU2
TYPEC_SBU1
TYPEC_CC2
TYPEC_CC1
HALL_INT_1
VCC_HALL_3V3
USB_Port_P
USB_Port_N
C9111 100nF/25V X5R C0402
CON9205 FH34SC-20-0D5SH-1L FH34SRJ-20S-0.5SH(50)
TP9291 TP9292 TP9215 TP9216 TP9293 TP9294 TP9226 TP9227 TP9224 TP9213
HALL_INT_1
USB_Port_N
USB_Port_P
TYPEC_CC2
TYPEC_CC1
D2504 D2503 D2504 D9205 D9207
SL1006TS050-0R5U-11
SL1006TS050-1R7U-11
PINE64
PINE64
Project: PineNote Mainboard Schematic-20210726
File: 25.USB Port+4G
Date: Monday, July 26, 2021
Rev: V1.1
Designed by: Daniel.J
Reviewed by: Default
Sheet: 25 of 99


SLEEP_STA_CTL
LPDDR4_CKE0_B
LPDDR4_CKE0_A
LPDDR4_CKE1_B
LPDDR4_CKE1_A
VCC_DDR
LPDDR4_RESET_SOC
LPDDR4_RESET_DDR
VCC_SYS
CH A
CH B
VCC1V8_DDR
VCC0V6_DDR
VCC0V6_DDR_P
VCCA1V8_PMU
SLEEP OFF
SLEEP ON
Sleep:0.7mA
Sleep:0.6mA
VCC0V6_DDR
VCC1V8_DDR
PINE64
Project: PineNote Mainboard Schematic-20210726
File: 38.DRAM-LPDDR4X_1X32bit_200P
Date: Monday, July 26, 2021
Rev: V1.1
Designed by: Daniel.J
Reviewed by: Default
Sheet: 38 of 99

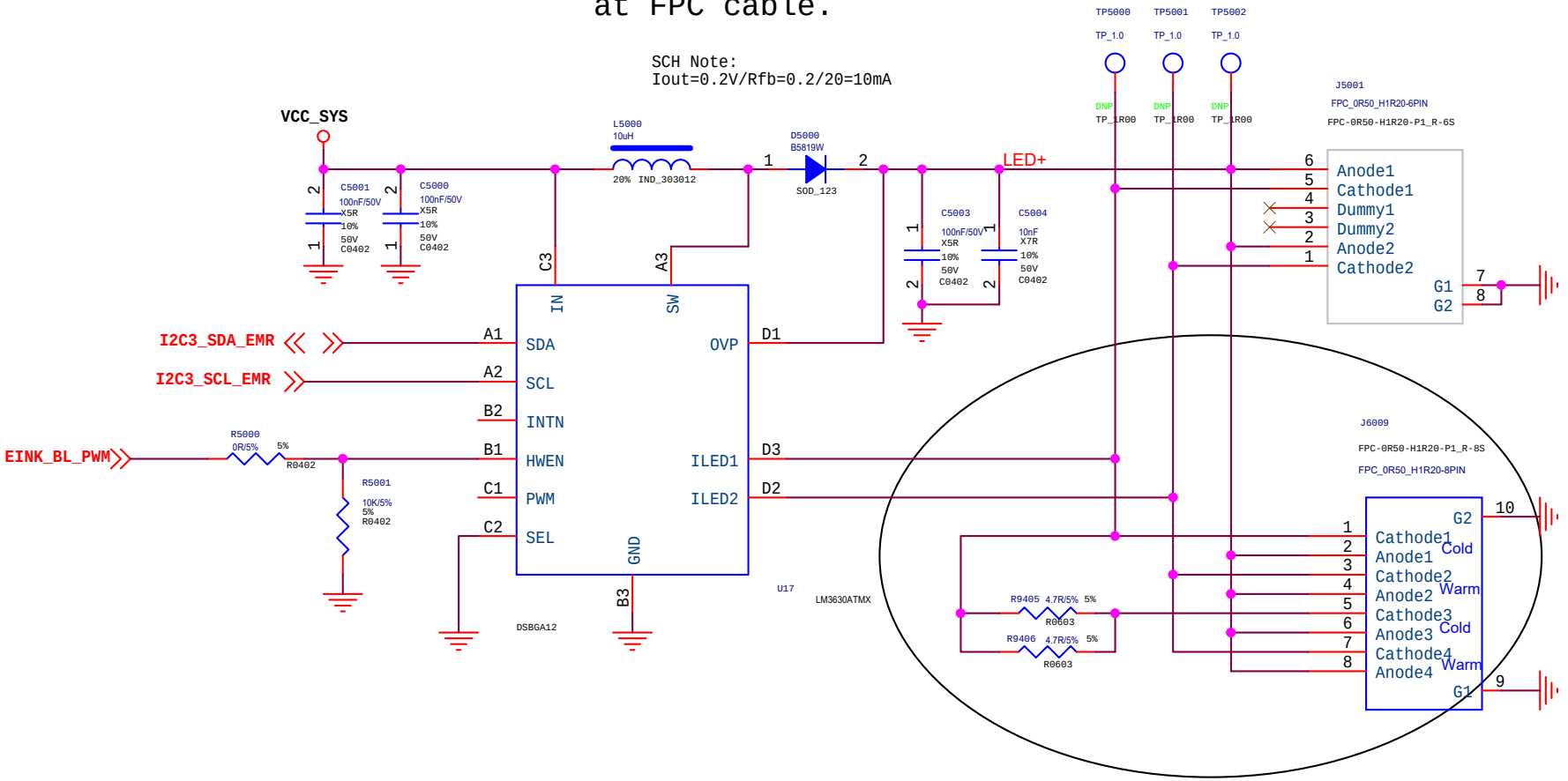


Rockchip Confidential

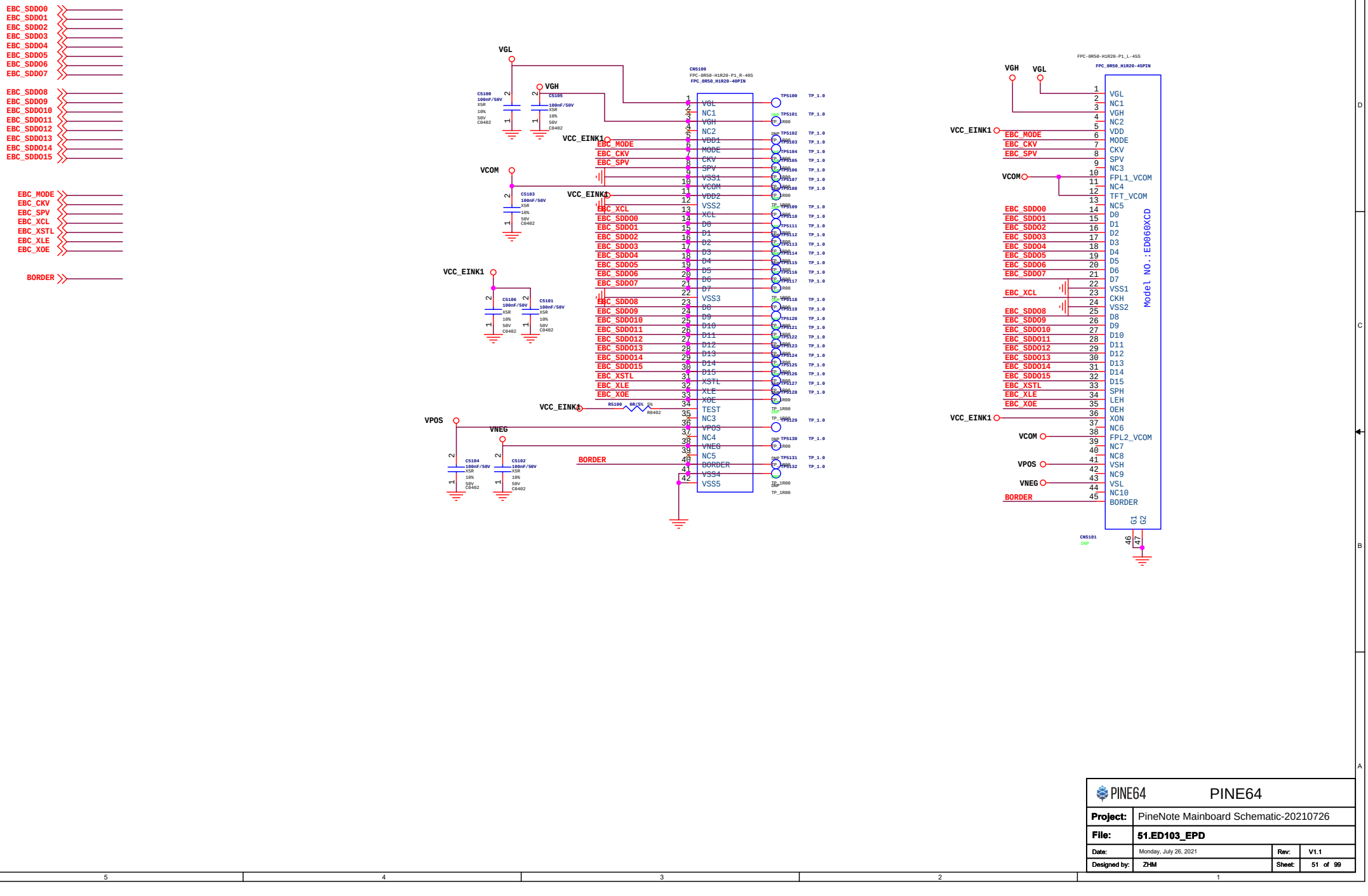
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**40.Flash-eMMC Flash**				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	40 of 99

Dual Cod/Warm light control, Front Light IC at FPC cable.

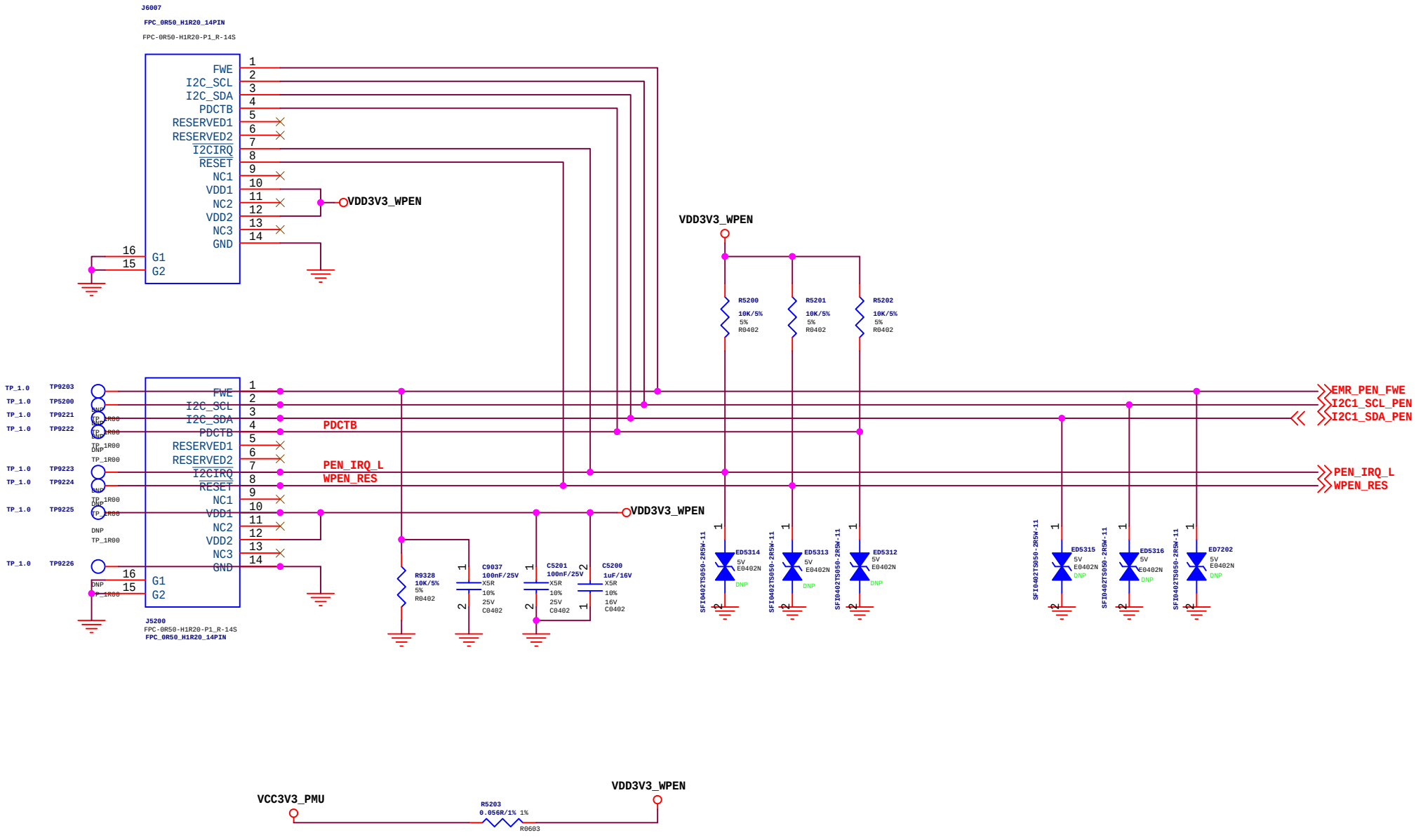
SCH Note:
Iout=0.2V/Rfb=0.2/20=10mA



PINE64	PINE64		
Project:	PineNote Mainboard Schematic-20210726		
File:	**50.Front Light**		
Date:	Monday, July 26, 2021	Rev:	V1.1
Designed by:	ZHM	Sheet:	50 of 99



PINE64	PINE64		
Project:	PineNote Mainboard Schematic-20210726		
File:	**51_ED103_EPD**		
Date:	Monday, July 26, 2021	**Rev:**	V1.1
Designed by:	ZHM	**Sheet:**	51 of 99



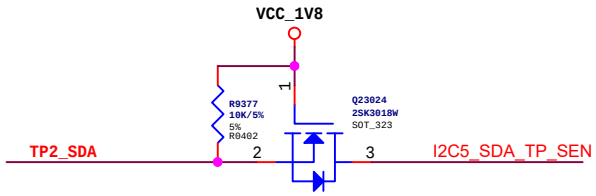
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**52.EMR**				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	52 of 99

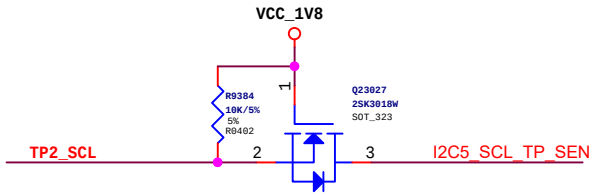
COF

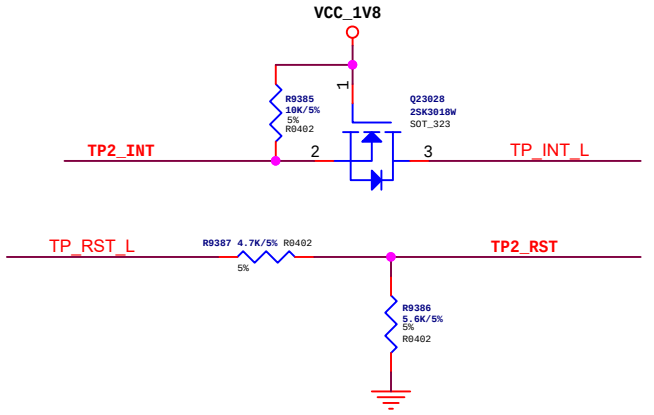
TP IO 电源域3.3V

TP_PWR_EN_H
TP_INT_L
TP_RST_L

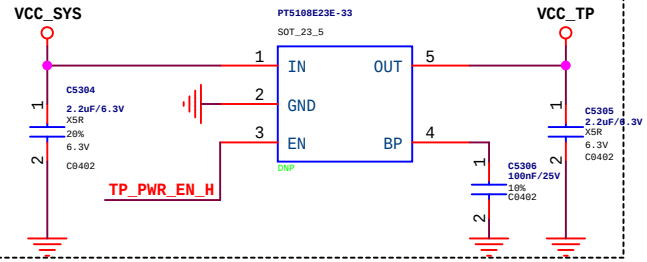
I2C5_SCL_TP_SEN
I2C5_SDA_TP_SEN

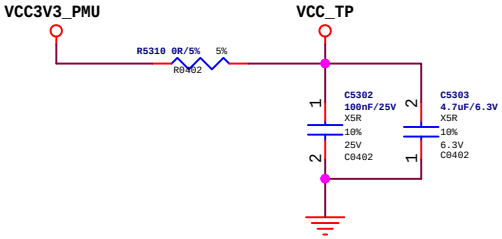


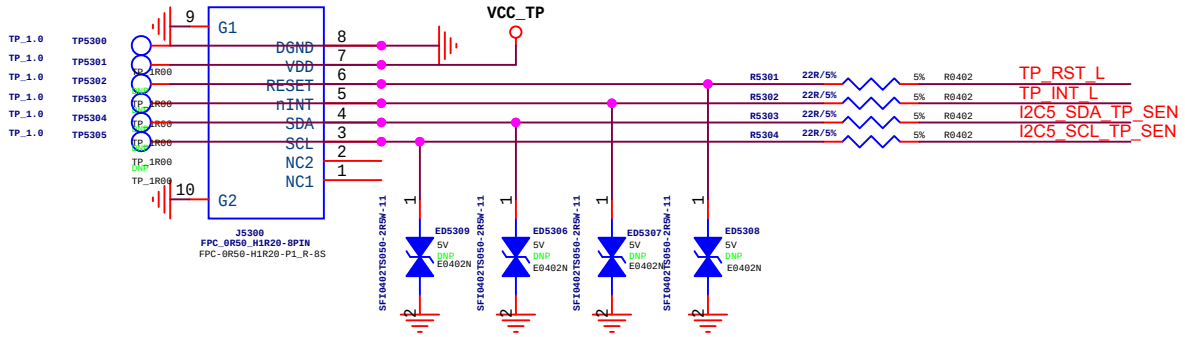


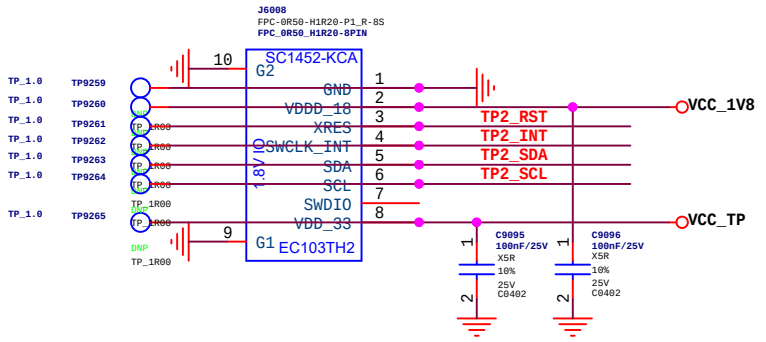


TP的休眠功耗如果小的话，可以直接用VCC_3V3_PMU供电的。通常在100uA左右否则需要外挂LDO



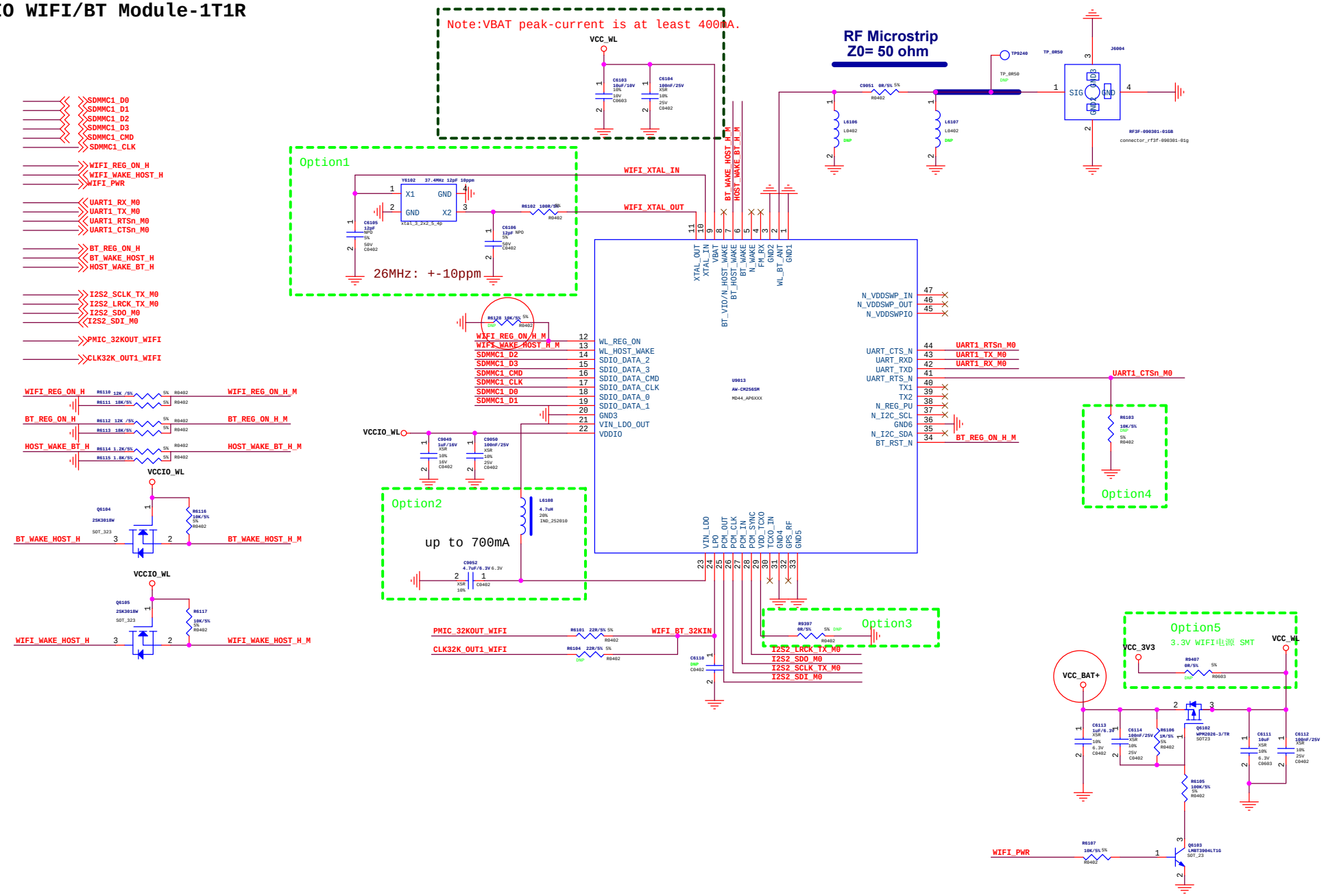




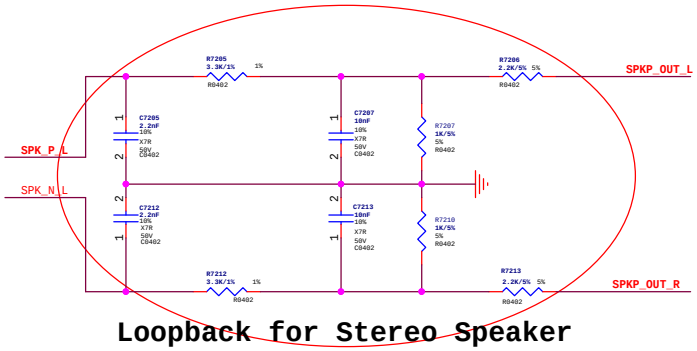


PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**53.TP**				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	1 of 38

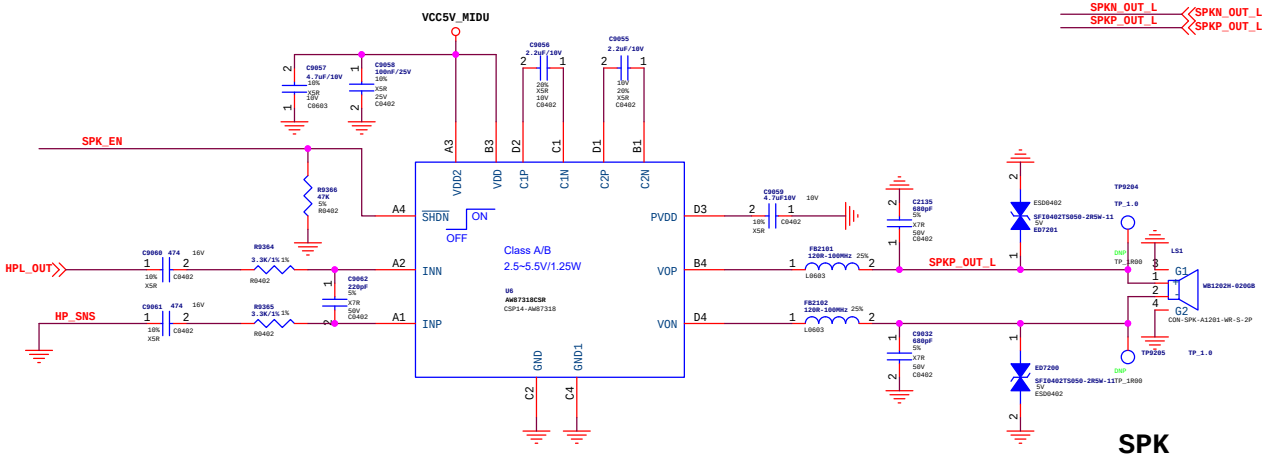
SDIO WIFI/BT Module-1T1R

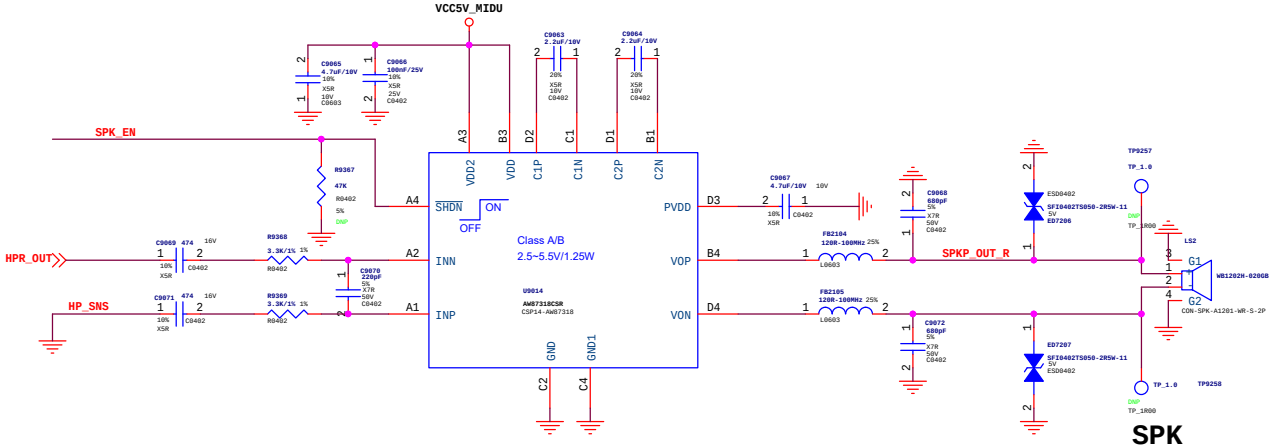


PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	61.WIFI/BT-SDIO_1T1R				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Linus.Lin	Reviewed by:		Sheet:	1 of 38



Loopback for Stereo Speaker





SPK_P_L
SPK_N_L
HPL_OUT
HPR_OUT
SPKN_OUT
SPKP_OUT
SPK_EN

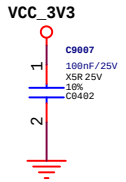
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	70.Audio-SPK				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	70 of 99

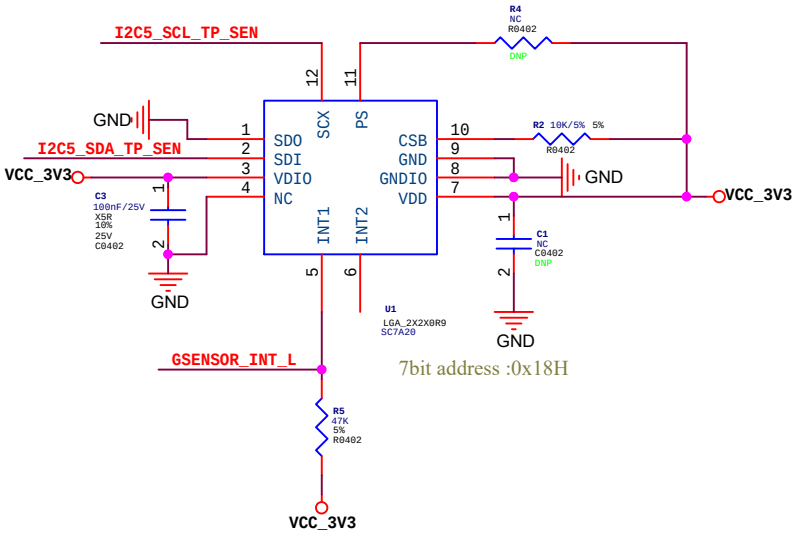
PMIC_SLEEP_PMIC

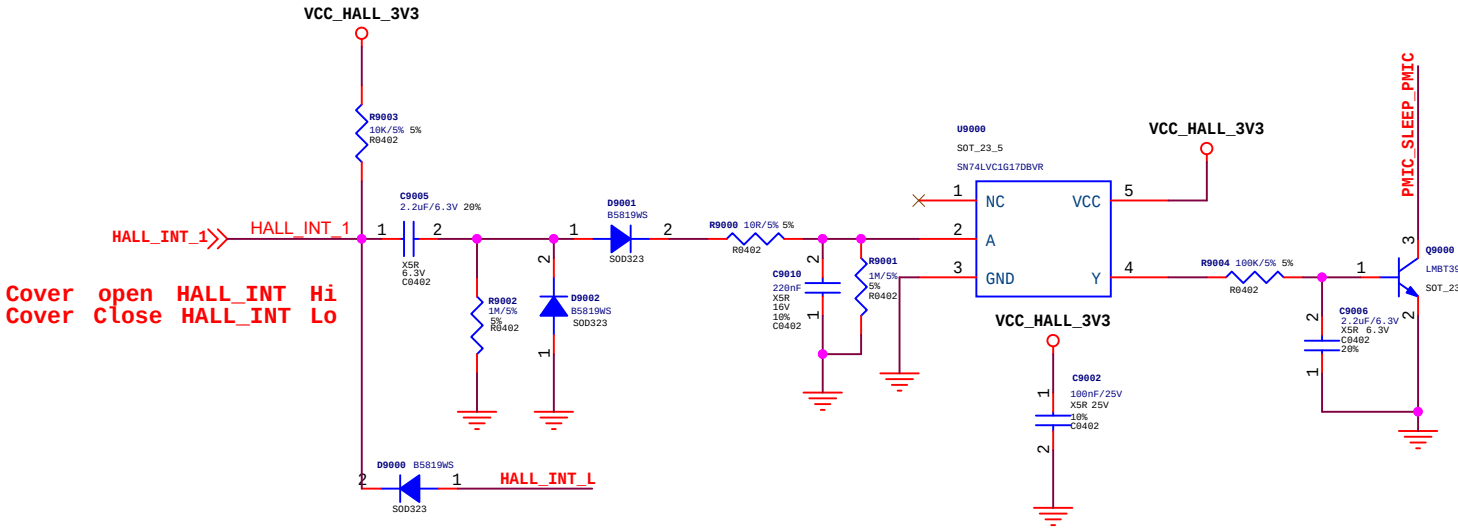
I2C5_SCL_TP_SEN
I2C5_SDA_TP_SEN

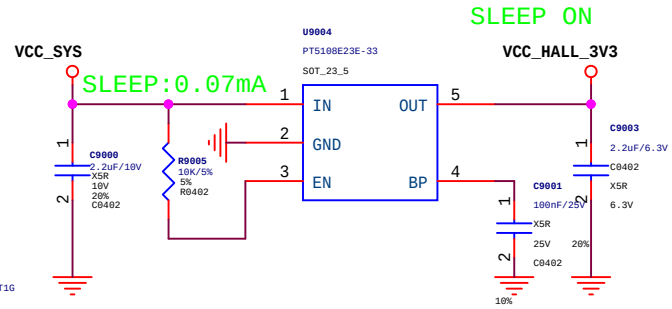
GSENSOR_INT_L

HALL_INT_L





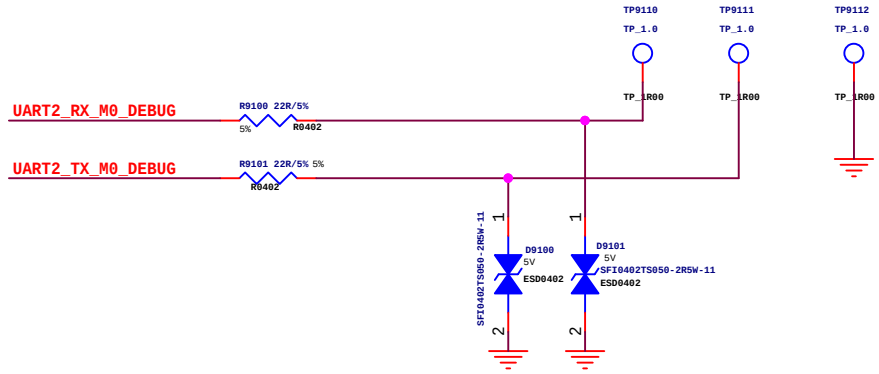




PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**90.Sensor/HALL**				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	90 of 99

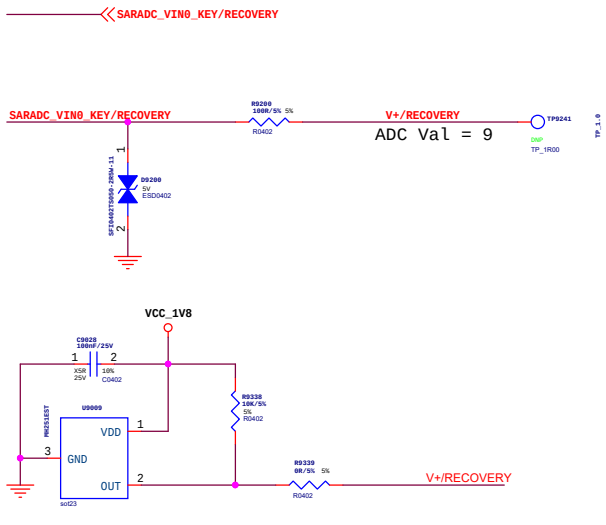
UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG

Debug UART2



PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**91.Debug UART**				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	91 of 99

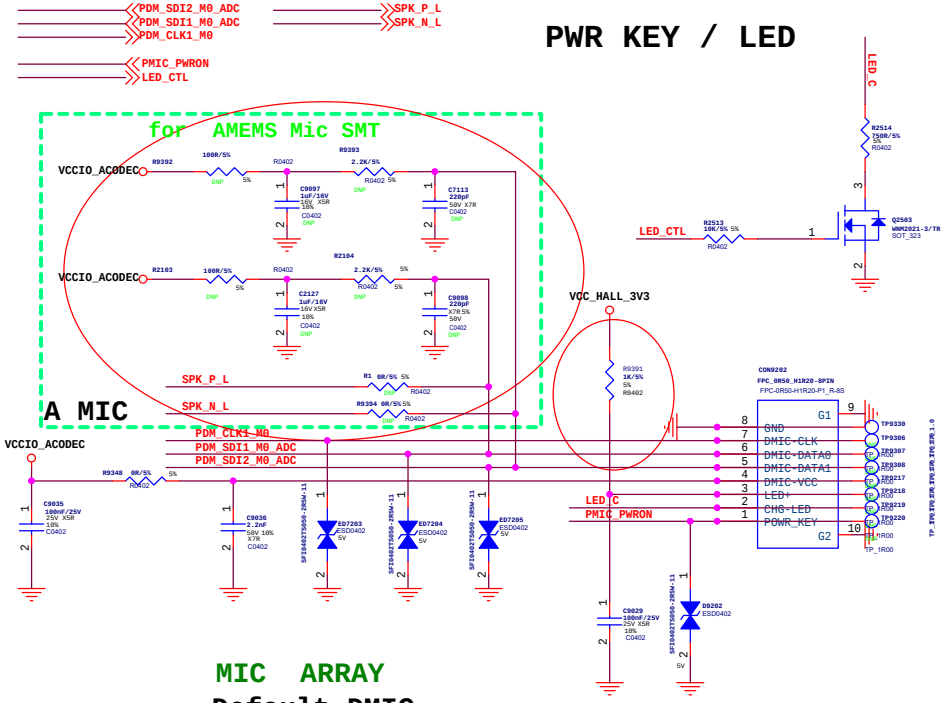
ADC KEY



FOR UPDATE

Update

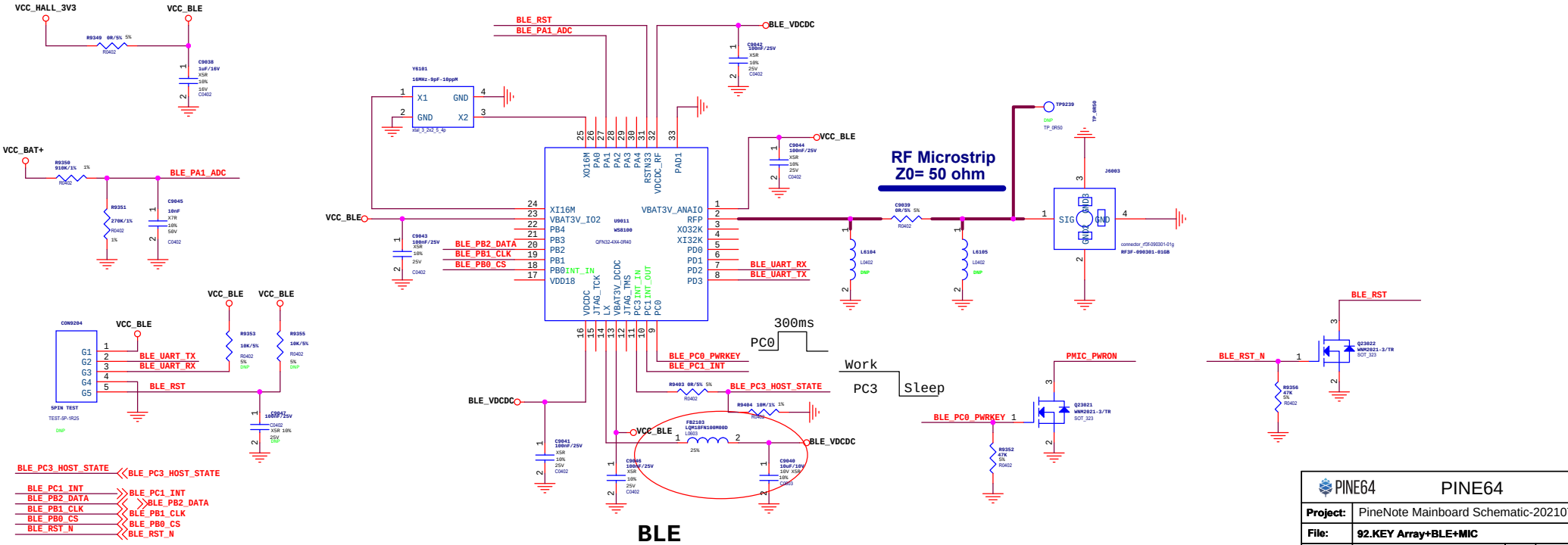
PWR KEY / LED



MIC ARRAY

Default DMIC

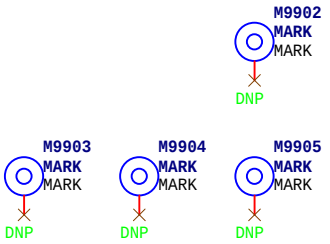
BLE

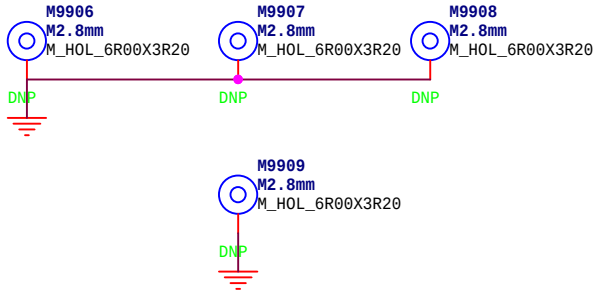


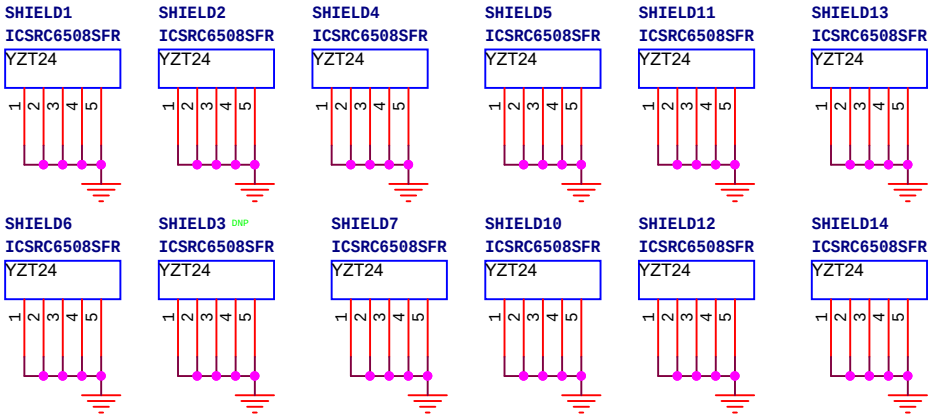
PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**92.KEY Array+BLE+MIC**				
Date:	Monday, July 26, 2021			**Rev:**	V1.1
Designed by:	Daniel.J	**Reviewed by:**	Default	**Sheet:**	92 of 99

Page of Accessories

PCB Mark Point







Heatsink

When use socket,
NO Heatsink holes is reserved.

PINE64	PINE64				
Project:	PineNote Mainboard Schematic-20210726				
File:	**99.Mark/Hole/Heatsink**				
Date:	Monday, July 26, 2021			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	99 of 99