VGA CMOS Image Sensor

BF3703

Datasheet

Revision History

Revised. Date	Revision	Brief Description	Author	Proofread	Authorize
2010-8-12	A/0	Initial release	Li Yaqian	Zhou Lei	Hu Wenge

1. General Description

The BF3703 is a highly integrated VGA camera chip which includes CMOS image sensor (CIS) and image signal processing function (ISP). It is fabricated with the world's most advanced CMOS image sensor process to realize ultra-low dark noise, high sensitivity and very low power imaging system. The sensor consists of a 653 x 493 effective pixel array which has an optical format of 1/10 inch. It has integrated noise canceling CDS (Correlated Double Sampling) circuits, analog global gain and separated R/G/B gain controller, auto black level compensation and on-chip 10-bit ADC. The on-chip ISP provides a very smooth AE (Auto Exposure) and accurate AWB (Auto White Balance) control. It provides various data formats, such as Bayer RGB, RGB444, RGB555, RGB565, YCBCR 4:2:2. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

The product is capable of operating at up to 30 frames per second at 24MHZ clock in VGA mode, with complete user control over image quality and data formatting. All required image processing functions, including exposure control, white balance control, color saturation control and so on, are also programmable through the two-wire serial bus.

2. Features

- Standard optical format of 1/10 inch.
- 30 frame/sec VGA mode @ 24MHz master clock.
- Ultra-low dark noise at high temperature.
- Various output formats: YCBCR4:2:2, RGB444, RGB555, RGB565, Raw Bayer(652 x 492).
- Power supply: 2.7~3.1V for core, 1.7~3.1V for I/O.
- Horizontal /Vertical mirror.
- 50/60Hz flicker cancellation.
- Programmable I/O drive capability.
- Automatic black level control.
- Image processing function: Lens Shading Correction, Gamma Correction, Bad pixel correction, Color Interpolation, False Color Suppression, Purple Fringe Correction, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Auto exposure, Auto White Balance, Color Saturation and Contrast, and Data Format Conversion.
- 12 types of special video effect
- On-chip test pattern generation of many types including customer programmable
- Package: CSP, Bare Die

3. Applications

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Security systems
- Industrial and environmental systems

4. Technical Specifications

- Active pixel array: 653 x 493
- Pixel size: 2.25μm×2.25μm
- Sensitivity: 1V/lux.s
- Dark current: 3 mV/S at 40℃
- Power consumption: 56mW @ 30fps and single 2.8V supply
- Standby current: 30uA
- S/N Ratio: 35dB
- Dynamic range: 58dB
- Operating temperature: -20~60℃
- Stable Image temperature 0~50℃
- Optimal lens chief ray angle: 25º

5. Functional Overview

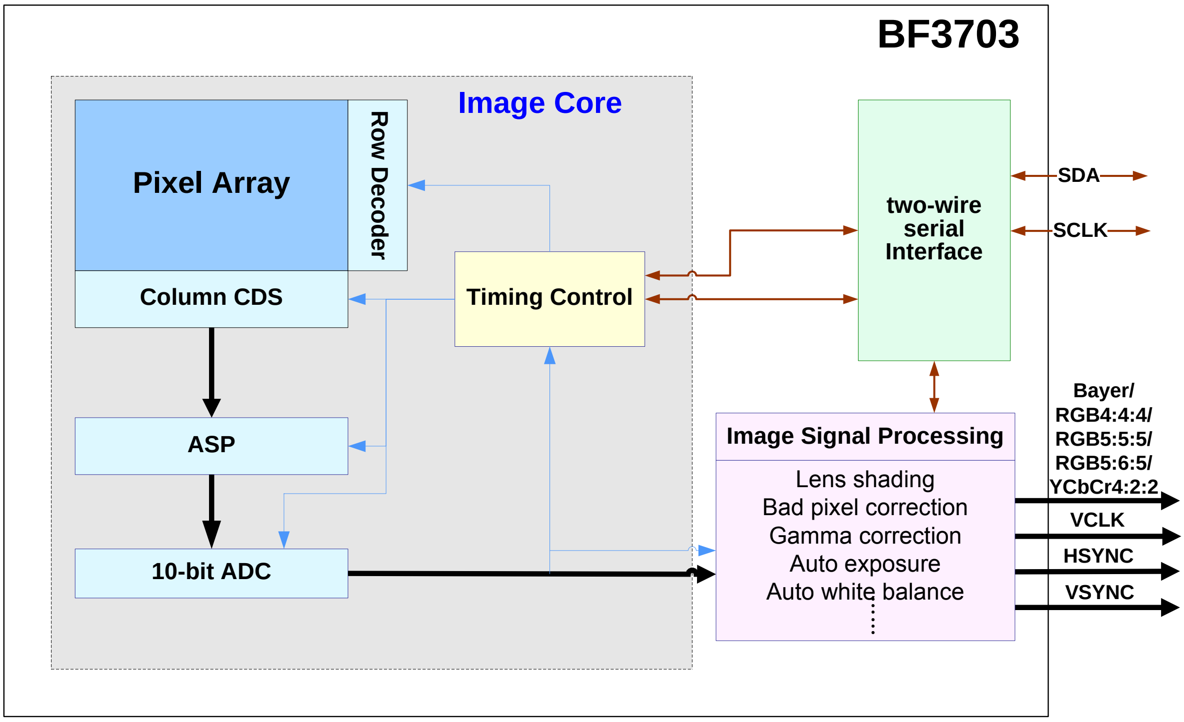

Figure 1. Block Diagram

BF3703 has an active image array of 653x493 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The ASP block is mainly used to control global gain and color gains to get accurate exposure and white balance under different light condition and color temperature. The analog signal is transferred to digital signal by A/D converter. The digital signals are processed in the ISP Block, including Bayer interpolation, low pass filter, color correction, gamma correction, data format conversion and so on. Users can easily control these functions via two-wire serial interface bus.

5.1 Pixel Array

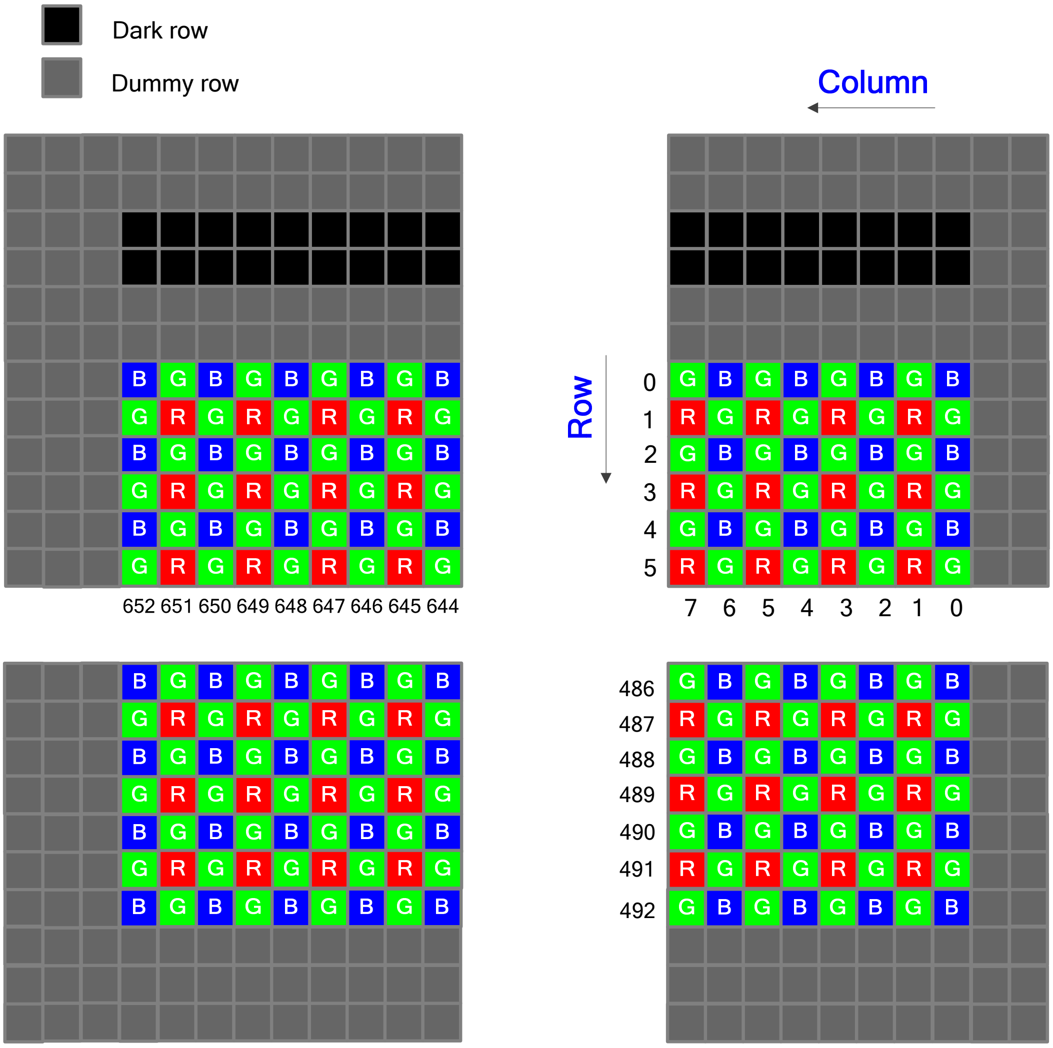

Figure 2. Sensor Array Region

The active pixel array is configured as 653 columns by 493 rows. Dummy pixels and dark rows are added outside the active pixel array.

Pixel array is covered by Bayer color filters as can be seen in the figure2. The primary color BG/GR array is arranged in line-alternating fashion. Since each pixel can have only one type of color filter on it, only one color component can be obtained by a pixel. BF3703 can provide the Raw Bayer data or YUV data through an 8-bit output data bus. If no flip in column, column is read out from 0 to 651. If flip in column, column is read out from 652 to 1. If no flip in row, row is read out from 0 to 491. If flip in row, row is read out from 492 to 1. In this way, the output pixel color order is always the same.

Pixel array output signal order is always:
BGBGBG……
GRGRGR…..

5.2 Column CDS

BF3703 has column/row driver circuits to read out the pixel data progressively. The CDS (Correlated Double Sampling) circuit reduces temporal noise and pixel level FPN (Fixed Pattern Noise). The unique patented column buffer amplifier and ASP (Analog Signal Processing) circuit remove column level FPN caused by various sources of manufacturing process variations.

5.3 Timing controller

The timing controller controls the following functions

- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing
- External timing outputs (VSYNC, HREF and VCLK)

5.4 Analog Signal Processor

This block performs all analog image functions including Color gain/Global gain control and black level compensation. Each of the R, G, B color pixel signals can be multiplied by different gain factors to balance the color of the image at various light conditions.

5.5 A/D converter

The analog signals are converted to digital forms column by column and row by row, through out the whole array. BF3703 provides the 10-bit Raw Bayer data for ISP through an internal 10-bit data bus.

5.6 Automatic Black Control

The automatic black level controller calculates the data of the dark row and controls the lowest black level for output image data.

5.7 Image Signal Processor

This block performs all image processing functions including Lens Shading Correction, Gamma Correction, Bad pixel correction, Color Interpolation, False Color Suppression, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Auto exposure, Auto White Balance, Color Saturation, Contrast, and Data Format Conversion.

6. Specifications

6.1 Electrical Characteristics

6.1.1. Absolute Maximum Ratings

- Supply voltage (VDDIO): 1.7 ~ 3.1 V
- Supply voltage (VDD3A): 2.7 ~ 3.1 V
- Operating temperature: -20~60 ℃
- Storage temperature: -30~80 ℃
- ESD Rating, Human Body mode: 2000 V

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

6.1.2. DC Parameters

Table 1. DC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
VDDIO	I/O power supply	V	1.7	2.8	3.1	
VDD3A	Analog power supply	V	2.7	2.8	3.1	--
I_vddio	VDDIO supply current, normal operation mode	mA	--	10.0	--	1
I_vdd3a	VDD3A supply current, normal operation mode	mA	--	10.0	--	2
Vih	Input voltage logic “1”	V	0.7*VDDIO	--	--	--
Vil	Input voltage logic “0”	V	--	--	0.2*VDDIO	--
Voh	Output voltage logic “1”	V	0.9*VDDIO	--	--	--
Vol	Output voltage logic “0”	V	--	--	0.1*VDDIO	--

Note：

1. Because power consumption of I/O depends on the output load and system environment, user

should supply enough current to sensor for stable operation. It is measured when output load is floated.

2. Because current of analog circuit depends on the registers' values, it is measured at specific register's value.

6.1.3. Clock Requirement

Table 2. AC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
MCLK	Main clock frequency	MHz	--	24	--	1
SCLk	two-wire serial interface clock frequency	KHz	--	400	--	2
Inormal	Current in YUV4:2:2 output mode	mA	--	20	--	3
Idown	Current in power down mode	uA	--	30	--	4

Note:

1. XCLK(external clock) may be divided by internal clock division logic to get MCLK for easy integration with high speed video codec system.
2. SCLK is driven by host processor. For the detail serial bus timing, refer to two-wire serial interface section
3. VDDIO=2.8V, VDD3A=2.8V(YUV4:2:2 output).
4. Hardware power down.

6.2 Electro-Optical Characteristics

Clock frequency: 24MHz.

Operating voltage: VDDIO=2.8V, VDD3A=2.8V.

Operating temperature: 25°C

Table 3. Electro-Optical Characteristics

Parameter	Unit	Min.	Typ.	Max.	Notes
Sensitivity	V/Lux·sec	--	1		1
Dark current	mV/sec	--	3	6	2
S/N ratio	dB	--	35dB	--	--
Dynamic Range	dB	--	58dB	--	--
Frame Rate	fps	--	--	30	3

Notes:

1. With color filter, measured at 50 lux green light condition at room temperature.
2. Measured at dark condition for exposure time of 1s (40 Celsius).
3. With 652×492 window size at MCLK 24MHz.

6.3 Input-Output AC Characteristics

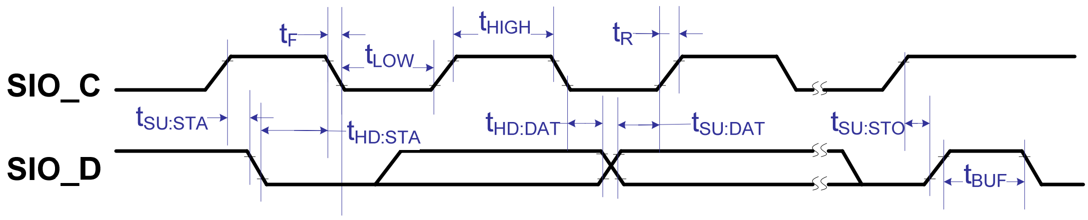

Figure 3. Two-Wire Serial Interface Timing

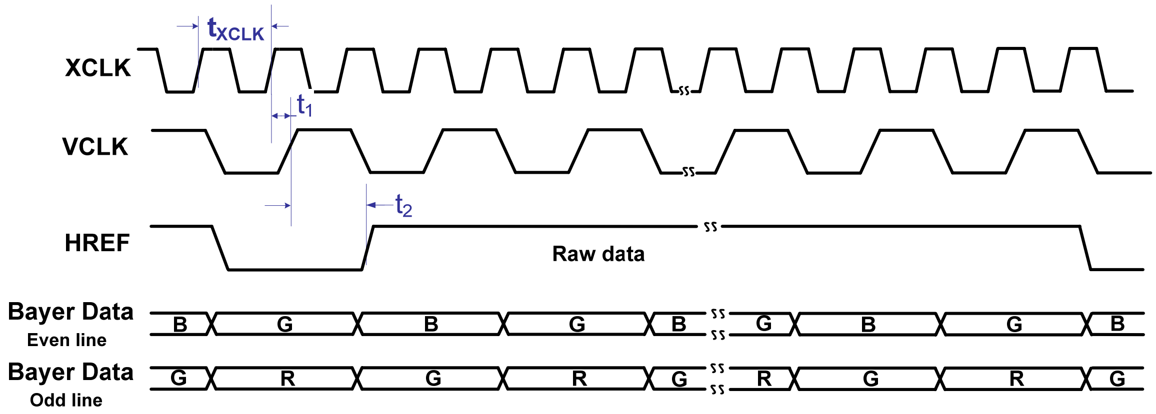

Figure 4. Horizontal Timing Raw Bayer Data

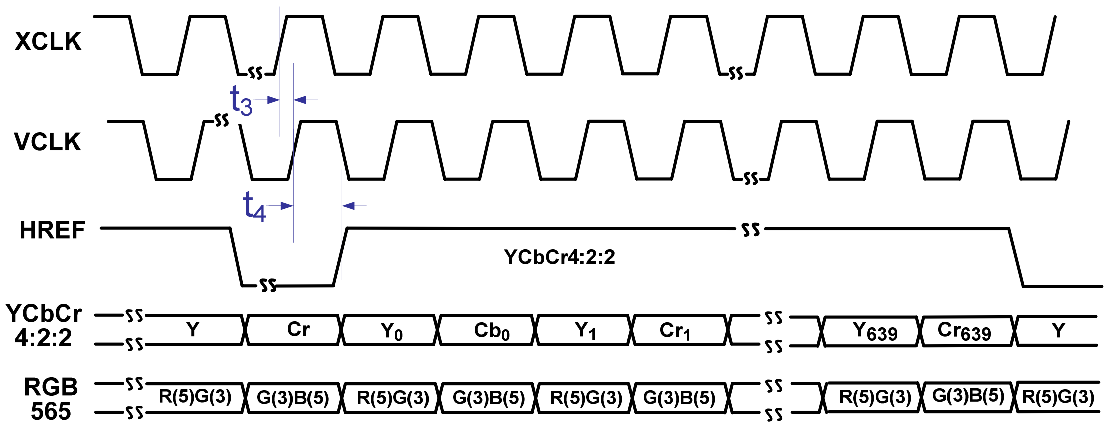

Figure 5. Horizontal Timing YUV4:2:2

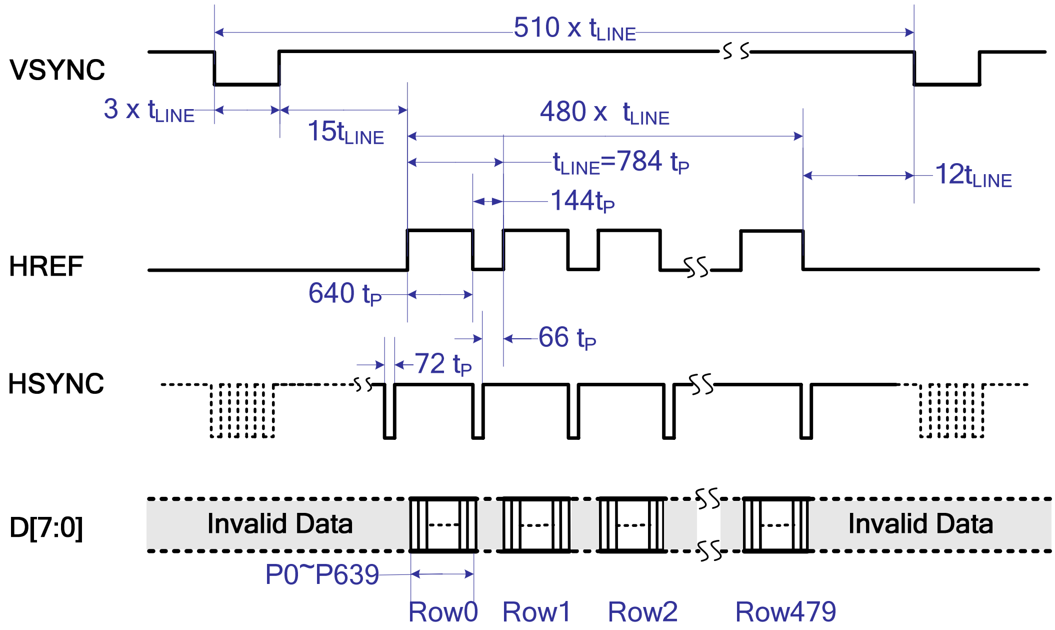

Figure 6. VGA Frame Timing

Table 4. AC Characteristics

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_P	t_P=2 x t_{MCLK}	--	83.2	--	ns
f_{MCLK}	Master Clock Frequency	--	24	--	MHz
f_{VCLK}	Video Clock Frequency for Raw data , f_V= f_{MCLK} /2 for YUV/RGB , f_V= f_{MCLK}	--	12/24	--	MHz
t_{LINE}	Line length	--	784x t_P	--	ns
t_R, t_F	two-wire serial interface rise/fall times	--	--	300	ns
t_{LOW}	Clock Low Period	1.3	--	--	us
t_{HIGH}	Clock High Period	600	--	--	ns
$t_{HD:STA}$	Start condition Hold Time	600	--	--	ns
$t_{SU:STA}$	Start condition Setup Time	600	--	--	ns
$t_{HD:DAT}$	Data-in Hold Time	0	--	--	ns
$t_{SU:DAT}$	Data-in Setup Time	100	--	--	ns
$t_{SU:STO}$	Stop condition Setup Time	600	--	--	ns
t1	XCLK rising to VCLK (RAW DATA)	--	28.8	--	ns
t2	VCLK rising to HREF (RAW DATA)	--	43.8	--	ns
t3	XCLK rising to VCLK (YUV)	--	19.2	--	ns
t4	VCLK rising to HREF (YUV)	--	21.6	--	ns

6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below.

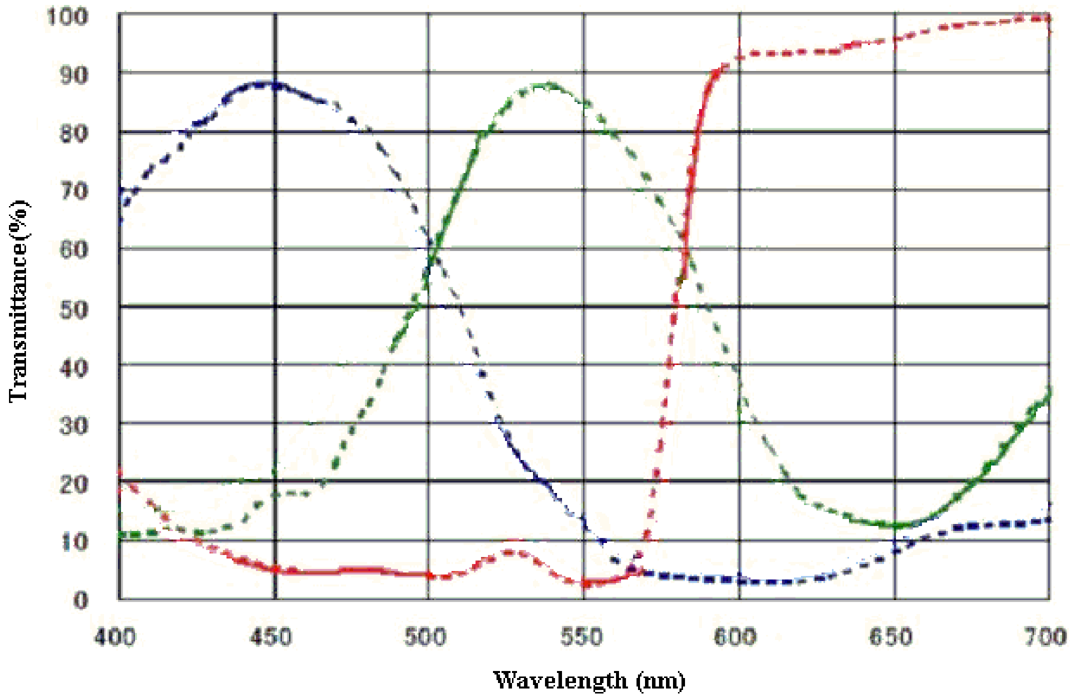

Figure 7. Spectral Characteristics

7. Two-wire serial interface& Register

7.1 Theory of Operation

The registers of BF3703 are written and read through the two-wire serial interface. BF3703 has two-wire serial interface slave. BF3703 is controlled by the two-wire serial interface clock (SCLK), which is driven by the two-wire serial interface master. Data is transferred into and out of BF3703 through the two-wire serial interface data (SDA) line. The SCL and SDA lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or the master device can pull the lines down. The two-wire serial interface protocol determines which device is allowed to pull the two lines down at any given time.

Note: Two-wire serial interface device address of BF3703 ***is 6eh.***

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A “0” in the LSB of the address indicates write mode, and “1” indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock: it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device’s 8-bit address. The last bit of the address determines if the request will be a read or a write, where “0” indicates write and “1” indicates read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The BF3703 uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

7.2 Two-wire Serial Interface Functional Description

Single Write Mode Operation

S	Slave address	W	A	Register address	A	Data	A	P

Multiple Write Mode (Register address is increased automatically) [1] **operation**

S	Slave address	W	A	Register address	A	Data	A	· · ·

· · ·	A	Data	A	Data	A	· · ·	A	Data	A	P

Single Read Mode Operation

S	Slave address	W	A	Register address	A	· · ·

Sr	Slave address	R	A	Data	NA	P

Multiple Read Mode (Register address is increased automatically) [1] **Operation**

S	Slave address	W	A	Register address	A	· · ·

Sr	Slave address	R	A	Data	A	Data	A	· · ·

· · ·	A	Data	A	Data	NA	P

From master to slave (shaded box) — From slave to master (white box)

S: Start condition. **Sr:** Repeated Start (Start without preceding stop.)

Slave Address: write address = DCh = 11011100b

read address = DDh = 11011101b

R/W: Read/Write selection. High = read, LOW = write.

A: Acknowledge bit. **NA:** No Acknowledge.

Data: 8-bit data **P:** Stop condition

Note1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

7.3 Register Summary (full list)

Table 5. BF3703 all registers

Address	Name	Width	Default value	Description
00h	***DBLKHE***	6	20h	Reserved.
01h	***BLUE_GAIN***	6	19h	Blue gain register.
02h	***RED_GAIN***	6	15h	Red gain register.
03h	***VHREF***	8	00h	VREF and HREF control. Bit[7:6]: VREF end low 2 Bits(high 8 Bit at ***VSTOP[7:0]***) Bit[5:4]: VREF start low 2 Bits(high 8 Bit at ***VSTART[7:0]***) Bit[3:2]: HREF end 2 LSB(high 8 MSB at register ***HSTOP***) Bit[1:0]: HREF start 2 LSB(high 8 MSB at register ***HSTART***)
05h	***LOFFN1E***	6	1eh	Coarse negative offset control-even column.
06h	***LOFFN0***	8	e0h	Bit[7]: Two wire serial interface switch. Bit[6]: Reserved. Bit[5:0]: Fine negative offset control col.
08h	***TAREG3***	8	00h	Reserved.
09h	***COM2***	8	10h	Common control 2. When ***0x20[6]***=0, Bit[1:0]: Data & clk & hsync output drive capability. 00: 1x, 01: 2x, 10: 3x, 11: 4x. When ***0x20[6]***=1, Bit[7:6]: Vclk output drive capability. 00: 1x, 01: 2x, 10: 3x, 11: 4x. Bit[5]: Spare. Bit[4]: Standby mode. 0: Disable standby mode. 1: Enable standby mode. Bit[3:2]: Hsyc output drive capability. 00: 1x, 01: 2x, 10: 3x, 11: 4x. Bit[1:0]: Data output drive capability. 00: 1x, 01: 2x, 10: 3x, 11: 4x.
0ah	***COM5***	8	21h	Common control 5. Bit[7:4]: Total column number1 for gate subsample. Bit[3:0]: Column select number1 for gate subsample.
0bh	***COM4***	8	00h	Common control 4. Bit[7]: 0: Select even row, 1: Select odd row. Bit[6]: 0: Select even column, 1: Select odd column. Bit[5:4]: 0x:Output normal HSYNC/VSYNC. 10: HSYNC=0,VSYNC=0. 11: HSYNC=1,VSYNC=1. Bit[3:0]: Skip frame counter.

0ch	***COM3***	8	00h	Common control 3. Bit[7]: PROCRSS RAW selection, 0: Process raw from YCBCR to RGB conversion in data format, 1: Process raw from color interpolation(deniose, gamma, lsc is selectable), Bit[6]:Output data MSB and LSB swap, Bit[5:4]: PROCESS RAW sequence(when ***0x0c[7]***=0), 00: (LINE0:BGBG/LINE1:GRGR), 01: (LINE0:GBGB/LINE1:RGRG), 10: (LINE0:GRGR/LINE1:BGBG), 11: (LINE0:RGRG/LINE1:GBGB). Bit[3]: 0:no HREF when VSYNC_DAT=0, 1:Always has HREF no matter VSYNC_DAT=0 or not, Bit[2]: DATA ahead 1 clk(YUV MCLK, RawData PCLK) or not, Bit[1]: HREF ahead 1 clk(YUV MCLK, RawData PCLK) or not, Bit[0]: HREF ahead 0.5 clk(YUV MCLK, RawData PCLK) or not, 0x0c[1:0]: 00:HREF and data is synchronous, 01:HREF before data 0.5 clk, 10:HREF before data 1 clk, 11:HREF before data 1.5 clk.
0dh	***DBLKLE***	6	20h	Reserved.
0eh	***DBLKHO***	6	20h	Reserved.
0fh	***DBLKLO***	6	20h	Reserved.
10h	***COM6***	8	21h	Common control 6. Bit[7:4]: Total row number1 for gate subsample. Bit[3:0]: Row select number1 for gate subsample.
11h	***CLKRC***	8	80h	Mclk division control. Bit[7]: Double Clock Option. 0:Disable double clock option, Meaning the maximum MCLK can be as high as half input clock. 1:Enable double clock option, Meaning the maximum MCLK can be as high as input clock. Bit[6]: Use external clock directly(F(internal clock)==F(input clock)). Bit[5:4]: Mclk divider factor 00: Divided by 1, 01: Divided by 2, 10: Digital power down, 11: Divided by4. Bit[3:2]: Pclk control. 0: Normal, 1: Inverse and dly 1.5ns, 2: Inverse and dly 3ns, 3: Inverse and dly 5.5ns. Bit[1]: Spare. Bit[0]: Doubler clock selection. 0: Mclk, 1: Mclk/2.

12h	***COM7***	8	00h	Common control 7. Bit[7]: SCCB Register Reset. 0: No change, 1: Resets all registers to default values. Bit[6]: Reserved. Bit[5]: Row subsample Selection. 0: Enable, 1: Disable. Bit[4]: 1/2 digital subsample Selection(only for YUV422/RGB565/RGB555/RGB444 output). Bit[3]: Reserved. Bit[2]: YUV422/RGB565/RGB555/RGB444 Selection. Bit[1]: Reserved. Bit[0]: Raw RGB Selection. {***0x12[2],0x12[0]***} 00: YUV422, 01: Bayer RAW, 10: RGB565/RGB555/RGB444(use with 0x3a), 11: Process RAW(use with 0x0c[7]).
13h	***COM8***	8	07h	Common control 8. Bit[7:4]: Reserved. Bit[3]: Select when to use small steps to adjust the integration time. 0: When ***INT_TIM*** lower than 10ms, 1: When ***INT_TIM*** lower than 20ms. Bit[2]: AGC Enable. 0:OFF , 1: ON. Bit[1]: AWB Enable. 0:OFF , 1: ON. Bit[0]: AEC Enable. 0:OFF , 1: ON.
14h	***LOFFN1O***	6	1eh	Coarse negative offset control-odd col.
15h	***COM10***	8	02h	Common control 10. Bit[7]: Reserved. Bit[6]: 0:HREF, 1:HSYNC. Bit[5]: 0:VSYNC_IMAGE, 1:VSYNC_DAT. Bit[4]: VCLK reverse Bit[3]: HREF option. 0: Active high, 1: Active low. Bit[2]: Reserved Bit[1]: VSYNC option. 0: Active low, 1: Active high. Bit[0]: HSYNC option. 0: Active high, 1: Active low.
16h	***BIAS2***	8	09h	Reserved.
17h	***HSTART***	8	00h	Output Format-Horizontal Frame(HREF column)start high 8-Bit(low 2Bits are at ***VHREF[1:0]***)
18h	***HSTOP***	8	a0h	Output Format-Horizontal Frame(HREF column)end high 8-Bit(low 2 Bits are at ***VHREF[3:2]***)
19h	***VSTART***	8	00h	Output Format-Vertical Frame(row)start high 8-Bit(low 2 Bits are at ***VHREF[5:4]***)
1ah	***VSTOP***	8	78h	Output Format-Vertical Frame(row)end high 8-Bit(low 2 Bits are at ***VHREF[7:6]***)
1bh	***PLLCTL***	8	80h	PLL control. Bit[7]: PLL pdn Enable. 0: Enable, 1: Disable. Bit[6:4]: Spare. Bit[3:2]: Loop divide, default11 (Divided by 3). 00: Divided by 4, 01: Divided by 1, 10: Divided by 2, 11: Divided by 3. Bit[1:0]: Output divide, default 11 (Divided by 24). 00: Divided by 1, 01: Divided by 6, 10: Divided by 12, 11: Divided by 24.
1ch	***MIDH***	8	7fh,RO	Reserved.
1dh	***MIDL***	8	a2h,RO	Reserved.

1eh	***MVFP***	8	00h	Mirror/Vflip Enable. Bit[7:6]:Reserved Bit[5]: Mirror. 0: Normal image, 1: Mirror image. Bit[4]: Vflip enable. 0: Normal image, 1: Vertically flip. Bit[3:0]: Reserved
1fh	***DBLK_TARG***	8	20h	Black control target for G. Bit[7:0]: Black control target for G. Bit[6:0]: Reserved.
20h	***TDREG***	8	00h	Bit[7]: Reserved. Bit[6]: Hsync&clk pad drive capability control. 0: Same drive capability, 1: Drive capability adjustment independently. (refer to register ***COM2***) Bit[5:0]: Reserved.
21h	***Reserved.***			
22h	***DBLK_TARR***	8	20h	Black control target for R. Bit[7:0]:Black control target for R. Bit[6:0]: Reserved.
23h	***GLGAINREG***	7	33h	GreenGain[2:0]: Bit[6:4]: For even column (used as ***GreenEgain[2:0]***). Bit[2:0]: For odd column (used as ***GreenOgain[2:0])***.
24h	***AE_LOCK1***	8	8Ah	Y target value 1.
25h	***AE_LOCK2***	8	7Ah	Y target value 2.
26h	***DBLK_TARB***	8	20h	Black control target for B, Bit[6:0]:Black control target for B.
27h	***STEP***	8	04h	Bit[7:6]: Coarse adjustment range, 00: 4, 01: 8, 10: 12, 11: 16. Bit[5:0]: Step.
28h	***DBLK_CNTL***	8	00h	Reserved.
29h	***BIAS1***	8	04h	BIAS control 1. Bit[7]: Black control fine adjustment resolution control for even column. Bit[6]: Black control coarse adjustment resolution control for even column. Bit[5]: Black control fine adjustment resolution control for odd column. Bit[4]: Black control coarse adjustment resolution control for odd column. Bit[3]: Spare. Bit[2:0] ADC bias setting. 0d: Lower bias, 15d: Higher bias.
2ah	***EXHCH***	8	00h	Dummy Pixel Insert MSB. Bit[7:4]: Dummy Pixel Insert MSB. Bit[3:0]: Reserved.
2bh	***EXHCL***	8	00h	Dummy Pixel Insert LSB. Bit[7:0]: Dummy Pixel Insert LSB.
2dh	***INT_TIMH***	8	06h	Integration time MSB.
2eh	***INT_TIML***	8	66h	Integration time LSB.
2fh	***DREF***	8	e2h	Reserved.
30h	***HSYST***	8	64h	Control the rising edged of HSYNC, HSYNC rising edge low 8 Bits.
31h	***HSYEN***	8	14h	Control the falling edged of HSYNC, HSYNC falling edge low 8 Bits.
32h	***LS_MODE***	8	1fh	Bit[7:5]: Reserved, Bit[4]: Light sensor control. 0: Disable, 1: Enable. Bit[3:0]: Reserved.
33h	***OFFSET_MODE***	8	00h	Lens shading offset selection: Bit[7]: 0: Use black average value(from Black Control function) as offset 1: Use register ***OFFSET_REG*** as offset Bit[6:0]: Reserved.
34h	***OFFSET_REG***	8	38h	Lens shading offset.
35h	***R_COEF***	8	46h	Lens shading gain of R.

36h	***Y0H_G,Y0H_B, X0H_G,X0H_B***	6	05h	Bit[5]: Y0H_G. Center row coordinate HSB of G channel. Bit[4]: Y0H_B. Center row coordinate HSB of B channel. Bit[3:2]: X0H_G. Center col coordinate HSB of G channel. Bit[1:0]: X0H_B. Center col coordinate HSB of B channel.
37h	***Y0L_B***	8	f6h	Reserved.
38h	***X0L_B***	8	46h	Reserved.
39h	***OFFSET2***	8	80h	Gamma Offset 2: Bit[7]: 0: Positive , 1: Negative Bit[6:0]: Value.
3ah	***TSLB***	8	00h	Data output sequence. If YUV422 is selected. The Sequence is: Bit[1:0]:Output YUV422 Sequence 00: YUYV, 01: YVYU 10: UYVY, 11: VYUY If RGB565/RGB555/RGB444 is selected. The Sequence is: Bit[4:0]:Output RGB565/RGB555/RGB444 Sequence RGB565: 00h: R5G3H,G3LB5， 01h: B5G3H,G3LR5. 02h: B5R3H,R2LG6， 03h: R5B3H,B2LG6. 04h: G3HB5,R5G3L， 05h: G3LB5,R5G3H. 06h: G3HR5,B5G3L， 07h: G3LR5,B5G3H. 08h: G6B2H,B3LR5， 09h: G6R2H,R3LB5. RGB555: 0Ah: 1'b0R5G2H,G3LB5, 0Bh: G3LB5,1'b0R5G2H. 0Ch: R5G3H,G2LB51'b0, 0Dh: G2LB51'b0, R5G3H. 0Eh: B5G3H,G2L1'b0,R5, 0Fh: R5G3H,G2L1'b0,B5. 10h: B51'b0G2H,G3LR5, 11h: R51'b0G2H,G3LB5. RGB444: 12h: 4'b0R4,G4B4, 13h: G4B4,4'b0R4. 14h: 4'b0B4,G4R4, 15h: G4R4,4'b0B4. 16h: R4G4,B44'b0, 17h: B44'b0,R4G4. 18h: B4G4,R44'b0, 19h: R44'b0,B4G4. 1Ah: B4G4,R4B4, 1Bh: R4G4,B4R4. 1Ch: R4G2H2'b0,G2LB42'b0, 1Dh: B4G2H2'b0,G2LR42'b0. 1Eh: B41'b0G3H,G1L2'b0R41'b0, 1Fh: R41'b0G3H,G1L2'b0B41'b0.
3bh	***Y_AVER_TH***	7	60h	Reserved.
3ch	***OFFSET_TH2***	7	24h	Reserved.
3dh	***COM11***	8	59h	Common control 11. Bit[7:4]: Total row number2 for gate sub. Bit[3:0]: Total column number2 for gate sub.
3eh	***TAREG2***	8	03h	Bit[7]:Tri-state option for output clock, HSYNC,VSYNC at power-down period. 0: Tri-state at this period, 1: No Tri-state at this period. Bit[6]: Tri-state option for output data OEN at power-down period. 0: Tri-state at this period, 1: No Tri-state at this period. Bit[5:0]: Reserved.
3fh	***OFFSET1***	8	9ah	Gamma Offset 1. Bit[7]: 0: Use black average value(from Black Control function) as offset. 1: Use register ***OFFSET1[6:0]*** as offset. Bit[6:0]:OFFSET1 value.
40h	***k0***	8	50h	Gamma Correction Slop Coefficient 0.
41h	***k1***	8	50h	Gamma Correction Slop Coefficient 1.
42h	***k2***	8	58h	Gamma Correction Slop Coefficient 2.
43h	***k3***	8	55h	Gamma Correction Slop Coefficient 3.
44h	***k4***	8	50h	Gamma Correction Slop Coefficient 4.
45h	***k5***	8	49h	Gamma Correction Slop Coefficient 5.
46h	***k6***	8	44h	Gamma Correction Slop Coefficient 6.

47h	***k7***	8	3eh	Gamma Correction Slop Coefficient 7.
48h	***k8***	8	38h	Gamma Correction Slop Coefficient 8.
49h	***k9***	8	34h	Gamma Correction Slop Coefficient 9.
4ah	***SUBSAMPLE***	7	60h	Bit[6:4]:Reserved Bit[3]:Window enable. 1: Window function enable, 0: Normal output(default). Bit[2]: Subsample mode. 1: Realize subsample, 0: No subsample. Bit[2:0]: 0xx: NO subsample(normal), 100:4/5sub, 101:3/5sub, 110:2/3sub, 111:1/2sub.
4bh	***k10***	8	30h	Gamma Correction Slop Coefficient 10.
4ch	***k11***	8	2dh	Gamma Correction Slop Coefficient 11.
4eh	***k12***	8	28h	Gamma Correction Slop Coefficient 12.
4fh	***k13***	8	23h	Gamma Correction Slop Coefficient 13.
50h	***k14***	8	20h	Gamma Correction Slop Coefficient 14.
51h	***TARGET1***	8	01h	Color Correction Coefficient 1.
52h	***TARGET2***	8	0dh	Color Correction Coefficient 2.
53h	***TARGET3***	8	0eh	Color Correction Coefficient 3.
54h	***TARGET4***	8	0ah	Color Correction Coefficient 4.
55h	***BRIGHT***	8	00h	Brightness control. Bit[7]: 0: Positive, 1: Negative. Bit[6:0] : Value.
56h	***Y_COEF***	8	40h	Y Coefficient for Contrast.
57h	***TARGET5***	8	42h	Color Correction Coefficient 5.
58h	***TARGET6***	8	4ch	Color Correction Coefficient 6.
59h	***TARGET7***	8	55h	Color Correction Coefficient 7.
5ah	***TARGET8***	8	76h	Color Correction Coefficient 8.
5bh	***TARGET9***	8	21h	Color Correction Coefficient 9.
5ch	***TARGET***	8	0eh	Bit[7]: Color Correction adjustment enable, 1: Disable, 0: Enable. Bit[6:5]: Reserved. Bit[4]: Sign of Color Correction Coefficients 9. Bit[3:0]: Reserved.
5dh	***TARGET_SIGN***	8	9ch	Bit[7]: Sign of Color Correction Coefficients 8. Bit[6]: Sign of Color Correction Coefficients 7. Bit[5]: Sign of Color Correction Coefficients 6. Bit[4]: Sign of Color Correction Coefficients 5. Bit[3]: Sign of Color Correction Coefficients 4. Bit[2]: Sign of Color Correction Coefficients 3. Bit[1]: Sign of Color Correction Coefficients 2. Bit[0]: Sign of Color Correction Coefficients 1.
5fh	***DARK_AVERE***	8	20h,RO	DARKROW_AVER FOR EVEN COLUMN
60h	***GLB_GAIN_TH***	8	20h	Reserved.
61h	***Ma_Th_Ctr***	8	e3h	Reserved.
64h	***DARK_AVER0***	8	20h,RO	Dark row average value for odd column.
65h	***G_COEF***	8	46h	Lens shading gain of G.
66h	***B_COEF***	8	46h	Lens shading gain of B.
67h	***MANU***	8	80h	Manual U value.
68h	***MANV***	8	80h	Manual V value.

69h	***DICOM1***	8	00h	Dither control 1. Bit[7]: YCBCR RANGE select. 0: YCBCR 0~255, 1: Y 16~235, CBCR 16~240. Bit[6]: Negative image enable 0: Normal image, 1: Negative image Bit[5]: UV output value select. 0: Output normal value, 1: Output fixed value set in MANU and MANV. Bit[4]: U、V dither when YCBCR mode/R、B dither when RGB mode: 0: Low 2 Bits, 1: Low 3Bits. Bit[3]: Y dither when YCBCR mode/G dither when RGB mode: 0: Low 2 Bits, 1: Low 3Bits. Bit[2]:Y dither enable. Bit[1] :U、V dither enable. Bit[0]: RGB dither enable.
6ah	***GNGAINREG***	8	81h	Bit[7:3]: Reserved. Bit[2:0]: G channel Gain (Bit2~Bit0 is used as GreenGain[5:3]).
6bh	***COM9***	8	02h	Common control 9. Bit[7]: 0:Use column_gate_sub for CKGATE, 1: Use HREF for CKGATE,default=0. Bit[6]: Reserved. Bit[5:4]: Average weight select, default value=00. Bit[3]: 0:Nomal, 1:CKGATE ahead 1 MCLK(YUV) or PCLK(rawdata). Bit[2]: 0:NomaL, 1:CKGATE ahead 0.5 MCLK(YUV) or PCLK(rawdata). Bit[1]: 0:No CKGATE when HREF=0, 1: Always has CKGATE. Bit[0]: 0:No gate sub, 1: Gate sub enable.
6ch	***CLKDIV***	8	10h	Reserved.
6fh	***DICOM2***	8	20h	Reserved.
70h	***IntCtr***	8	6fh	Interpolation control. Bit[7:4]: Reserved. Bit[3]:Edge enhancement switch. 0: Off, 1: On. Bit[2]: Processed rawdata output format switch. (use with 0x0c[7]=1) 0: 648x488, 1:652x492, Bit[1]: Reserved Bit[0]: Low pass filter switch. 0: Off, 1:On.
71h	***BpcCtr***	8	a6h	Reserved.
72h	***DenCtr***	8	4fh	Reserved.
73h	***EdgCtr***	8	2fh	Reserved.
74h	***DaECtr***	8	27h	Reserved.
75h	***DakCtr***	8	0eh	Reserved.
76h	***EffCtr***	8	00h	Bit[7]: Special effect output on/off 0: Off, 1: On. Bit[6:4]: Special effect choice 011: Sketch, 100: Cuprum relievo, 101: Blue relievo, 110: Black relievo, 111: White relievo, default: Normal relievo. Bit[3]: Sram on/off 0: On, 1: Off. Bit[2:0]: Reserved.

77h	***SobCtr***	7	10h	Bit[7]: Reserved Bit[6]: Select the mode for G balance. 0: Less smoothing. 1: More smoothing, Bit[4]: Edge thin enable.. 1: On, 0: Off. Bit[3:0]: Reserved.
78h	***SobMax***	8	ddh	{Bit[7],Bit[3]}: The speed of denoise according to Gain difference 11: 1, 10:1/2, 01: 1/4, 00:0. Bit[6:4]: Reserved
79h	***MacCtr***	8	c8h	Reserved.
7ah	***BlaCtr***	8	86h	Bit[7:4]: Y_AVER threshold. Bit[3]: Denoise enable in the condition of low light. 0: Denoise mode 1. 1: Denoise mode 2. Bit[2:0]: Reserved.
7bh	***GaiCtr***	7	2ch	Bit[6:0]: When ***GLB_GAIN =GLB_GAIN_MAX***, enable the denose function in the condition of low light.
80h	***AE_MODE***	8	45h	AE control mode. Bit[7]: AE mode selection. 0: Use Y (from color space module). 1: Use rawdata (from gamma module), when special effect in color interpolation module is selected, 0x80[7] must set to be 1. Bit[6]: INT_TIM lower than INT_STEP_50(INT_STEP_60) or not. 0: Limit int_tim>=step(no flicker), 1: Int_tim can be less than 1*integration step(existing flicker). Bit[5:4]: Center window select. 00: ROW*12/16, COL*12/16, 01: ROW*10/16, COL*10/16, 10: ROW* 8/16, COL*8/16, 11: ROW* 6/16, COL*6/16. Bit[3:1]: Weight select. 000: 4/8*center+4/8*border, 001: 5/8*center+3/8*border, 010: 6/8*center+2/8*border, 011: 7/8*center+1/8*border, 1xx: Center 100%. Bit[0]: Banding filter value select. 0: Select {0x89[5],0x9E[7:0]} as Banding Filter Value. 1: Select {0x89[4],0x9D[7:0]} as Banding Filter Value.
81h	***AE_SPEED***	8	02h	Frame count value for AE speed
82h	***GLB_GAIN_MIN***	7	0Ah	Global Gain Minimum
83h	***GLB_GAIN_MEANL***	7	1Ah	Reserved.
84h	***GLB_GAIN_MEANM***	7	1Bh	Reserved.
85h	***GLB_GAIN_MEANH***	7	26h	Reserved.
86h	***GLB_GAIN_MAX***	7	2ch	Global Gain Maximum
87h	***GLB_GAIN***	7	16h	Global gain register, (the max value is limited to 0x3f)
88h	***Y_AVER***	8	80h,RO	The average of the current frame
89h	***INT_MEAN_H***	7	02h	Bit[6]: Use as INT_MIN Bit[8],INT_MIN={0X89[6],0X8b[7:0]}, Bit[5]: Use as 60HZ Banding Filter STEP's Bit[8], Bit[4]: Use as 50HZ Banding Filter STEP's Bit[8], Bit[3:0]: Reserved.
8ah	***INT_MEAN_L***	8	fdh	Reserved.
8bh	***INT_TIM_MIN***	8	06h	Min integration time[7:0], INT_MIN={0X89[6],0X8b[7:0]}, effective only when *0x80[6]*=1
8ch	***INT_TIM[15:8]***	8	01h	Integration time MSB.
8dh	***INT_TIM[7:0]***	8	cbh	Integration time LSB.

8eh	***INT_TIM_MAX_H***	8	0bh	Integration time upper limit MSB.
8fh	***INT_TIM_MAX_L***	8	f5h	Integration time upper limit LSB.
90h	***INT_TIM_TH***	7	20h	Reserved.
91h	***OFFSET_TH1***	7	1ch	Reserved.
92h	***DM_LNL***	8	05h	Dummy line insert after active line low 8 Bits.
93h	***DM_LNH***	8	00h	Dummy line insert after active line high 8 Bits.
94h	***INT_OPEN***	6	10h	Integration time open value.
95h	***INTSTEPSD_SEL***	8	94h	Bit[7]: IF ***INT_TIM*** < ***INT_STEP*** , it will limit the speed when AE is stable. 0: Normal, 1: Limit the speed.. Bit[6:0]: Threshold for AE speed. The value smaller, the AE speed faster. NOTE: Too small value may cause AE instability.
96h	***GLB_STEPS_SEL***	8	9Ah	Bit[7] : Reserved Bit[6:0]: Global gain threshold for AE speed.
97h	***INT_TIM_COEF_TH***	8	08h	Integration time threshold for AE speed.
98h	***Y_AVER_TH***	5	10h	Y frame average threshold for AE speed, The value larger, AE speed faster. Note: Too large value may cause AE instability.
9ah	***GLB_GAIN_MEANL_STEPSD***	7	1ah	Reserved.
9bh	***Y0L_G***	8	f6h	Reserved.
9ch	***X0L_G***	8	46h	Reserved.
9dh	***INT_STEP_50***	8	99h	50HZ Banding Filter STEP low 8 Bits, Bit[8] is in 0x89[4] (***INT_MEAN_H[4]***).
9eh	***INT_STEP_60***	8	7fh	60HZ Banding Filter STEP low 8 Bits, Bit[8] is in 0x89[5] (***INT_MEAN_H[5]***).
a0h	***UPDATE_MODE***	8	07h	Bit[7:2]: Reserved. Bit[1]: YCBCR limit enable, Bit[0]: For manual write RGAIN/BGAIN mode, 0: RGAIN/BGAIN can't be written if AWB_EN***(COM8[1])***=0 not strides over vsync's negedge, 1: RGAIN/BGAIN can be written no matter AWB_EN=0 strides over vsync's negedge or not.
a1h	***AWB_LOCK*** ***AWB_SPEED***	8	31h	Bit[7:4]:Auto White Balance Lock Boundary, Bit[3:0]:AWB Update Speed.
a2h	***BLUE_GAIN_LOW_IN***	6	0ah	The low limit value of blue gain.
a3h	***BLUE_GAIN_HIGH_IN***	6	20h	The high limit value of blue gain.
a4h	***RED_GAIN_LOW_IN***	6	0ch	The low limit value of red gain.
a5h	***RED_GAIN_HIGH_IN***	6	26h	The high limit value of red gain.
a6h	***COUNT_EN***	8	04h	AWB criterion: white pixels count threshold, '1' equal to 1024 pixels.
a7h	***CB_TARGET***	8	80h	CB frame average target value.
a8h	***CR_TARGET***	8	80h	CR frame average target value.
a9h	***CB_LIMIT***	8	1eh	AWB criterion: CB.
aah	***CR_LIMIT***	8	19h	AWB criterion: CR.
abh	***CBCR_LIMIT***	8	1eh	AWB criterion: CBCR.
ach	***Y_LOW***	8	3ch	AWB criterion: Y_LOW.
adh	***Y_HIGH***	8	f0h	AWB criterion: Y_HIGH.
aeh	***OUTDOOR_EN*** ***INT_TIM_EN***	8	00h	Reserved.
afh	***BGAIN_LOW_OUT***	6	00h	Reserved.
b0h	***SAT_CTR1***	8	c0h	Saturation control: Bit[7]: Saturation mode. 0: Normal 1: Auto. Bit[6:0] Reserved.

b1h	***CB_COEF***	8	c6h	CB Coefficient for Color Saturation.
b2h	***CR_COEF***	8	cch	CR Coefficient for Color Saturation.
b3h	***SAT_CTR2***	8	8ch	Reserved.
b6h	***MAN_R***	8	80h	Define R value.
b7h	***MAN_G***	8	80h	Define G value.
b8h	***MAN_B***	8	80h	Define B value.
b9h	***TEST_MODE***	8	00h	Bit[7]: 0: Test pattern bypass, 1: Test pattern enable. Bit[6:5]: 00: Output color bar pattern. 01: Output gradual pattern. 10: Output manual write R/G/B. 11: Auto mode, speed is controlled by ***TEST_MODE [4:0].*** Bit[4] : 0: Vertical pattern, 1: Horizontal pattern Bit[3:0]: Gradual gray pattern mode control
bbh	***BLANK***	8	00h	Reserved.
bch	***Y0H_R,X0H_R***	5	01h	Reserved.
bdh	***Y0L_R***	8	F6h	Reserved.
beh	***X0L_R***	8	46h	Reserved.
c5h	***BGAIN_HIGH_OUT***	6	16h	Reserved.
c6h	***RGAIN_LOW_OUT***	6	00h	Reserved.
c7h	***RGAIN_HIGH_OUT***	6	1fh	Reserved.
c8h	***BGAIN_OUTTH***	6	17h	Reserved.
c9h	***RGAIN_OUTTH***	6	19h	Reserved.
cah	***BGAIN_INTH***	6	15h	Reserved.
cbh	***RGAIN_INTH***	6	17h	Reserved.
cch	***INT_TIM_TH***	8	4dh	Reserved.
cdh	***YCBCR_LIMIT***	8	b4h	Reserved.
d9h	***H_START_H***	8	00h	When *SUBSAMPLE[3]*==1'b1, in window mode, window X start[9:2].
dah	***H_END_H***	8	a3h	When *SUBSAMPLE[3]*==1'b1, in window mode, window X end[9:2].
dbh	***V_START_H***	7	00h	When *SUBSAMPLE[3]*==1'b1, in window mode, window Y start[8:2].
dch	***V_END_H***	7	7bh	When *SUBSAMPLE[3]*==1'b1, in window mode, window Y end[8:2].
ddh	***VH_ADD_L***	8	00h	In window mode. Bit[1:0]: window X start[1:0]. Bit[3:2]: window X end[1:0]. Bit[5:4]: window Y start[1:0]. Bit[7:6]: window Y end[1:0].
e0h	***PRSTF***	6	06h	Reserved.
e1h	***TX2_R***	7	38h	Reserved.
e2h	***HREF_CNTL***	8	04h	Reserved.
e3h	***DM_ROWL***	8	09h	Dummy line insert before active line low 8 Bits.
e4h	***DM_ROWH***	8	00h	Dummy line insert before active line high 8 Bits.
e5h	***SHRF***	6	14h	Reserved.
e6h	***SHSF***	6	32h	Reserved.
e7h	***MXSTART_R***	8	74h	Reserved
e8h	***H_HSYNC_EDGE***	8	00h	Bit[7:4]: Control the rising edge of HSYNC. HSYNC rising edge high 4 Bits; Bit[3:0]: Control the falling edge of HSYNC. HSYNC falling edge high 4 Bits .
e9h	***ISP_CK***	8	72h	Reserved.
eah	***ANALOG_PDN***	8	50h	Reserved.
ebh	***ISP_CK_CNTL***	8	20h	Reserved.
eeh	***P_TH***	8	4ch	Reserved.
efh	***SKIN_CTR***	4	bh	Reserved.

f1h	***BYPASS0***	8	00h	Bit[7]: Data format enable, 0: Enable, 1: Disable. Bit[6]: Contrast enable, 0: Enable, 1: Disable. Bit[5]: Saturation enable , 0: Enable, 1: Disable. Bit[4]: Color space & Color correction enable, 0: Enable, 1: Disable. Bit[3]: Color Correction enable, 0: Enable, 1: Disable. Bit[2]: Color Interpolation enable, 0: Enable, 1: Disable. Bit[1]: Gamma Correction enable, 0: Enable, 1: Disable. Bit[0]: Lens Correction enable, 0: Enable, 1: Disable.
f2h	***HUE_COS***	8	7fh	Hue cosine coefficient range -1~0.99(*0X80~0X7F*) MSB is symbol
f3h	***HUE_SIN***	8	00h	Hue sine coefficient range -1~0.99(*0X80~0X7F*) MSB is symbol.
f4h	***ISP_CK_NUM***	8	09h	Reserved
f5h	***READEN_R***	5	20h	Reserved
f8h	***Y_LS0***	8	00h,RO	Reserved
f9h	***LS_REG,Y_LS1***	8	00h	Reserved
fch	***PID_BME***	8	37h,RO	Product ID MSB.
fdh	***VER_BME***	8	03h,RO	Product ID LSB.

8. Package Specifications

Mechanical Diagram

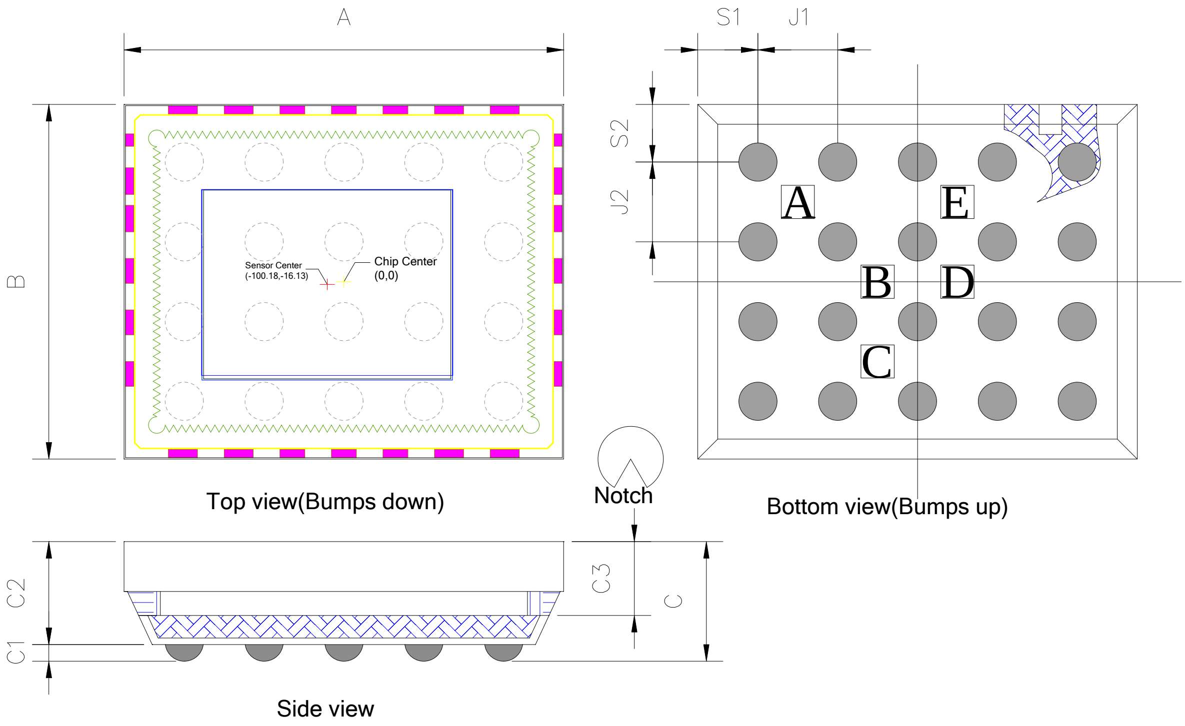

Figure 7 CSP dimension description

Table 6 CSP Dimensions

	Symbol	Nominal	Min	Max
		Unit（μm）		
Package Body Dimension X	A	2643	2618	2668
Package Body Dimension Y	B	2134	2109	2159
Package Height	C	720	660	780
Ball Height	C1	100	70	130
Package Body Thickness	C2	620	575	665
Thickness from top glass surface to wafer	C3	445	425	465
Ball Diameter	D	230	200	260
Total Ball Count	N	20		
Ball Count X axis	N1	5		
Ball Count Y axis	N2	4		
Pins Pitch X axis	J1	480		
Pins Pitch Y axis	J2	480		
Edge to Pin Center Distance along X	S1	362	332	392
Edge to Pin Center Distance along Y	S2	347	317	377

Table 7 Ball Matrix Table

	1	2	3	4	5
A	VDD3A	D6	D5	D3	VCLK
B	VSSA	D7	D4	D2	VSSD
C	SCL	HREF	RESET	D1	PWDN
D	SDA	VSYNC	XCLK	D0	VDDIO

Table 8 Pin Descriptions

Pin Number	Name	Pin Type	Function/Description
A1	VDD3A	Power	Analog power supply.
A2	D6	Output	YUV/RGB image data output port [6].
A3	D5	Output	YUV/RGB image data output port [5].
A4	D3	Output	YUV/RGB image data output port [3].
A5	VCLK	Output	Pixel clock output.
B1	VSSA	Power	Analog ground.
B2	D7	Output	YUV/RGB image data output port [7].
B3	D4	Output	YUV/RGB image data output port [4].
B4	D2	Output	YUV/RGB image data output port [2].
B5	VSSD	Power	Digital ground.
C1	SCLK	Input	SCCB serial interface clock input.
C2	HREF	Output	HREF output.
C3	RSTB	Input(1)*	Reset all registers to their default values. 0: Reset mode 1: Normal mode

C4	D1	Output	YUV/RGB image data output port [1].
C5	PDN	Input(0)**	Power Down Mode Selection. 0: Normal mode. 1: Power down mode.
D1	SDA	I/O	SCCB serial interface data I/O.
D2	VSYNC	Output	Vertical sync output.
D3	XCLK	Input	System clock input.
D4	D0	Input	YUV/RGB image data output port [0].
D5	VDDIO	Power	Power supply for I/O.

Note:
** Input(1) represents an internal pull-up resistor.
** Input(0) represents an internal pull-down resistor.

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