iNAND 7232

e.MMC 5.1 with Command-Queue and HS400 Interface
**REVISION HISTORY**

<table>
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<tr>
<th>Doc. No</th>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
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<td>DOC-06397</td>
<td>1.00</td>
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<td>Change max preloading image size</td>
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<td>Fixed RMS numbers</td>
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<td>Fixed Part Number typo</td>
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<td>Added 16GB capacity</td>
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<td>Update preloading max image size</td>
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<tr>
<td>DOC-06397</td>
<td>1.12</td>
<td>18-Oct-2015</td>
<td>Added new SKU (SDINADF4-XXXG-H)</td>
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<td>Typo fixes</td>
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<td>DOC-06397</td>
<td>1.13</td>
<td>25-Oct-2015</td>
<td>Updated introduction section</td>
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<td></td>
<td></td>
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<td>Fixed SmartSLC number</td>
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1. INTRODUCTION

1.1. General Description

Overview SanDisk iNAND 7232 is an Embedded Flash Drive (EFD) for boosting the overall performance of existing flash-based product lines like smartphones, tablets and automotive infotainment systems as well as enabling manufacturers to bring the benefits of flash (rapid boot-up, high reliability, robustness, consistent performance) to new markets such as entry-level notebooks.

Providing up to 128GB of capacity and technology for features such as low-power consumption, the iNAND 7232 is the ideal choice to deliver amazing performance for storage-hungry applications like imaging, video, music, GPS, gaming, email, office and other applications on 4G smartphones, embedded systems or other devices.

The design of the iNAND 7232 is based on JEDEC compatible form factors to lower integration costs and accelerate time-to-market.

Architecture iNAND 7232 combines an embedded thin flash controller with advanced Triple-Level Cell (TLC) NAND flash technology enhanced by SanDisk’s embedded flash management software running as firmware on the flash controller. iNAND 7232 employs an industry-standard e.MMC 5.1 interface featuring Command-Queue, HS400 interface, FFU, as well as legacy e.MMC 4.51 features such as Power Off Notifications, Packed commands, Cache, Boot / RPMB partitions, HPI, and HW Reset, make it an optimal device for both reliable code and data storage.

Like our other iNAND products, iNAND 7232 offers plug-and-play integration and support for multiple NAND technology transitions, as well as features such as an advanced power management scheme.

iNAND 7232 architecture and embedded firmware fully emulates a hard disk to the host processor, enabling read/write operations that are identical to a standard, sector-based hard drive. In addition, SanDisk firmware employs patented methods, such as virtual mapping, dynamic and static wear-leveling, and automatic block management to ensure high data reliability and maximizing flash life expectancy.

iNAND 7232 also includes an intelligent controller, which manages interface protocols, data storage and retrieval, error correction code (ECC) algorithms, defect handling and diagnostics, power management and clock control.

Combining high performance with features for easy integration and exceptional reliability, iNAND 7232 is an EFD designed to exceed the demands of both manufacturers and their customers.

1.2. Plug-and-Play Integration

iNAND’s optimized architecture eliminates the need for complicated software integration and testing processes thereby enabling plug-and-play integration into the host system. The

1 Compatible to JESD84-B50
replacement of one iNAND device with another of a newer generation requires virtually no changes to the host. This allows manufacturers to adopt advanced NAND Flash technologies and update product lines with minimal integration or qualification efforts.

With JEDEC form factors measuring 11.5x13mm (153 balls) for all capacities, iNAND 7232 is ideally suited for a wide variety of portable devices such as multimedia mobile handsets, tablets, and automotive infotainment.

iNAND 7232 features a MMC interface allows for easy integration regardless of the host (chipset) type used. All device and interface configuration data (such as maximum frequency and device identification) are stored on the device.

Figure 1 shows a block diagram of the SanDisk iNAND 7232 with MMC Interface.

1.3. Feature Overview
SanDisk iNAND 7232, with MMC interface, includes the following features:

- Memory controller and NAND flash
- Mechanical design complies with JEDEC Specification
- Offered in three TFBGA packages of e.MMC 5.12
  - 11.5mm x 13mm x 0.9mm (16GB-32GB)
  - 11.5mm x 13mm x 1.0mm (64GB)
  - 11.5mm x 13mm x 1.2mm (128GB)
- Operating temperature range: –25°C to +85°C
- Dual power system
- Core voltage (VCC) 2.7-3.6 V
- I/O (VCCQ) voltage, either: 1.7-1.95V or 2.7-3.6V

2 Refer to JEDEC Standards No. JESD84-B50
• Note: Device operation under 3.3V VCCQ is limited to Max 1 hour
• Up to 128GB of data storage
• Supports three data bus widths: 1bit (default), 4bit, 8bit
• Complies with e.MMC Specification Ver. 5.1 HS400
• Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed), 0-200 MHz SDR (HS200), 0-200 MHz DDR (HS400)
• Up to 400 MB/sec bus transfer rate, using 8 parallel data lines at 200 MHz, HS400 Mode
• Correction of memory field errors
• Designed for portable and stationary applications that require high performance and reliable data storage

1.4. Defect and Error Management
The SanDisk iNAND 7232 contains a sophisticated defect and error management system for exceptional data reliability. iNAND 7232 will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume additional user data space. In the extremely rare case that a read error does occur, iNAND has innovative algorithms to recover the data.

1.5. MMC bus and Power Lines
SanDisk iNAND 7232 with MMC interface supports the MMC protocol. For more details regarding these buses refer to JEDEC standards No. JESD84-B51.

The iNAND bus has the following communication and power lines:
• CMD: Command is a bidirectional signal. The host and iNAND operate in two modes, open drain and push-pull.
• DAT0-7: Data lines are bidirectional signals. Host and iNAND operate in push-pull mode.
• CLK: Clock input.
• RST_n: Hardware Reset Input.
• VCCQ: VCCQ is the power supply line for host interface.
• VCC: VCC is the power supply line for internal flash memory.
• VDDi: VDDi is iNAND’s internal power node, not the power supply. Connect 0.1uF capacitor from VDDi to ground.
• VSS, VSSQ: Ground lines.
• RCLK: Data strobe.
• VSF: Vendor specific functions used for debugging purposes.
1.5.1. **Bus operating conditions**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak voltage on all lines</td>
<td>-0.5</td>
<td>VCCQ+0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Leakage Current (before initializing and/or connecting the internal pull-up resistors)</td>
<td>-100</td>
<td>100</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)</td>
<td>-2</td>
<td>2</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Output Leakage Current (before initializing and/or connecting the internal pull-up resistors)</td>
<td>-100</td>
<td>100</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)</td>
<td>-2</td>
<td>2</td>
<td>µA</td>
<td></td>
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</tbody>
</table>

**Table 2 – Power supply voltage**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>VCCQ (Low)</td>
<td>1.7</td>
<td>1.95</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VCCQ (High)</td>
<td>2.7</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VCC</td>
<td>2.7</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VSS-VSSQ</td>
<td>-0.3</td>
<td>0.3</td>
<td>V</td>
</tr>
</tbody>
</table>

*Note1: HS400 mode only supports the 1.7 – 1.95 V VCCQ option*

*Note2: Device operation under 3.3V VCCQ is limited to Max 1 hour*
## 2. e.MMC 5.1 Selected Features Overview

### iNAND 7232 supported feature list:

<table>
<thead>
<tr>
<th>e.MMC</th>
<th>Device Features</th>
<th>Benefit</th>
<th>Support</th>
</tr>
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<tbody>
<tr>
<td>N/A</td>
<td>INTERFACE</td>
<td>Speed</td>
<td>HS400</td>
</tr>
<tr>
<td>N/A</td>
<td>BUS SPEED</td>
<td>Max theoretical Speed</td>
<td>Up to 400MB/s</td>
</tr>
<tr>
<td>4.41</td>
<td>SECURE ERASE/TRIM</td>
<td>&quot;True Wipe&quot;</td>
<td>Yes</td>
</tr>
<tr>
<td>4.41</td>
<td>BOOT AND MASS STORAGE</td>
<td>One storage device (reduced BOM)</td>
<td>Yes</td>
</tr>
<tr>
<td>4.41</td>
<td>PARTITIONING &amp; PROTECTION</td>
<td>Flexibility</td>
<td>Yes</td>
</tr>
<tr>
<td>4.41</td>
<td>BACKGROUND OPERATIONS</td>
<td>Better User Experience (low latency)</td>
<td>Yes</td>
</tr>
<tr>
<td>4.41</td>
<td>POWER OFF NOTIFICATION</td>
<td>Faster Boot; Responsiveness</td>
<td>Yes</td>
</tr>
<tr>
<td>4.41</td>
<td>HARDWARE RESET</td>
<td>Robust System Design</td>
<td>Yes</td>
</tr>
<tr>
<td>4.41</td>
<td>HPI</td>
<td>Control Long Reads/Writes</td>
<td>Yes</td>
</tr>
<tr>
<td>4.41</td>
<td>HPI</td>
<td>Secure Folders</td>
<td>Yes</td>
</tr>
<tr>
<td>4.5</td>
<td>EXTENDED PARTITION ATTRIBUTE</td>
<td>Flexibility</td>
<td>Yes</td>
</tr>
<tr>
<td>4.5</td>
<td>LARGE SECTOR SIZE</td>
<td>Potential performance</td>
<td>No</td>
</tr>
<tr>
<td>4.5</td>
<td>SANITIZE (4.51)</td>
<td>&quot;True Wipe&quot;</td>
<td>Yes</td>
</tr>
<tr>
<td>4.5</td>
<td>PACKED COMMANDS</td>
<td>Reduce Host Overhead</td>
<td>Yes</td>
</tr>
<tr>
<td>4.5</td>
<td>DISCARD</td>
<td>Improved Performance on Full Media</td>
<td>Yes</td>
</tr>
<tr>
<td>4.5</td>
<td>DATA TAG</td>
<td>Performance and/or Reliability</td>
<td>Yes (API only)</td>
</tr>
<tr>
<td>4.5</td>
<td>CONTEXT MANAGEMENT</td>
<td>Performance and/or Reliability</td>
<td>Yes (API only)</td>
</tr>
<tr>
<td>4.5</td>
<td>CACHE</td>
<td>Better Sequential &amp; Random Writes</td>
<td>Yes</td>
</tr>
<tr>
<td>5.0</td>
<td>FIELD FIRMWARE UPGRADE (FFU)</td>
<td>Enables feature enhancements in the field</td>
<td>Yes</td>
</tr>
<tr>
<td>5.0</td>
<td>PRODUCTION STATE AWARENESS</td>
<td>Different operation during production</td>
<td>Yes</td>
</tr>
<tr>
<td>5.0</td>
<td>DEVICE HEALTH</td>
<td>Vital NAND info</td>
<td>Yes</td>
</tr>
<tr>
<td>5.1</td>
<td>ENHANCE STROBE</td>
<td>Sync between Device and Host in HS400</td>
<td>Yes</td>
</tr>
<tr>
<td>5.1</td>
<td>COMMAND QUEUE</td>
<td>responsiveness</td>
<td>Yes</td>
</tr>
<tr>
<td>5.1</td>
<td>RPMB THROUGHPUT</td>
<td>Faster RPMB write throughput</td>
<td>Yes</td>
</tr>
<tr>
<td>5.1</td>
<td>CACHE FLUSH AND BARRIER</td>
<td>Ordered Cache flushing</td>
<td>Yes</td>
</tr>
<tr>
<td>5.1</td>
<td>BKOPS CONTROLLER</td>
<td>Host control on BKOPs</td>
<td>* No – for SKU SDINADF4-xxxG &amp; S DINADF4-xxxG-L &amp; SDINADF4-xxxG-H</td>
</tr>
<tr>
<td>5.1</td>
<td>SECURE WP</td>
<td>Secure Write Protect</td>
<td>* No – for SKU SDINADF4-xxxG &amp; S DINADF4-xxxG-L &amp; S DINADF4-xxxG-H</td>
</tr>
<tr>
<td>Propriety</td>
<td>SMART-SLC</td>
<td>Fast write speed per application need</td>
<td>Yes</td>
</tr>
<tr>
<td>Propriety</td>
<td>VSF</td>
<td>Enable on-board debugging</td>
<td>Yes</td>
</tr>
<tr>
<td>Propriety</td>
<td>PNM</td>
<td>Special product name</td>
<td>Yes</td>
</tr>
<tr>
<td>Propriety</td>
<td>DEVICE REPORT</td>
<td>Device Firmware status</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### 2.1. HS400 Interface

Support HS400 signaling to achieve a bus speed of 400 MB/s via a 200MHz dual data rate clock frequency. HS400 mode supports 4 or 8 bit bus width and the 1.7 – 1.95 VCCQ option. Due to the speed, the host may need to have an adjustable sampling point to reliably receive the incoming data. For additional information please refer to JESD84-B51 standard.
2.2. Field Firmware Upgrade (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism, the host downloads a new version of the firmware to the e.MMC device and instructs the e.MMC device to install the new downloaded firmware into the device. The entire FFU process occurs in the background without affecting the user / OS data. During the FFU process, the host can replace firmware files or single / all file systems.

The secure FFU (sFFU) usage model for firmware upgrades is as follows:

1. sFFU files are generated and signed at the SanDisk lab
2. The sFFU files are handed to SanDisk’s customer
3. SanDisk’s customer can push the firmware updates to their end-users in a transparent way

   Note 1: The sFFU process and sFFU files are protected against leakage to unauthorized entities.

   Note 2: During the sFFU process the Host may retrieve the exact status of the process using the smart report feature.

For additional information please refer to JESD84-B51 standard and the SanDisk application note on this subject.

2.3. Cache

The eMMC cache is dedicated volatile memory at the size of 512KB. Caching enables to improve iNAND performance for both sequential and random access. For additional information please refer to JESD84-B51 standard.

2.4. Discard

iNAND supports discard command as defined in e.MMC 5.1 spec\(^3\). This command allows the host to identify data which is not needed, without requiring the device to remove the data from the Media. It is highly recommended for use to guarantee optimal performance of iNAND and reduce amount of housekeeping operation.

2.5. Power off Notifications

iNAND supports power off notifications as defined in e.MMC 5.1 spec\(^4\). The usage of power off notifications allows the device to prepare itself to power off, and improve user experience during power-on. Note that the device may be set into sleep mode while power off notification is enabled.

Power off notification long allows the device to shutdown properly and save important data for fast boot time on the next power cycle.

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\(^3\) For additional information refer to JEDEC Standard No. JESD84-B50

\(^4\) For additional information refer to JEDEC Standard No. JESD84-B50
2.6. Packed Commands
To enable optimal system performance, iNAND supports packed commands as defined in e.MMC 5.1 spec. It allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus. Thus, it allows reducing overall bus overheads.

2.7. Boot Partition
iNAND supports e.MMC 5.1 boot operation mode: Factory configuration supplies two boot partitions each 4MB in size for 8GB-64GB

2.8. RPMB Partition
iNAND supports e.MMC 5.1 RPMB operation mode: Factory configuration supplies one RPMB partition 4MB in size for 8GB-64GB

2.9. Automatic Sleep Mode
A unique feature of iNAND is automatic entrance and exit from sleep mode. Upon completion of an operation, iNAND enters sleep mode to conserve power if no further commands are received. The host does not have to take any action for this to occur, however, in order to achieve the lowest sleep current, the host needs to shut down its clock to the memory device. In most systems, embedded devices are in sleep mode except when accessed by the host, thus conserving power. When the host is ready to access a memory device in sleep mode, any command issued to it will cause it to exit sleep and respond immediately.

2.10. Sleep (CMD5)
An iNAND 7232 device may be switched between a Sleep and a Standby state using the SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized and the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device.

The VCC power supply may be switched off in Sleep state to enable even further system power consumption saving.

For additional information please refer to JESD84-B51.

2.11. Enhanced Reliable Write
iNAND 7232 supports enhanced reliable write as defined in e.MMC 5.1 spec.

Enhanced reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write

---

5 For additional information refer to JEDEC Standard No. JESD84-B50
6 For additional information refer to JEDEC Standards No. JESD84-B50
transaction never contains undefined data. When writing in reliable write, data will remain valid even if a sudden power loss occurs during programming.

2.12. Sanitize

The Sanitize operation is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. The device will continue the sanitize operation, with busy asserted, until one of the following events occurs:

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure
- Hardware reset

After the sanitize operation is complete no data should exist in the unmapped host address space.

2.13. Secure Erase

For backward compatibility reasons, in addition to the standard erase command the iNAND 7232 supports the optional Secure Erase command\(^7\).

This command allows the host to erase the provided range of LBAs and ensure no older copies of this data exist in the flash.

2.14. Secure Trim

For backward compatibility reasons, iNAND 7232 support Secure Trim command. The Secure Trim\(^8\) command is similar to the Secure Erase command but performs a secure purge operation on write blocks instead of erase groups.

The secure trim command is performed in two steps:

1) Mark the LBA range as candidate for erase.
2) Erase the marked address range and ensure no old copies are left.

2.15. Partition Management

iNAND 7232 offers the possibility for the host to configure additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore memory block area scan be classified as follows

- Factory configuration supplies two boot partitions (refer to section 2.8) implemented as enhanced storage media and one RPMB partitioning of 4MB in size (refer to section 2.9).

- Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of

\(^7\) For additional information refer to JEDEC Standards No. JESD84-B50

\(^8\) For additional information refer to JEDEC Standards No. JESD84-B50
the write protect group. Size can be programmed once in device life-cycle (one-time programmable).

2.16. Device Health
Device Health is similar to SMART features of modern hard disks, it provides only vital NAND flash program/erase cycles information in percentage of useful flash life span.
The host can query Device Health information utilizing standard MMC command, to get the extended CSD structure:
DEVICE_LIFE_TIME_EST_TYP_A[268], The host may use it to query SLC device health information
DEVICE_LIFE_TIME_EST_TYP_B[269], The host may use it to query TLC device health information
The device health feature will provide a % of the wear of the device in 10% fragments.

2.17. EOL Status
EOL status is implemented according to the eMMC 5.1 spec. One additional state (state 4) was added to INAND 7232 which indicates that the device is in EOL mode.

2.18. Enhanced Write Protection
To allow the host to protect data against erase or write INAND 7232 supports two levels of write protect command
- The entire INAND 7232 (including the Boot Area Partitions, General Purpose Area Partition, and User Area Partition) may be write-protected by setting the permanent or temporary write protect bits in the CSD
- Specific segments of INAND 7232 may be permanently, power-on or temporarily write protected. Segment size can be programmed via the EXT_CSD register
For additional information please refer to the JESD84-B51 standard.

2.19. High Priority Interrupt (HPI)
The operating system usually uses demand-paging to launch a process requested by the user. If the host needs to fetch pages while in a middle of a write operation the request will be delayed until the completion of the write command.
The high priority interrupt (HPI) as defined in JESD84-B51 enables low read latency operation by suspending a lower priority operation before it is actually completed.
For additional information on the HPI function, refer to JESD84-B51.
2.20. H/W Reset
Hardware reset may be used by host to reset the device, moving the device to a Pre-idle state and disabling the power-on period write protect on blocks that were power-on write protected before the reset was asserted. For more information, refer to JESD84-B51 standard.

2.21. Host-Device Synchronization Flow (Enhanced STROBE)
The Enhanced STROBE feature as implemented in iNAND 7232 allows utilizing STROBE to synchronize also the CMD response:

- CMD clocking stays SDR (similar to legacy DDR52)
- Host commands are clocked out with the rising edge of the host clock (as done in legacy eMMC devices)
- iNAND 7232 will provide STROBE signaling synced with the CMD response in addition to DATA Out
- Host may use the STROBE signaling for DAT and CMD-Response capturing eliminating the need for a tuning mechanism

This feature requires support by the host to enable faster and more reliable operation.

2.22. Command-Queue
e.MMC Command Queue enables device visibility of next commands and allows performance improvement. The protocol allows the host to queue up to 32 data-transfer commands in the device by implementing 5 new commands.

The benefits of command queuing are:

- Random Read performance improvement (higher IOPs)
- Reducing protocol overhead
- Command issuance allowed while data transfer is on-going
- Device order the tasks according to best access to/from flash
3. PRODUCT SPECIFICATIONS

3.1. Typical Power Requirements

Table 3 – iNAND 7232 Power Consumption Sleep (Ta=25°C@3.3/1.8V)

<table>
<thead>
<tr>
<th></th>
<th>16GB</th>
<th>32GB</th>
<th>64GB</th>
<th>128GB</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>HS400 Sleep</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>uA</td>
</tr>
<tr>
<td>HS200 Sleep</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>uA</td>
</tr>
<tr>
<td>DDR52 Sleep</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>uA</td>
</tr>
</tbody>
</table>

Table 4 - iNAND 7232, Power Consumption Peak (Max) VCC / VCCQ (Ta=25°C@3.3V/1.8V)

<table>
<thead>
<tr>
<th></th>
<th>16GB</th>
<th>32GB</th>
<th>64GB</th>
<th>128GB</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active HS400</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak [2µs window] VCC</td>
<td>250</td>
<td>300</td>
<td>450</td>
<td>450</td>
<td>mA</td>
</tr>
<tr>
<td>Max [1ms window] VCCQ</td>
<td>320</td>
<td>340</td>
<td>450</td>
<td>450</td>
<td>mA</td>
</tr>
<tr>
<td>Active HS200</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak [2µs window] VCC</td>
<td>250</td>
<td>300</td>
<td>450</td>
<td>450</td>
<td>mA</td>
</tr>
<tr>
<td>Max [1ms window] VCCQ</td>
<td>320</td>
<td>340</td>
<td>450</td>
<td>450</td>
<td>mA</td>
</tr>
<tr>
<td>Active DDR52</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak [2µs window] VCC</td>
<td>250</td>
<td>300</td>
<td>450</td>
<td>450</td>
<td>mA</td>
</tr>
<tr>
<td>Max [1ms window] VCCQ</td>
<td>310</td>
<td>350</td>
<td>400</td>
<td>400</td>
<td>mA</td>
</tr>
</tbody>
</table>

Table 5 - iNAND 7232, Power Consumption RMS VCC / VCCQ (Ta=25°C@3.3V/1.8V)

<table>
<thead>
<tr>
<th></th>
<th>16GB</th>
<th>32GB</th>
<th>64GB</th>
<th>128GB</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read HS400</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RMS [100ms window] VCC</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>mA</td>
</tr>
<tr>
<td>RMS [100ms window] VCCQ</td>
<td>250</td>
<td>275</td>
<td>275</td>
<td>300</td>
<td>mA</td>
</tr>
<tr>
<td>Write HS400</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RMS [100ms window] VCC</td>
<td>125</td>
<td>150</td>
<td>200</td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>RMS [100ms window] VCCQ</td>
<td>175</td>
<td>175</td>
<td>175</td>
<td>175</td>
<td>mA</td>
</tr>
<tr>
<td>Read HS200</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RMS [100ms window] VCC</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>RMS [100ms window] VCCQ</td>
<td>175</td>
<td>175</td>
<td>200</td>
<td>250</td>
<td>mA</td>
</tr>
<tr>
<td>Write HS200</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RMS [100ms window] VCC</td>
<td>50</td>
<td>90</td>
<td>160</td>
<td>160</td>
<td>mA</td>
</tr>
<tr>
<td>RMS [100ms window] VCCQ</td>
<td>125</td>
<td>150</td>
<td>200</td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>Read DDR52</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RMS [100ms window] VCC</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>RMS [100ms window] VCCQ</td>
<td>135</td>
<td>135</td>
<td>160</td>
<td>160</td>
<td>mA</td>
</tr>
<tr>
<td>Write DDR52</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RMS [100ms window] VCC</td>
<td>50</td>
<td>90</td>
<td>160</td>
<td>160</td>
<td>mA</td>
</tr>
<tr>
<td>RMS [100ms window] VCCQ</td>
<td>115</td>
<td>140</td>
<td>160</td>
<td>160</td>
<td>mA</td>
</tr>
</tbody>
</table>
3.2. Operating Conditions

3.2.1. Operating and Storage Temperature Specifications

Table 6 - Operating and Storage Temperatures

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Minimum and Maximum Operating*</th>
<th>Minimum and Maximum Non-Operating: After soldered onto PCBA</th>
</tr>
</thead>
<tbody>
<tr>
<td>-25°C to 85°C</td>
<td>-40°C to 85°C</td>
<td></td>
</tr>
</tbody>
</table>

* Per eMMC5.1 specification (JESD84-BS1): To achieve optimized power/performance, maximum Tcase temperature should not exceed 85°C.

3.2.2. Moisture Sensitivity

The moisture sensitivity level for iNAND 7232 is MSL = 3.

3.3. Reliability

SanDisk iNAND 7232 product meets or exceeds NAND type of products Endurance and Data Retention requirements as per evaluated representative usage models for designed market and relevant sections of JESD47I standard.

Table 8 - Critical Reliability Characteristics

<table>
<thead>
<tr>
<th>Reliability Characteristics</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uncorrectable Bit Error Rate (UBER)</td>
<td>Uncorrectable bit error rate will not exceed one sector in the specified number of bits read. In such rare events data can be lost.</td>
<td>1 sector in $10^{15}$ bits read</td>
</tr>
</tbody>
</table>
| Write Endurance Specification (TBW) | Write endurance is commonly classified in Total Terabytes Written (TBW) to a device. This is the total amount of data that can be written to the device over its useful life time and depends on workload. Representative workload description:  
  - 74% Sequential write , 16% Random Write, 10% big Sequential Write  
  - Distribution of IO Transaction Sizes: 30% : 4KB, 27% : 16KB, 42% : Mix of 8KB, 32KB-256KB, 1% : 512KB  
  - Cache On, Packed Off  
  - Host data is 4K aligned | Total Terabytes Written [TBW] Per representative Android workload:  
  16GB: 11 [TB]  
  32GB: 22 [TB]  
  64GB: 44 [TB]  
  128GB: 88 [TB] |
| Data Retention Specification (Years) | Fresh or Early Life Device  
(A device whose total write cycles to the flash is less than 10% of the maximum endurance specification) | 10 years of Data Retention @ 55°C |
| Cycled Device | Active Use (power on)  
(Any device whose total write cycles are between 10% of the maximum write endurance specification and equal to or exceed the maximum write endurance specification) | 1 year of Data Retention @ 55°C  
Note: In the case where the number of writes exceed the endurance spec read and Write performance can be intermediately reduced. |
| Retention Use (power off) | 1 year of Data Retention @ 40°C or 3 months  
Data Retention @55°C  
Note: In the case where the number of write exceed the endurance spec data loss or functional failure is expected. |
3.4. System Performance

All performance values for iNAND 7232 in Table were measured under the following conditions:

- Voltage range:
  - Core voltage (VCC): 2.7-3.6 V
  - Host voltage (VCCQ), either: 1.7-1.95 V or 2.7-3.6V
  - Note: Device operation under 3.3V VCCQ is limited to Max 1 hour

- Operating temperature: -25° C to 85° C

Table 9 – Sequential Performance for SKUs SDINADF4-xxG and SDINADF4-xxG-L

<table>
<thead>
<tr>
<th></th>
<th>HS400</th>
<th>HS200</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Write (MBs)</td>
<td>Read (MBs)</td>
</tr>
<tr>
<td>16GB</td>
<td>95</td>
<td>270</td>
</tr>
<tr>
<td>32GB</td>
<td>150</td>
<td>290</td>
</tr>
<tr>
<td>64GB</td>
<td>150</td>
<td>290</td>
</tr>
<tr>
<td>128GB</td>
<td>150</td>
<td>290</td>
</tr>
</tbody>
</table>

Table 10 – Sequential Performance for SKUs SDINADF4-xxG-H

<table>
<thead>
<tr>
<th></th>
<th>HS400</th>
<th>HS200</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Write (MBs)</td>
<td>Read (MBs)</td>
</tr>
<tr>
<td>16GB</td>
<td>130</td>
<td>270</td>
</tr>
<tr>
<td>32GB</td>
<td>160</td>
<td>290</td>
</tr>
<tr>
<td>64GB</td>
<td>160</td>
<td>290</td>
</tr>
<tr>
<td>128GB</td>
<td>160</td>
<td>290</td>
</tr>
</tbody>
</table>

Table 11 – Random Performance for SKUs SDINADF4-xxG and SDINADF4-xxG-L

<table>
<thead>
<tr>
<th></th>
<th>HS400</th>
<th>HS200</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Write (IOPs)</td>
<td>Read (IOPs)</td>
</tr>
<tr>
<td></td>
<td>Cache ON</td>
<td>Cache OFF</td>
</tr>
<tr>
<td>16GB</td>
<td>3300</td>
<td>1400</td>
</tr>
<tr>
<td>32GB</td>
<td>4000</td>
<td>1800</td>
</tr>
<tr>
<td>64GB</td>
<td>4000</td>
<td>1800</td>
</tr>
<tr>
<td>128GB</td>
<td>4000</td>
<td>1800</td>
</tr>
</tbody>
</table>

Table 12 – Random Performance for SKUs SDINADF4-xxG-H

<table>
<thead>
<tr>
<th></th>
<th>HS400</th>
<th>HS200</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Write (IOPs)</td>
<td>Read (IOPs)</td>
</tr>
<tr>
<td></td>
<td>Cache ON</td>
<td>Cache OFF</td>
</tr>
<tr>
<td>16GB</td>
<td>3900</td>
<td>1900</td>
</tr>
<tr>
<td>32GB</td>
<td>4100</td>
<td>2300</td>
</tr>
<tr>
<td>64GB</td>
<td>4100</td>
<td>2500</td>
</tr>
<tr>
<td>128GB</td>
<td>4100</td>
<td>2200</td>
</tr>
</tbody>
</table>

Note 1: Sustained Sequential Read/Write performance is measured under HS400 mode with a bus width of 8 bit at 200 MHz DDR mode, chunk size of 512KB, and data transfer of 1GB.

Note 2: Random performance is measured with a chunk size of 4KB and address range of 1GB.

Note 3: All performance is measured using SanDisk proprietary test environment, without file system overhead and host turnaround time (HTAT).

Note 4: Sequential Write performance is measured for 100MB host payloads.
4. PHYSICAL SPECIFICATIONS

The SanDisk iNAND 7232 is a 153-pin, thin fine-pitched ball grid array (BGA). See Figure 3, Figure 4, and Tables 13/14/15 for physical specifications and dimensions.

Figure 2 - INAND 7232 Specification Top and Side View (Detail A)

Figure 3 - Package Outline Drawing – bottom view
### Table 13 – iNAND 7232 Package Specification 16-32GB

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimension In mm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
</tr>
<tr>
<td><strong>A</strong></td>
<td>---</td>
</tr>
<tr>
<td><strong>A1</strong></td>
<td>0.17</td>
</tr>
<tr>
<td><strong>A2</strong></td>
<td>0.54</td>
</tr>
<tr>
<td><strong>C</strong></td>
<td>0.10</td>
</tr>
<tr>
<td><strong>D</strong></td>
<td>11.43</td>
</tr>
<tr>
<td><strong>E</strong></td>
<td>12.93</td>
</tr>
<tr>
<td><strong>DI</strong></td>
<td>---</td>
</tr>
<tr>
<td><strong>EL</strong></td>
<td>---</td>
</tr>
<tr>
<td><strong>e</strong></td>
<td>---</td>
</tr>
<tr>
<td><strong>b</strong></td>
<td>0.25</td>
</tr>
<tr>
<td><strong>aaa</strong></td>
<td>0.10</td>
</tr>
<tr>
<td><strong>bbb</strong></td>
<td>0.10</td>
</tr>
<tr>
<td><strong>ddd</strong></td>
<td>0.08</td>
</tr>
<tr>
<td><strong>eee</strong></td>
<td>0.15</td>
</tr>
<tr>
<td><strong>fff</strong></td>
<td>0.05</td>
</tr>
<tr>
<td><strong>MD/ME</strong></td>
<td>14/14</td>
</tr>
</tbody>
</table>

### Table 14 – iNAND 7232 Package Specification 64GB

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimension In mm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
</tr>
<tr>
<td><strong>A</strong></td>
<td>---</td>
</tr>
<tr>
<td><strong>A1</strong></td>
<td>0.17</td>
</tr>
<tr>
<td><strong>A2</strong></td>
<td>0.64</td>
</tr>
<tr>
<td><strong>C</strong></td>
<td>0.10</td>
</tr>
<tr>
<td><strong>D</strong></td>
<td>11.43</td>
</tr>
<tr>
<td><strong>E</strong></td>
<td>12.93</td>
</tr>
<tr>
<td><strong>DI</strong></td>
<td>---</td>
</tr>
<tr>
<td><strong>EL</strong></td>
<td>---</td>
</tr>
<tr>
<td><strong>e</strong></td>
<td>---</td>
</tr>
<tr>
<td><strong>b</strong></td>
<td>0.25</td>
</tr>
<tr>
<td><strong>aaa</strong></td>
<td>0.10</td>
</tr>
<tr>
<td><strong>bbb</strong></td>
<td>0.10</td>
</tr>
<tr>
<td><strong>ddd</strong></td>
<td>0.08</td>
</tr>
<tr>
<td><strong>eee</strong></td>
<td>0.15</td>
</tr>
<tr>
<td><strong>fff</strong></td>
<td>0.05</td>
</tr>
<tr>
<td><strong>MD/ME</strong></td>
<td>14/14</td>
</tr>
</tbody>
</table>
### Table 15 – iNAND 7232 Package Specification 128GB

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimension in mm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
</tr>
<tr>
<td>A</td>
<td>---</td>
</tr>
<tr>
<td>A1</td>
<td>0.17</td>
</tr>
<tr>
<td>A2</td>
<td>0.81</td>
</tr>
<tr>
<td>C</td>
<td>0.10</td>
</tr>
<tr>
<td>D</td>
<td>11.43</td>
</tr>
<tr>
<td>E</td>
<td>12.93</td>
</tr>
<tr>
<td>H1</td>
<td>---</td>
</tr>
<tr>
<td>P</td>
<td>---</td>
</tr>
<tr>
<td>b</td>
<td>0.25</td>
</tr>
<tr>
<td>w</td>
<td>0.20</td>
</tr>
<tr>
<td>d</td>
<td>0.00</td>
</tr>
<tr>
<td>e</td>
<td>0.10</td>
</tr>
<tr>
<td>ddd</td>
<td>0.08</td>
</tr>
<tr>
<td>eee</td>
<td>0.15</td>
</tr>
<tr>
<td>fff</td>
<td>0.05</td>
</tr>
<tr>
<td>MD/ME</td>
<td>74/74</td>
</tr>
</tbody>
</table>
5. INTERFACE DESCRIPTION

5.1. MMC I/F Ball Array

Figure 4 - 153 balls - Ball Array (Top View)
5.2. Pins and Signal Description

Table 16 contains the SanDisk iNAND 7232, with MMC interface (153 balls), functional pin assignment.

<table>
<thead>
<tr>
<th>Ball No.</th>
<th>Ball Signal</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A3</td>
<td>DAT0</td>
<td>I/O</td>
<td>Data I/O: Bidirectional channel used for data transfer</td>
</tr>
<tr>
<td>A4</td>
<td>DAT1</td>
<td>I/O</td>
<td>Data I/O: Bidirectional channel used for data transfer</td>
</tr>
<tr>
<td>A5</td>
<td>DAT2</td>
<td>I/O</td>
<td>Data I/O: Bidirectional channel used for data transfer</td>
</tr>
<tr>
<td>B2</td>
<td>DAT3</td>
<td>I/O</td>
<td>Data I/O: Bidirectional channel used for data transfer</td>
</tr>
<tr>
<td>B3</td>
<td>DAT4</td>
<td>I/O</td>
<td>Data I/O: Bidirectional channel used for data transfer</td>
</tr>
<tr>
<td>B4</td>
<td>DAT5</td>
<td>I/O</td>
<td>Command: A bidirectional channel used for device initialization and command transfers.</td>
</tr>
<tr>
<td>B5</td>
<td>DAT6</td>
<td>I/O</td>
<td>Command: A bidirectional channel used for device initialization and command transfers.</td>
</tr>
<tr>
<td>B6</td>
<td>DAT7</td>
<td>I/O</td>
<td>Command: A bidirectional channel used for device initialization and command transfers.</td>
</tr>
<tr>
<td>M5</td>
<td>CMD</td>
<td>I/O</td>
<td>Command: A bidirectional channel used for device initialization and command transfers.</td>
</tr>
<tr>
<td>M6</td>
<td>CLK</td>
<td>Input</td>
<td>Clock: Each cycle directs a 1-bit transfer on the command and DAT lines</td>
</tr>
<tr>
<td>K5</td>
<td>RST_n</td>
<td>Input</td>
<td>Hardware Reset</td>
</tr>
<tr>
<td>H5</td>
<td>RCLK</td>
<td>Output</td>
<td>Data Strobe</td>
</tr>
<tr>
<td>E6</td>
<td>VCC</td>
<td>Supply</td>
<td>Flash I/O and memory power supply</td>
</tr>
<tr>
<td>F5</td>
<td>VCC</td>
<td>Supply</td>
<td>Flash I/O and memory power supply</td>
</tr>
<tr>
<td>J10</td>
<td>VCC</td>
<td>Supply</td>
<td>Memory controller core and MMC I/F I/O power supply</td>
</tr>
<tr>
<td>K9</td>
<td>VCC</td>
<td>Supply</td>
<td>Memory controller core and MMC I/F I/O power supply</td>
</tr>
<tr>
<td>C6</td>
<td>VCCQ</td>
<td>Supply</td>
<td>Memory controller core and MMC I/F I/O power supply</td>
</tr>
<tr>
<td>M4</td>
<td>VCCQ</td>
<td>Supply</td>
<td>Memory controller core and MMC I/F I/O power supply</td>
</tr>
<tr>
<td>N4</td>
<td>VCCQ</td>
<td>Supply</td>
<td>Memory controller core and MMC I/F I/O power supply</td>
</tr>
<tr>
<td>P3</td>
<td>VCCQ</td>
<td>Supply</td>
<td>Memory controller core and MMC I/F I/O power supply</td>
</tr>
<tr>
<td>P5</td>
<td>VCCQ</td>
<td>Supply</td>
<td>Memory controller core and MMC I/F ground connection</td>
</tr>
<tr>
<td>E7</td>
<td>VSS</td>
<td>Supply</td>
<td>Flash I/O and memory ground connection</td>
</tr>
<tr>
<td>G5</td>
<td>VSS</td>
<td>Supply</td>
<td>Flash I/O and memory ground connection</td>
</tr>
<tr>
<td>H10</td>
<td>VSS</td>
<td>Supply</td>
<td>Flash I/O and memory ground connection</td>
</tr>
<tr>
<td>K8</td>
<td>VSS</td>
<td>Supply</td>
<td>Flash I/O and memory ground connection</td>
</tr>
<tr>
<td>A6</td>
<td>VSS</td>
<td>Supply</td>
<td>Flash I/O and memory ground connection</td>
</tr>
<tr>
<td>J5</td>
<td>VSS</td>
<td>Supply</td>
<td>Flash I/O and memory ground connection</td>
</tr>
<tr>
<td>C4</td>
<td>VSSQ</td>
<td>Supply</td>
<td>Memory controller core and MMC I/F ground connection</td>
</tr>
<tr>
<td>N2</td>
<td>VSSQ</td>
<td>Supply</td>
<td>Memory controller core and MMC I/F ground connection</td>
</tr>
<tr>
<td>N5</td>
<td>VSSQ</td>
<td>Supply</td>
<td>Memory controller core and MMC I/F ground connection</td>
</tr>
<tr>
<td>P4</td>
<td>VSSQ</td>
<td>Supply</td>
<td>Memory controller core and MMC I/F ground connection</td>
</tr>
<tr>
<td>P6</td>
<td>VSSQ</td>
<td>Supply</td>
<td>Memory controller core and MMC I/F ground connection</td>
</tr>
<tr>
<td>C2</td>
<td>VDDi</td>
<td>VSF</td>
<td>Internal power node. Connect 0.1uF capacitor from VDDi to ground</td>
</tr>
<tr>
<td>E9</td>
<td>VSF1</td>
<td>VSF</td>
<td>Vendor Specific Function balls for test/debug.</td>
</tr>
<tr>
<td>E10</td>
<td>VSF2</td>
<td>VSF</td>
<td>Vendor Specific Function balls for test/debug.</td>
</tr>
<tr>
<td>F10</td>
<td>VSF3</td>
<td>VSF</td>
<td>VSF balls should be floating and be brought out to test pads.</td>
</tr>
<tr>
<td>K10</td>
<td>VSF4</td>
<td>VSF</td>
<td>VSF balls should be floating and be brought out to test pads.</td>
</tr>
</tbody>
</table>

Note: All other pins are not connected [NC] and can be connected to GND or left floating
### 5.3. Registers value

#### 5.3.1. OCR Register

<table>
<thead>
<tr>
<th>Parameter</th>
<th>DSR slice</th>
<th>Description</th>
<th>Value</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>[23:15]</td>
<td>VDD: 2.7 - 3.6 range</td>
<td>1FFh</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>[14:8]</td>
<td>VDD: 2.0 - 2.6 range</td>
<td>00h</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>[7]</td>
<td>VDD: 1.7 - 1.95 range</td>
<td>1h</td>
<td>1</td>
</tr>
</tbody>
</table>

**Note:** Bit 30 is set because the device is High Capacity; bit 31 will be set only when the device is ready.

#### 5.3.2. CID Register

<table>
<thead>
<tr>
<th>Parameter</th>
<th>DSR slice</th>
<th>Description</th>
<th>Value</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>MMC MID</td>
<td>[127:120]</td>
<td>Manufacturer ID</td>
<td>45h</td>
<td>8</td>
</tr>
<tr>
<td>CBX</td>
<td>[113:112]</td>
<td>Card BGA</td>
<td>01h</td>
<td>2</td>
</tr>
<tr>
<td>OID</td>
<td>[111:104]</td>
<td>OEM/Application ID</td>
<td>00h</td>
<td>8</td>
</tr>
<tr>
<td>PNM</td>
<td>[103:56]</td>
<td>Product name</td>
<td>16GB-DF4016 32GB-DF4032 64GB-DF4064 128GB-DF4128</td>
<td>48</td>
</tr>
<tr>
<td>PRV</td>
<td>[55:48]</td>
<td>Product revision</td>
<td>01h</td>
<td>8</td>
</tr>
<tr>
<td>PSN</td>
<td>[47:16]</td>
<td>Product serial number</td>
<td>Random by Production</td>
<td>32</td>
</tr>
<tr>
<td>MDT</td>
<td>[15:8]</td>
<td>Manufacturing date</td>
<td>month, year</td>
<td>8</td>
</tr>
<tr>
<td>CRC</td>
<td>[7:1]</td>
<td>Calculated CRC</td>
<td>CRC7 Generator</td>
<td>7</td>
</tr>
</tbody>
</table>

**Note:** Please refer to the definition of the MDT field as defined in eMMC Spec version 5.0.

#### 5.3.3. DSR Register

<table>
<thead>
<tr>
<th>Parameter</th>
<th>DSR slice</th>
<th>Description</th>
<th>Value</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSRVD</td>
<td>[15:8]</td>
<td>Reserved</td>
<td>04h</td>
<td>8</td>
</tr>
<tr>
<td>RSRVD</td>
<td>[7:0]</td>
<td>Reserved</td>
<td>04h</td>
<td>8</td>
</tr>
</tbody>
</table>

**Note:** DSR is not implemented; in case of read, a value of 0x0404 will be returned.

#### 5.3.4. CSD Register

<table>
<thead>
<tr>
<th>Parameter</th>
<th>CSD Slice</th>
<th>Description</th>
<th>Value</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD_STRUCTURE</td>
<td>[127:126]</td>
<td>CSD structure</td>
<td>3h</td>
<td>3</td>
</tr>
<tr>
<td>SPEC_VERS</td>
<td>[125:122]</td>
<td>System specification version</td>
<td>4h</td>
<td>4</td>
</tr>
<tr>
<td>TAAC</td>
<td>[119:112]</td>
<td>Data read access-time 1</td>
<td>0Fh</td>
<td>8</td>
</tr>
<tr>
<td>NSAC</td>
<td>[111:104]</td>
<td>Data read access-time 2 in CLK cycles (NSAC*100)</td>
<td>00h</td>
<td>8</td>
</tr>
</tbody>
</table>
### 5.3.5. EXT_CSD Register

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ECSD slice</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>S_CMD_SET</td>
<td>[504]</td>
<td>Supported Command Sets</td>
<td>1h</td>
</tr>
<tr>
<td>HPI_FEATURES</td>
<td>[503]</td>
<td>HPI Features</td>
<td>1h</td>
</tr>
<tr>
<td>BKOPS_SUPPORT</td>
<td>[502]</td>
<td>Background operations support</td>
<td>1h</td>
</tr>
<tr>
<td>MAX_PACKED_READS</td>
<td>[501]</td>
<td>Max packed read commands</td>
<td>3Fh</td>
</tr>
<tr>
<td>MAX_PACKED_WRITES</td>
<td>[500]</td>
<td>Max packed write commands</td>
<td>3Fh</td>
</tr>
<tr>
<td>Parameter</td>
<td>ECSD slice</td>
<td>Description</td>
<td>Value</td>
</tr>
<tr>
<td>---------------------------------</td>
<td>------------</td>
<td>--------------------------------------------------</td>
<td>--------</td>
</tr>
<tr>
<td>DATA_TAG_SUPPORT</td>
<td>[499]</td>
<td>Data Tag Support</td>
<td>1h</td>
</tr>
<tr>
<td>TAG_UNIT_SIZE</td>
<td>[498]</td>
<td>Tag Unit Size</td>
<td>3h</td>
</tr>
<tr>
<td>TAG_RES_SIZE</td>
<td>[497]</td>
<td>Tag Resources Size</td>
<td>3h</td>
</tr>
<tr>
<td>CONTEXT_CAPABILITIES</td>
<td>[496]</td>
<td>Context management capabilities</td>
<td>5h</td>
</tr>
<tr>
<td>LARGE_UNIT_SIZE_M1</td>
<td>[495]</td>
<td>Large Unit size</td>
<td>0h</td>
</tr>
<tr>
<td>EXT_SUPPORT</td>
<td>[494]</td>
<td>Extended partitions attribute support</td>
<td>3h</td>
</tr>
<tr>
<td>SUPPORTED_MODES</td>
<td>[493]</td>
<td>FFU supported modes</td>
<td>3h</td>
</tr>
<tr>
<td>FFU_FEATURES</td>
<td>[492]</td>
<td>FFU features</td>
<td>0h</td>
</tr>
<tr>
<td>OPERATION_CODES_TIMEOUT</td>
<td>[491]</td>
<td>Operation codes timeout</td>
<td>10h</td>
</tr>
<tr>
<td>FFU_ARG</td>
<td>[490:487]</td>
<td>FFU Argument</td>
<td>0h</td>
</tr>
<tr>
<td>BARRIER_SUPPORT</td>
<td>[486]</td>
<td>Cache barrier support</td>
<td>1h</td>
</tr>
<tr>
<td>CMDQ_SUPPORT</td>
<td>[308]</td>
<td>Command queue support</td>
<td>1h</td>
</tr>
<tr>
<td>CMDQ_DEPTH</td>
<td>[307]</td>
<td>Command queue depth</td>
<td>1Fh</td>
</tr>
<tr>
<td>NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED</td>
<td>[305:302]</td>
<td>Number of FW sectors correctly programmed</td>
<td>0h</td>
</tr>
<tr>
<td>VENDOR_PROPRIETARY_HEALTH_REPORT</td>
<td>[301:270]</td>
<td>Vendor proprietary health report</td>
<td>0h</td>
</tr>
<tr>
<td>DEVICE_LIFE_TIME_EST_TYP_B</td>
<td>[269]</td>
<td>Device life time estimation type B (MLC)</td>
<td>1h</td>
</tr>
<tr>
<td>DEVICE_LIFE_TIME_EST_TYP_A</td>
<td>[268]</td>
<td>Device life time estimation type A (SLC)</td>
<td>1h</td>
</tr>
<tr>
<td>PRE_EOL_INFO</td>
<td>[267]</td>
<td>Pre EOL information</td>
<td>1h</td>
</tr>
<tr>
<td>OPTIMAL_READ_SIZE</td>
<td>[266]</td>
<td>Optimal read size</td>
<td>8h</td>
</tr>
<tr>
<td>OPTIMAL_WRITE_SIZE</td>
<td>[265]</td>
<td>Optimal write size</td>
<td>8h</td>
</tr>
<tr>
<td>OPTIMAL_TRIM_UNIT_SIZE</td>
<td>[264]</td>
<td>Optimal trim unit size</td>
<td>8h</td>
</tr>
<tr>
<td>DEVICE_VERSION</td>
<td>[263:262]</td>
<td>Device version</td>
<td>5341h</td>
</tr>
<tr>
<td>PWR_CL_DDR_200_360</td>
<td>[253]</td>
<td>Power class for 200MHz, DDR at VCC= 3.6V</td>
<td>0h</td>
</tr>
<tr>
<td>CACHE_SIZE</td>
<td>[252:249]</td>
<td>Cache size</td>
<td>1000h</td>
</tr>
<tr>
<td>GENERIC_CMD6_TIME</td>
<td>[248]</td>
<td>Generic CMD6 timeout</td>
<td>19h</td>
</tr>
<tr>
<td>POWER_OFF_LONG_TIME</td>
<td>[247]</td>
<td>Power off notification (long) timeout</td>
<td>Ah</td>
</tr>
<tr>
<td>BKOPS_STATUS</td>
<td>[246]</td>
<td>Background operations status</td>
<td>Default = 0h</td>
</tr>
<tr>
<td>CORRECTLY_PRG_SECTORS_NUM</td>
<td>[245:242]</td>
<td>Number of correctly programmed sectors</td>
<td>Default = 0h</td>
</tr>
<tr>
<td>INI_TIMEOUT_AP</td>
<td>[241]</td>
<td>1st Initialization time after partitioning</td>
<td>50h</td>
</tr>
<tr>
<td>Parameter</td>
<td>ECSD slice</td>
<td>Description</td>
<td>Value</td>
</tr>
<tr>
<td>----------------------------</td>
<td>------------</td>
<td>------------------------------------------------------------------------------</td>
<td>-------</td>
</tr>
<tr>
<td>CACHE_FLUSH_POLICY</td>
<td>[240]</td>
<td>Cache Flush Policy</td>
<td>1h</td>
</tr>
<tr>
<td>PWR_CL_DDR_52_360</td>
<td>[239]</td>
<td>Power class for 52MHz DDR at VCC = 3.6V</td>
<td>0h</td>
</tr>
<tr>
<td>PWR_CL_DDR_52_195</td>
<td>[238]</td>
<td>Power class for 52MHz DDR at VCC = 1.95V</td>
<td>0h</td>
</tr>
<tr>
<td>PWR_CL_200_195</td>
<td>[237]</td>
<td>Power class for 200MHz at VCCQ = 1.95V, VCC = 3.6V</td>
<td>0h</td>
</tr>
<tr>
<td>PWR_CL_200_130</td>
<td>[236]</td>
<td>Power class for 200MHz, at VCCQ = 1.3V, VCC = 3.6V</td>
<td>0h</td>
</tr>
<tr>
<td>MIN_PERF_DDR_W_8_52</td>
<td>[235]</td>
<td>Minimum Write Performance for 8bit at 52MHz in DDR mode</td>
<td>0h</td>
</tr>
<tr>
<td>MIN_PERF_DDR_R_8_52</td>
<td>[234]</td>
<td>Minimum Read Performance for 8bit at 52MHz in DDR mode</td>
<td>0h</td>
</tr>
<tr>
<td>TRIM_MULTI</td>
<td>[232]</td>
<td>TRIM Multiplier</td>
<td>3h</td>
</tr>
<tr>
<td>SEC_FEATURE_SUPPORT</td>
<td>[231]</td>
<td>Secure Feature support</td>
<td>55h</td>
</tr>
<tr>
<td>SEC_ERASE_MULTI</td>
<td>[230]</td>
<td>Secure Erase Multiplier</td>
<td>A6h</td>
</tr>
<tr>
<td>SEC_TRIM_MULTI</td>
<td>[229]</td>
<td>Secure TRIM Multiplier</td>
<td>A6h</td>
</tr>
<tr>
<td>BOOT_INFO</td>
<td>[228]</td>
<td>Boot Information</td>
<td>7h</td>
</tr>
<tr>
<td>BOOT_SIZE_MULTI</td>
<td>[226]</td>
<td>Boot partition size</td>
<td>20h</td>
</tr>
<tr>
<td>ACCESS_SIZE</td>
<td>[225]</td>
<td>Access size</td>
<td>8h</td>
</tr>
<tr>
<td>HC_ERASE_GROUP_SIZE</td>
<td>[224]</td>
<td>High Capacity Erase unit size</td>
<td>1h (see WP group size table below)</td>
</tr>
<tr>
<td>ERASE_TIMEOUT_MULTI</td>
<td>[223]</td>
<td>High capacity erase time out</td>
<td>3h</td>
</tr>
<tr>
<td>REL_WR_SEC_C</td>
<td>[222]</td>
<td>Reliable write sector count</td>
<td>10h</td>
</tr>
<tr>
<td>HC_WP_GRP_SIZE</td>
<td>[221]</td>
<td>High capacity write protect group size</td>
<td>10h (see WP group size table below)</td>
</tr>
<tr>
<td>S_C_VCC</td>
<td>[220]</td>
<td>Sleep current [VCC]</td>
<td>8h</td>
</tr>
<tr>
<td>S_C_VCCQ</td>
<td>[219]</td>
<td>Sleep current [VCCQ]</td>
<td>7h</td>
</tr>
<tr>
<td>PRODUCTION_STATE_AWARENIS_TIMEOUT</td>
<td>[218]</td>
<td>Production state awareness timeout</td>
<td>Ch</td>
</tr>
<tr>
<td>S_A_TIMEOUT</td>
<td>[217]</td>
<td>Sleep/Awake time out</td>
<td>12h</td>
</tr>
<tr>
<td>SLEEP_NOTIFICATION_TIME</td>
<td>[216]</td>
<td>Sleep notification timeout</td>
<td>17h</td>
</tr>
<tr>
<td>SEC_COUNT</td>
<td>[215:212]</td>
<td>Sector count</td>
<td>See exported capacity table below</td>
</tr>
</tbody>
</table>
| SECURE_WP_INFO             | [211]      | Secure Write Protect Info                                                    | * 0h – for SKU SDINADF4-xxxG & SKU SDINADF4-xxxG-L  
* 1h – for SDINADF4-xxxG-H |
<p>| MIN_PERF_W_8_52            | [210]      | Minimum Write Performance for 8bit @52MHz                                   | Ah    |
| MIN_PERF_R_8_52            | [209]      | Minimum Read Performance for 8bit @52MHz                                     | Ah    |
| MIN_PERF_W_8_26_4_52       | [208]      | Minimum Write Performance for 4bit @52MHz or 8bit @26MHz                     | Ah    |
| MIN_PERF_R_8_26_4_5        | [207]      | Minimum Read Performance for 4bit @52MHz or 8bit @26MHz                       | Ah    |</p>
<table>
<thead>
<tr>
<th>Parameter</th>
<th>ECSD slice</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td></td>
<td>8bit @26MHz</td>
<td>Ah</td>
</tr>
<tr>
<td>MIN_PERF_W_4_26</td>
<td>[206]</td>
<td>Minimum Write Performance for 4bit @26MHz</td>
<td>Ah</td>
</tr>
<tr>
<td>MIN_PERF_R_4_26</td>
<td>[205]</td>
<td>Minimum Read Performance for 4bit @26MHz</td>
<td>Ah</td>
</tr>
<tr>
<td>PWR_CL_26_360</td>
<td>[203]</td>
<td>Power Class for 26MHz @ 3.6V</td>
<td>0x0</td>
</tr>
<tr>
<td>PWR_CL_52_360</td>
<td>[202]</td>
<td>Power Class for 52MHz @ 3.6V</td>
<td>0x0</td>
</tr>
<tr>
<td>PWR_CL_26_195</td>
<td>[201]</td>
<td>Power Class for 26MHz @ 1.95V</td>
<td>DDh</td>
</tr>
<tr>
<td>PWR_CL_52_195</td>
<td>[200]</td>
<td>Power Class for 52MHz @ 1.95V</td>
<td>0h</td>
</tr>
<tr>
<td>PARTITION_SWITCH_TIME</td>
<td>[199]</td>
<td>Partition switching timing</td>
<td>3h</td>
</tr>
<tr>
<td>OUT_OF_INTERRUPT_TIME</td>
<td>[198]</td>
<td>Out-of-interrupt busy timing</td>
<td>5h</td>
</tr>
<tr>
<td>DRIVER_STRENGTH</td>
<td>[197]</td>
<td>I/O Driver Strength</td>
<td>1h</td>
</tr>
<tr>
<td>DEVICE_TYPE</td>
<td>[196]</td>
<td>Device Type</td>
<td>57h</td>
</tr>
<tr>
<td>CSD_STRUCTURE</td>
<td>[194]</td>
<td>CSD Structure Version</td>
<td>2h</td>
</tr>
<tr>
<td>EXT_CSD_REV</td>
<td>[192]</td>
<td>Extended CSD Revision</td>
<td>* 7h – for SKU SDINADF4-xxxG &amp; SDINADF4-xxxG-L &amp; SDINADF4-xxxG-H</td>
</tr>
<tr>
<td>CMD_SET</td>
<td>[191]</td>
<td>Command Set</td>
<td>Default = 0h Updated in runtime</td>
</tr>
<tr>
<td>CMD_SET_REV</td>
<td>[189]</td>
<td>Command Set Revision</td>
<td>0h</td>
</tr>
<tr>
<td>POWER_CLASS</td>
<td>[187]</td>
<td>Power Class</td>
<td>Dh</td>
</tr>
<tr>
<td>HS_TIMING</td>
<td>[185]</td>
<td>High Speed Interface Timing</td>
<td>Default = 0h Updated in runtime by the host</td>
</tr>
<tr>
<td>DATA_STRB_MODE_SUPPORT</td>
<td>[184]</td>
<td>Data strobe mode support</td>
<td>1h</td>
</tr>
<tr>
<td>BUS_WIDTH</td>
<td>[183]</td>
<td>Bus Width Mode</td>
<td>Default = 0h Updated in runtime by the host</td>
</tr>
<tr>
<td>ERASE_MEM_CONT</td>
<td>[181]</td>
<td>Content of explicit erased memory range</td>
<td>0h</td>
</tr>
<tr>
<td>PARTITION_CONFIG</td>
<td>[179]</td>
<td>Partition Configuration</td>
<td>Default = 0h Updated in runtime by the host</td>
</tr>
<tr>
<td>BOOT_CONFIG_PROT</td>
<td>[178]</td>
<td>Boot config protection</td>
<td>Default = 0h Updated in runtime by the host</td>
</tr>
<tr>
<td>BOOT_BUS_CONDITIONS</td>
<td>[177]</td>
<td>Boot bus width1</td>
<td>Default = 0h Updated in runtime by the host</td>
</tr>
<tr>
<td>ERASE_GROUP_DEF</td>
<td>[175]</td>
<td>High-density erase group definition</td>
<td>Default = 0h Updated in runtime by the host</td>
</tr>
<tr>
<td>BOOT_WP_STATUS</td>
<td>[174]</td>
<td>Boot write protection status registers</td>
<td>Default = 0h Updated in runtime</td>
</tr>
<tr>
<td>BOOT_WP</td>
<td>[173]</td>
<td>Boot area write protect register</td>
<td>0h</td>
</tr>
<tr>
<td>Parameter</td>
<td>ECSD slice</td>
<td>Description</td>
<td>Value</td>
</tr>
<tr>
<td>----------------------------</td>
<td>------------</td>
<td>-------------------------------------------</td>
<td>----------------------------</td>
</tr>
<tr>
<td>USER_WP</td>
<td>[171]</td>
<td>User area write protect register</td>
<td>0h</td>
</tr>
<tr>
<td>FW_CONFIG</td>
<td>[169]</td>
<td>FW Configuration</td>
<td>0h</td>
</tr>
<tr>
<td>RPMB_SIZE_MULT</td>
<td>[168]</td>
<td>RPMB Size</td>
<td>20h</td>
</tr>
<tr>
<td>WR_REL_SET</td>
<td>[167]</td>
<td>Write reliability setting register</td>
<td>1Fh</td>
</tr>
<tr>
<td>WR_REL_PARAM</td>
<td>[166]</td>
<td>Write reliability parameter register</td>
<td>15h</td>
</tr>
<tr>
<td>SANITIZE_START</td>
<td>[165]</td>
<td>Start Sanitize operation</td>
<td>Default = 0h Updated in runtime by the host</td>
</tr>
<tr>
<td>BKOPS_START</td>
<td>[164]</td>
<td>Manually start background operations</td>
<td>Default = 0h Updated in runtime by the host</td>
</tr>
<tr>
<td>BKOPS_EN</td>
<td>[163]</td>
<td>Enable background operations handshake</td>
<td>* 0h – for SKU SDINADF4-xxxG &amp; SDINADF4-xxxG-H * 2h – for SKU SDINADF4-xxxG-L &amp; SDINADF4-xxxG-H</td>
</tr>
<tr>
<td>RST_n_FUNCTION</td>
<td>[162]</td>
<td>H/W reset function</td>
<td>Default = 0h Updated by the host</td>
</tr>
<tr>
<td>HPI_MGMT</td>
<td>[161]</td>
<td>HPI management</td>
<td>Default = 0h Updated by the host</td>
</tr>
<tr>
<td>PARTITIONING SUPPORT</td>
<td>[160]</td>
<td>Partitioning support</td>
<td>7h</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Note: EUDA is not supported</td>
<td></td>
</tr>
<tr>
<td>MAX_ENH_SIZE_MULT</td>
<td>[159:157]</td>
<td>Max Enhanced Area Size</td>
<td>16GB = 0x24E</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>32GB = 0x492</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>64GB = 0x925</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>128GB = 0x124C</td>
</tr>
<tr>
<td>PARTITIONS_ATTRIBUTE</td>
<td>[156]</td>
<td>Partitions Attribute</td>
<td>Default = 0h Updated by the host</td>
</tr>
<tr>
<td>PARTITION_SETTING_COMPLETED</td>
<td>[155]</td>
<td>Partitioning Setting</td>
<td>Default = 0h Updated by the host</td>
</tr>
<tr>
<td>GP_SIZE_MULT</td>
<td>[154:143]</td>
<td>General Purpose Partition Size (GP4)</td>
<td>0h</td>
</tr>
<tr>
<td>GP_SIZE_MULT</td>
<td>[151:149]</td>
<td>General Purpose Partition Size (GP3)</td>
<td>0h</td>
</tr>
<tr>
<td>GP_SIZE_MULT</td>
<td>[148:146]</td>
<td>General Purpose Partition Size (GP2)</td>
<td>0h</td>
</tr>
<tr>
<td>GP_SIZE_MULT</td>
<td>[145:143]</td>
<td>General Purpose Partition Size (GP1)</td>
<td>0h</td>
</tr>
<tr>
<td>ENH_SIZE_MULT</td>
<td>[142:140]</td>
<td>Enhanced User Data Area Size</td>
<td>0h</td>
</tr>
<tr>
<td>ENH_START_ADDR</td>
<td>[139:136]</td>
<td>Enhanced User Data Start Address</td>
<td>0h</td>
</tr>
<tr>
<td>SEC_BAD_BLK_MGMNT</td>
<td>[134]</td>
<td>Bad Block Management mode</td>
<td>0h</td>
</tr>
<tr>
<td>PRODUCTION_STATE_AWARENESS</td>
<td>[133]</td>
<td>Production state awareness</td>
<td>0h</td>
</tr>
<tr>
<td>TCASE_SUPPORT</td>
<td>[132]</td>
<td>Package Case Temperature is controlled</td>
<td>0h</td>
</tr>
<tr>
<td>PERIODIC_WAKEUP</td>
<td>[131]</td>
<td>Periodic Wake-up</td>
<td>0h</td>
</tr>
<tr>
<td>PROGRAM_CID_CSD_DD</td>
<td>[130]</td>
<td>Program CID/CSD in DDR mode support</td>
<td>0h</td>
</tr>
<tr>
<td>Parameter</td>
<td>ECSD slice</td>
<td>Description</td>
<td>Value</td>
</tr>
<tr>
<td>-----------------------------------------------</td>
<td>------------</td>
<td>-----------------------------------------------------------------------------</td>
<td>------------------------</td>
</tr>
<tr>
<td>R_SUPPORT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VENDOR_SPECIFIC_FIELD</td>
<td>[127:64]</td>
<td>Vendor Specific Fields</td>
<td>Reserved</td>
</tr>
<tr>
<td>NATIVE_SECTOR_SIZE</td>
<td>[63]</td>
<td>Native sector size</td>
<td>0h</td>
</tr>
<tr>
<td>USE_NATIVE_SECTOR</td>
<td>[62]</td>
<td>Sector size emulation</td>
<td>0h</td>
</tr>
<tr>
<td>DATA_SECTOR_SIZE</td>
<td>[61]</td>
<td>Sector size</td>
<td>0h</td>
</tr>
<tr>
<td>INI_TIMEOUT_EMU</td>
<td>[60]</td>
<td>1st initialization after disabling sector size emulation</td>
<td>Ah</td>
</tr>
<tr>
<td>CLASS_6_CTRL</td>
<td>[59]</td>
<td>Class 6 commands control</td>
<td>0h</td>
</tr>
<tr>
<td>DYNCAP_NEEDED</td>
<td>[58]</td>
<td>Number of addressed group to be Released</td>
<td>0h</td>
</tr>
<tr>
<td>EXCEPTION_EVENTS_CTRL</td>
<td>[57:56]</td>
<td>Exception events control</td>
<td>0h</td>
</tr>
<tr>
<td>EXCEPTION_EVENTS_STATUS</td>
<td>[55:54]</td>
<td>Exception events status</td>
<td>0h</td>
</tr>
<tr>
<td>EXT_PARTITIONS_ATTRIB</td>
<td>[53:52]</td>
<td>Extended Partitions Attribute</td>
<td>0h</td>
</tr>
<tr>
<td>CONTEXT_CONF</td>
<td>[51:37]</td>
<td>Context configuration</td>
<td>Default = 0h</td>
</tr>
<tr>
<td>PACKED_COMMAND_STATUS</td>
<td>[36]</td>
<td>Packed command status</td>
<td>Default = 0h</td>
</tr>
<tr>
<td>PACKED_FAILURE_INDEX</td>
<td>[35]</td>
<td>Packed command failure index</td>
<td>Default = 0h</td>
</tr>
<tr>
<td>POWER_OFF_NOTIFICATION</td>
<td>[34]</td>
<td>Power Off Notification</td>
<td>Default = 0h</td>
</tr>
<tr>
<td>CACHE_CTRL</td>
<td>[33]</td>
<td>Control to turn the Cache ON/OFF</td>
<td>0h</td>
</tr>
<tr>
<td>FLUSH_CACHE</td>
<td>[32]</td>
<td>Flushing of the cache</td>
<td>0h</td>
</tr>
<tr>
<td>BARRIER_CTRL</td>
<td>[31]</td>
<td>Cache barrier</td>
<td>0h</td>
</tr>
<tr>
<td>MODE_CONFIG</td>
<td>[30]</td>
<td>Mode config</td>
<td>0h</td>
</tr>
<tr>
<td>MODE_OPERATION_CODE</td>
<td>[29]</td>
<td>Mode operation codes</td>
<td>0h</td>
</tr>
<tr>
<td>FFU_STATUS</td>
<td>[26]</td>
<td>FFU status</td>
<td>0h</td>
</tr>
<tr>
<td>PRE_LOADING_DATA_SIZE</td>
<td>[25:22]</td>
<td>Pre loading data size</td>
<td>0h</td>
</tr>
<tr>
<td>MAX_PRE_LOADING_DATA_SIZE</td>
<td>[21:18]</td>
<td>Max pre loading data size</td>
<td>See Max Preloading size table below</td>
</tr>
<tr>
<td>PRODUCT_STATE_AWARENESS_ENABLEMENT</td>
<td>[17]</td>
<td>Product state awareness enablement</td>
<td>3h AUTO_PRE_SOLDERING</td>
</tr>
<tr>
<td>SECURE_REMOVAL_TYPE</td>
<td>[16]</td>
<td>Secure Removal Type</td>
<td>8h</td>
</tr>
<tr>
<td>CMDQ_MODE_EN</td>
<td>[15]</td>
<td>Command queue</td>
<td>0h</td>
</tr>
</tbody>
</table>
5.3.6. User Density

The following table shows the capacity available for user data for the different device sizes:

Table 17: Capacity for user data

<table>
<thead>
<tr>
<th>Capacity</th>
<th>LBA [Hex]</th>
</tr>
</thead>
<tbody>
<tr>
<td>16GB</td>
<td>0x1D5A000</td>
</tr>
<tr>
<td>32GB</td>
<td>0x3A3E000</td>
</tr>
<tr>
<td>64GB</td>
<td>0x747C000</td>
</tr>
<tr>
<td>128GB</td>
<td>0xE8F6000</td>
</tr>
</tbody>
</table>

Table 18: Write protect group size

<table>
<thead>
<tr>
<th>Capacity</th>
<th>HC_ERASE_GROUP_SIZE</th>
<th>HC_WP_GRP_SIZE</th>
<th>Erase Unit Size [MB]</th>
<th>Write Protect Group Size [MB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>16GB</td>
<td>1h</td>
<td>10h</td>
<td>0.5MB</td>
<td>8MB</td>
</tr>
<tr>
<td>32GB</td>
<td>1h</td>
<td>10h</td>
<td>0.5MB</td>
<td>8MB</td>
</tr>
<tr>
<td>64GB</td>
<td>1h</td>
<td>10h</td>
<td>0.5MB</td>
<td>8MB</td>
</tr>
<tr>
<td>128GB</td>
<td>1h</td>
<td>10h</td>
<td>0.5MB</td>
<td>8MB</td>
</tr>
</tbody>
</table>

Table 19: Max Preloading Data Size

<table>
<thead>
<tr>
<th>Capacity</th>
<th>Max preloading Image size (in LBA Dec)</th>
<th>Max preloading Image Size (in Bytes)</th>
<th>Max preloading Image Size (in GB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16GB</td>
<td>10,181,096</td>
<td>5,212,721,152</td>
<td>4.85</td>
</tr>
<tr>
<td>32GB</td>
<td>20,178,120</td>
<td>10,331,197,440</td>
<td>9.62</td>
</tr>
<tr>
<td>64GB</td>
<td>40,331,672</td>
<td>20,649,816,064</td>
<td>19.23</td>
</tr>
<tr>
<td>128GB</td>
<td>80,636,064</td>
<td>41,285,664,768</td>
<td>38.45</td>
</tr>
</tbody>
</table>
6. POWER DELIVERY AND CAPACITOR SPECIFICATIONS

6.1. SanDisk iNAND 7232 Power Domains
SanDisk iNAND 7232 has three power domains assigned to VCCQ, VCC and VDDi, as shown in Table 21 below.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Power Domain</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCQ</td>
<td>Host Interface</td>
<td>Supported voltage ranges:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low Voltage Region: 1.8V (nominal)</td>
</tr>
<tr>
<td>VCC</td>
<td>Memory</td>
<td>Supported voltage range:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High Voltage Region: 3.3V (nominal)</td>
</tr>
<tr>
<td>VDDi</td>
<td>Internal</td>
<td>VDDi is the internal regulator connection to an external decoupling capacitor.</td>
</tr>
</tbody>
</table>
6.2. Capacitor Connection Guidelines

It is recommended to place the following capacitors on VCC & VCCQ domains:

- **Cin1 = 4.7uF**
  - E.g.:
    - Manufacturer & Manufacturer P/N
      - MURATA: GRM185R60J475ME15D
      - TAIYO YUDEN: JMK107J475MK-T

- **Cin2 = 0.1uF**
  - E.g.:
    - Manufacturer & Manufacturer P/N
      - MURATA: GRM155R71A104KA01D
      - KYOCERA: CM05X5R104K06AH

For VDDi (1.1V), it is recommended to place:

- **0.1uF <= Cin(VDDi) <= 2.2uF**
  - E.g.:
    - Manufacturer & Manufacturer P/N
      - TAIYO YUDEN: JDK105BJ225MV
      - PANASONIC: ECJ0E0J225M
      - SAMSUNG: CL05A225MQ5NSNC

- For HS200/400 can use 0.1 uF <= Cin(VDDi) <= 2.2uF

Capacitors Type:

- SMT-Ceramic
- X5R/X7R
- 6.3V/10V
- Min height – 0.55mm
- Foot Print: 0402 or above

When using a low value ceramic input filter capacitor, it should be located as close to the supply ball as possible. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply.

Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

Make all of the power (high current) traces as short, direct, and thick as possible. The capacitors should be as close to each other as possible, as it reduces EMI radiated by the power traces due to the high switching currents through them. In addition it shall also reduce lead inductance and
resistance as well, which in turn reduces noise spikes, ringings, and resistive losses which produce voltage errors.

The grounds of the IC capacitors should be connected close together directly to a ground plane. It is also recommended to have a ground plane on both sides of the PCB, as it reduces noise by reducing ground loop errors as well.

The loop inductance per capacitor shall not exceed 3nH (both on VCC/VCCQ & VSS/VSSQ loops).

Cin2 shall be placed closer (from both distance & inductance POV) to the iNAND power & ground balls.

Multiple via connections are recommended per each capacitor pad.

On test platforms, where the iNAND socket is in use, the loop inductance per capacitor shall not exceed 5nH (both on VCC/VCCQ & VSS/VSSQ loop).

No passives should be placed below the iNAND device (between iNAND & PCB).

VSF balls (VSF1/4) should have exposed and floated test pads on the PCB, with near exposed GND for better measurement.
Signal Traces:

- Data, CMD, CLK & RCLK bus trace length mismatch should be minimal (up to +/-1mm).
- Traces should be 50ohm controlled impedance.

![Diagram of recommended power domain connections]

**Figure 5 - Recommended Power Domain Connections**

Note: Signal routing in the diagram is for illustration purposes only and the final routing depends on the final PCB layout.

For clarity, the diagram does not include VSS connection. All balls marked VSS shall be connected to a ground (GND) plane.

### 6.3. Reference Schematics

- The e.MMC specification enforces single device per host channel; multi-device configuration per a single host channel is not supported.

- CLK, RCLK(DS), CMD and DATx lines should be connected to respected host signals. The e.MMC specification requires that all signals will be connected point-to-point, i.e. a single e.MMC device per host channel.

- The e.MMC hardware reset signal (RST_n) is not mandatory and could be connected to the host reset signal or left unconnected (floating) if not used.

- All power supply and ground pads must be connected.
- Make sure pull-up resistors are placed on schematic in case these are external. For further details please refer to “Table 22 - Pull-ups Definition”

- Bypass capacitors shall be placed as close to the e.MMC device as possible; normally it is recommended to have 0.1µF and 4.7µF capacitors per power supply rail, though specific designs may include a different configuration in which there are more than two capacitors:
  - VCC and VCCQ slew rates shall be minimally affected by any bypass capacitors configuration
  - It is recommended to verify the bypass capacitors requirement in the product data sheet

- VDDi bypass capacitor shall be placed on the PCB. The VDDi is an internal power node for the controller and requires capacitor in range 0.1µF – 2.2µF connected between VDDi pad and ground

- Vendor Specific Function (VSF) pins should be connected to accessible test points on the PCB (TP on schematic below). It’s recommended to have accessible ground (GND) pads near each TP on PCB

- It is recommended to layout e.MMC signals with controlled impedance of 45-50 Ohm referencing to adjusted ground plane

![Figure 6 – e.MMC Package Schematics](image)

**Table 22 – Pull-ups Definition**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pull-up resistance for CMD</td>
<td>R&lt;sub&gt;CMD&lt;/sub&gt;</td>
<td>4.7</td>
<td>100(1)</td>
<td>100(1)</td>
<td>Kohm</td>
<td>to prevent bus floating</td>
</tr>
<tr>
<td>Pull-up resistance for DAT0–7</td>
<td>R&lt;sub&gt;DAT&lt;/sub&gt;</td>
<td>10</td>
<td>100(1)</td>
<td>100(1)</td>
<td>Kohm</td>
<td>to prevent bus floating</td>
</tr>
<tr>
<td>Pull-down resistance for Data Strobe (RCLK)</td>
<td>10</td>
<td>47</td>
<td>Kohm</td>
<td>At HS400 mode</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Recommended maximum pull-up is 50Kohm for 1.8V interface supply voltages. A 3V part may use the whole range up to 100Kohms.
7. **PROPERTY iNAND 7232 FEATURE OVERVIEW**

7.1. **Content Preloading Operation Mode**

High temperature during IR-Reflow process on 1Ynm X3 flash devices cause significant increase of read errors on TLC blocks (Uncorrectable read errors of data that was programmed before the IR Reflow process).

This high level of read errors is higher compared to previous flash technologies. Currently this level of errors cannot be fixed by special error correction algorithms (as it was done in previous flash technologies).

To overcome these challenges in 1Ynm X3 flash devices iNAND 7232 introduced the Pre-Loading feature, which solves the IR-Reflow process’s reliability, by writing the preloaded data to the SLC area of the device.

Every iNAND 7232 fresh device is defined to start in Implicit Loading state. There are several of exit triggers that will switch it to Migration state. Once Migration is completed the device will start to work in normal state.

During Implicit mode all written data (the preloaded data before IR-Reflow) will be written to the SLC area of the device.

Max preloading data allowed is 33% from device exported capacity.

Triggers to exit Implicit mode and start Migration stage are:

- Host accumulated written data payload that is >33% (15% was for CS1.00/CS1.01 previous firmware releases) of the exported capacity.
- Host switches interface to High-Speed bus (HS200/400).
- (Recommended) Host issues Vendor Specific command signals to device signaling “IR-Reflow completed”.

```
Reset Implicit Triggers (3)  
Programmer Pre-Loading image  
Device Soldering (IR Reflow)  

(start) Implicit Loading  
Exist Implicit Triggers (4)  
Migration  
Post Pre-Loading (end)  

"Pre-Loading" Mode
```
Triggers to reset Implicit mode counters (Only possible during Implicit mode and if device switched already to Migration stage there is no option to reverse/reset it to Implicit stage anymore)

- Host erases the whole written user area.
- Host issues Vendor Specific command of “Production Restore To Default”
- Firmware Download

During Migration state the device will do automatic relocation of the preloaded data written to SLC blocks during implicit mode to TLC blocks, after IR reflow.

It is recommended to allow system BKOPS during IDLE time that will expedite the folding of the preloaded data from SLC to the TLC.

Following each of the BKOPS periods (500ms), performance improvement is expected until the iNAND reaches its sustained performance.
7.2. SmartSLC

The iNAND SmartSLC feature gives the customer the write performance they require, so that they will have a UX experience that makes an X3 memory look better than X2. The iNAND SmartSLC provides the following value to the system:

- Auto-adjust iNAND performance per application need
- Improves system efficiency and UX
  - Reduce system WRITE-BUSY time by improving IO throughput
- Vertical iNAND technology:
  - Host access to iNAND NAND flash performance capabilities
  - Controller and Firmware auto-detections of hosts needs and auto-adjustment device behavior based on these host needs
  - Host (eMMC driver) customizations and modifications in IDLE time management to allow optimized utilization of SmartSLC capabilities

iNAND 7232 uses allocated SLC blocks within the SanDisk NAND design to implement the feature. The allocation of these blocks does not impact the as sold capacity of the device (Exported Capacity). The device uses the detection mechanism as described in section xx once a pattern requiring sequential write performance is detected, the device postpones any background management operations, if feasible,) and dedicates resources to SLC programing. Any IDLE state bigger than tIDLE [ms], shall trigger migration operations to free up enough space for the next burst and eliminate potential performance drop.

iNAND SmartSLC buffer size and Performance for SDINADF4-xxxG & SDINADF4-xxxG-L products:

<table>
<thead>
<tr>
<th>Capacity (GB)</th>
<th>Buffer Size (MB)</th>
<th>Write speed * (MB/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16GB</td>
<td>140</td>
<td>95</td>
</tr>
<tr>
<td>32GB</td>
<td>400</td>
<td>150</td>
</tr>
<tr>
<td>64GB</td>
<td>800</td>
<td>150</td>
</tr>
<tr>
<td>128GB</td>
<td>1600</td>
<td>150</td>
</tr>
</tbody>
</table>

iNAND SmartSLC buffer size and Performance for SDINADF4-xxxG-H product (BigFile Mode):

<table>
<thead>
<tr>
<th>Capacity (GB)</th>
<th>Buffer Size (MB)</th>
<th>Write speed * (MB/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16GB</td>
<td>4GB</td>
<td>130</td>
</tr>
<tr>
<td>32GB</td>
<td>8GB</td>
<td>160</td>
</tr>
<tr>
<td>64GB</td>
<td>16GB</td>
<td>160</td>
</tr>
<tr>
<td>128GB</td>
<td>32GB</td>
<td>160</td>
</tr>
</tbody>
</table>

* Sequential write Performance is measured using SanDisk proprietary test environment, without file system overhead and host turn-around time (HTAT), 512KB chunk, enough recovery time before measurement.
Emptying the iNAND SmartSLC buffer

There are a number of host enabled mechanisms that can be used to empty the SmartSLC buffer (migration). All of these modes can be enabled at the same time or only a single or a few modes can be selected. The more modes that are supported by the host, the more the buffer will be available and empty for use in observing host high speed payloads. During migration time there won’t be degradation of device performance and no impact on latency and system responsiveness. Host optional configuration for iNAND SmartSLC:

1. IDLE only mode (PoN=1) – Recommended option.
2. BKOPs APIs with HPI
3. Sleep Notification before standby (CMD5)

<table>
<thead>
<tr>
<th>SmartSLC Buffer migration</th>
<th>1. Host allow House-Keeping during IDLE (Auto BKOps)</th>
<th>2. Host periodically send BKOps API (Manual BKOps)</th>
<th>3. SLEEP-NOTIFICATION before CMD5</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXT_CSD REV[192]</td>
<td>Migration during in system IDLE with HPI</td>
<td>Migration during in system IDLE with HPI</td>
<td>Migration in Sleep-Notification busy</td>
</tr>
<tr>
<td>AUTO_EN BKOPS_EN[163][1]</td>
<td>7h (eMMC 5.0)</td>
<td>8h (eMMC 5.1)</td>
<td>7h or 8h (eMMC 5.0/5.1)</td>
</tr>
<tr>
<td>POWER_OFF_NOTIFICATION [34] (PON activated)</td>
<td>1h (POWERED_ON)</td>
<td>1h (POWERED_ON)</td>
<td>1h (POWERED_ON)</td>
</tr>
<tr>
<td>BKOPS_EN BKOPS_EN[163][0]</td>
<td>Don’t care</td>
<td>Don’t care</td>
<td>1h</td>
</tr>
<tr>
<td>POWER_OFF_NOTIFICATION [34] (Sleep Notification)</td>
<td>No</td>
<td>No</td>
<td>Don’t care</td>
</tr>
<tr>
<td>Standby mode CMD5</td>
<td>If system uses CMD5 it is requires 5-10sec delay before CMD5 transmission</td>
<td>If system uses CMD5 it is requires 5-10sec delay before CMD5 transmission</td>
<td>Don’t care</td>
</tr>
<tr>
<td></td>
<td>System uses of CMD5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 7.3. Device Report

iNAND 7232 introduce new proprietary Device Report feature that reflects the Firmware and Device status.

- **Enabling Device Report Mode:** Send CMD62 with argument of 0x96C9D71C - R1b Response will be returned
- **Reading Device Report Data:** Once the host enters Device Report mode, CMD63 with argument 0x00000000 will retrieve the report - 512 Bytes will be returned to the host (Note: CMD63 behaves similarly to CMD17)
- **Resume Normal Operation Mode:** Once the Device Report read command (CMD63) was completed, the device automatically goes out of Device Report mode, and resumes normal operation mode.

<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Size (Bytes)</th>
<th>Field</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>[3:0]</td>
<td>4</td>
<td>Average Erase Cycles Enhanced</td>
<td>The Average Program/Erase count for all Enhanced Blocks</td>
</tr>
<tr>
<td>[7:4]</td>
<td>4</td>
<td>Average Erase Cycles SLC</td>
<td>The Average Program/Erase count for all SLC Blocks</td>
</tr>
<tr>
<td>[8:8]</td>
<td>4</td>
<td>Average Erase Cycles MLC</td>
<td>The Average Program/Erase count for all MLC Blocks</td>
</tr>
<tr>
<td>[F:C]</td>
<td>4</td>
<td>Read reclaim count Enhanced</td>
<td>The amount of Reads on enhanced area which passed Read-refresh thresholds and requires reclaim</td>
</tr>
<tr>
<td>[13:10]</td>
<td>4</td>
<td>Read reclaim count SLC</td>
<td>The amount of Reads on SLC area which passed Read-refresh thresholds and requires reclaim</td>
</tr>
<tr>
<td>[17:13]</td>
<td>4</td>
<td>Read reclaim count MLC</td>
<td>The amount of Reads on MLC area which passed Read-refresh thresholds and requires reclaim</td>
</tr>
<tr>
<td>[1B:18]</td>
<td>4</td>
<td>Bad Block Manufactory</td>
<td>All BB detected during manufacturing process</td>
</tr>
<tr>
<td>[1F:1C]</td>
<td>4</td>
<td>Bad Block Runtime Enhanced</td>
<td>All BB related to Enhanced partition detected during run-time</td>
</tr>
<tr>
<td>[23:20]</td>
<td>4</td>
<td>Bad Block Runtime SLC</td>
<td>All BB related to SLC partition detected during run-time</td>
</tr>
<tr>
<td>[27:24]</td>
<td>4</td>
<td>Bad Block Runtime MLC</td>
<td>All BB related to MLC partition detected during run-time</td>
</tr>
<tr>
<td>[2B:28]</td>
<td>4</td>
<td>Patch Trial Count</td>
<td>The number of Field Firmware Updates done from the beginning of the device life time</td>
</tr>
<tr>
<td>[37:2C]</td>
<td>12</td>
<td>Patch Release Date</td>
<td>Current FFU Release date</td>
</tr>
<tr>
<td>[3F:38]</td>
<td>8</td>
<td>Patch Release Time</td>
<td>Current FFU Release hour</td>
</tr>
<tr>
<td>[43:40]</td>
<td>4</td>
<td>Cumulative Write data size</td>
<td>Counts the amount of Host Writes transaction (100MB multiplication)</td>
</tr>
<tr>
<td>[47:44]</td>
<td>4</td>
<td>Number of occurrences of VCC voltage drops</td>
<td>Counts the number of ungraceful Power Down to the device</td>
</tr>
<tr>
<td>[4B:48]</td>
<td>4</td>
<td>Number of occurrences of VCC voltage droops</td>
<td>Counts the number of times Power-Droop (Slight power-droop below certain threshold) were detected</td>
</tr>
<tr>
<td>[4F:4C]</td>
<td>4</td>
<td>Number of failures recover new host data after Power Loss</td>
<td>Every time NEW Host data is dismissed due to Power Loss, this counter will be incremented.</td>
</tr>
<tr>
<td>[53:50]</td>
<td>4</td>
<td>Total Recovery Operations After Voltage Droop</td>
<td>The total amount of recovery operation required to be done by the device while power-droop was detected</td>
</tr>
<tr>
<td>[54:57]</td>
<td>4</td>
<td>Cumulative write data size in SmartSLC mode</td>
<td>Counts the amount of Host written data, that were written in SmartSLC mode [in 100MB]</td>
</tr>
<tr>
<td>[58:5B]</td>
<td>4</td>
<td>Cumulative write data size in SLC mode on MLC-designated blocks</td>
<td>Counts the amount of Host written data, that were written as SmartSLC data on MLC-designated blocks [in 100MB]</td>
</tr>
</tbody>
</table>
Power-Loss indications:
iNAND 7232 is also serving the host by notifying him on cases of Power-Loss events and internal handling of those events. A dedicated field in the EXT_CSD register was allocated to indicate the occurrence of Power Loss/Write Abort during the last power down. This field reports if a Power Loss was detected and recovered during the last power-up.
In order to retrieve this field the host should issue CMD8 command – SEND_EXT_CSD. This command returns full EXT_CSD structure – 512 bytes as block of data. Following is the EXT_CSD field details:

<table>
<thead>
<tr>
<th>Name</th>
<th>Field</th>
<th>Size (bytes)</th>
<th>Cell Type</th>
<th>Hex Offset</th>
<th>Dec. Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Loss indication</td>
<td>POWER LOSS REPORT</td>
<td>1</td>
<td>R</td>
<td>0x79</td>
<td>121</td>
</tr>
</tbody>
</table>

POWER LOSS REPORT[121] details:
- Bit[2]: RECOVERY_SUCCESS
  0x1: Recovery passed successfully
  0x0: Recovery failed
- Bit[1]: RECOVER_OLD_DATA
  0x1: Recovery to old copy of data
  0x0: No data recovery required
- Bit[0]: POWER LOSS DETECTED
  0x1: Unexpected Power Loss was detected - Detection is done during initialization, immediately after Power-Up

Note: In case Power Loss did not occur on last shut down, this register will show 0x00

Unstable Power-Supply indications:
In case of Flash voltage drop, the iNAND may not be able to recover the data that was already transferred to the iNAND device, but wasn’t committed in the Flash. In this case the iNAND will “abort” the current host write and return back to the host with an error indication.
iNAND 7232 will use BIT19 and BIT20 (cc_error) in the command response to indicate VDET error status to the host. The VDET error indication can be seen only if CMD13 was issued, or in the next command response.

Examples:
- Open Mode (CMD25+CMD12+CMD13):
  In both cases, where the voltage droop occurs before or after CMD12: CMD12 response will not have BIT19 and BIT20 set.
CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response
Note: The host may send many CMD13 and the BIT19 will be set only in first CMD13 after releasing the busy.

- Close Mode (CMD23+CMD25+CMD13):
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response
- Single Block Mode (CMD24+CMD13):
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response

Host shall retry latest command as long as the VDET error indication on CMD13 response (or next command response (BIT19 and BIT20 are set) is still set
8. MARKING

First row: Simplified SanDisk Logo
Second row: Sales item P/N
Third row: Country of origin i.e. ‘TAIWAN’ or ‘CHINA’
* No ES marking for product in mass production.
Fourth row: Y- Last digit of year
            WW- Work week
            D- A day within the week.
            MTLLLLXX – Internal use
2D barcode: Store the 12 Digital unique ID information as reflected in the fourth row.

Figure 7 - Product marking 16G-64GB

Figure 8 - Product marking 128GB
9. ORDERING INFORMATION

Table 23 – Ordering Information

<table>
<thead>
<tr>
<th>Capacity</th>
<th>Technology</th>
<th>Part Number</th>
<th>Samples Part Number</th>
<th>Package</th>
<th>eMMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>16GB</td>
<td>X3</td>
<td>SDINADF4-16G</td>
<td>SDINADF4-16G-Q</td>
<td>11.5x13x0.9mm</td>
<td>5.0</td>
</tr>
<tr>
<td>16GB</td>
<td>X3</td>
<td>SDINADF4-16G-L</td>
<td>SDINADF4-16G-LQ</td>
<td>11.5x13x0.9mm</td>
<td>5.1</td>
</tr>
<tr>
<td>16GB</td>
<td>X3</td>
<td>SDINADF4-16G-H</td>
<td>SDINADF4-16G-HQ</td>
<td>11.5x13x0.9mm</td>
<td>5.1</td>
</tr>
<tr>
<td>32GB</td>
<td>X3</td>
<td>SDINADF4-32G</td>
<td>SDINADF4-32G-Q</td>
<td>11.5x13x0.9mm</td>
<td>5.0</td>
</tr>
<tr>
<td>32GB</td>
<td>X3</td>
<td>SDINADF4-32G-L</td>
<td>SDINADF4-32G-LQ</td>
<td>11.5x13x0.9mm</td>
<td>5.1</td>
</tr>
<tr>
<td>32GB</td>
<td>X3</td>
<td>SDINADF4-32G-H</td>
<td>SDINADF4-32G-HQ</td>
<td>11.5x13x0.9mm</td>
<td>5.1</td>
</tr>
<tr>
<td>64GB</td>
<td>X3</td>
<td>SDINADF4-64G</td>
<td>SDINADF4-64G-Q</td>
<td>11.5x13x1.0mm</td>
<td>5.0</td>
</tr>
<tr>
<td>64GB</td>
<td>X3</td>
<td>SDINADF4-64G-L</td>
<td>SDINADF4-64G-LQ</td>
<td>11.5x13x1.0mm</td>
<td>5.1</td>
</tr>
<tr>
<td>64GB</td>
<td>X3</td>
<td>SDINADF4-64G-H</td>
<td>SDINADF4-64G-HQ</td>
<td>11.5x13x1.0mm</td>
<td>5.1</td>
</tr>
<tr>
<td>128GB</td>
<td>X3</td>
<td>SDINADF4-128G</td>
<td>SDINADF4-128G-Q</td>
<td>11.5x13x1.2mm</td>
<td>5.0</td>
</tr>
<tr>
<td>128GB</td>
<td>X3</td>
<td>SDINADF4-128G-L</td>
<td>SDINADF4-128G-LQ</td>
<td>11.5x13x1.2mm</td>
<td>5.1</td>
</tr>
<tr>
<td>128GB</td>
<td>X3</td>
<td>SDINADF4-128G-H</td>
<td>SDINADF4-128G-HQ</td>
<td>11.5x13x1.2mm</td>
<td>5.1</td>
</tr>
</tbody>
</table>

Note: Optional Customer Code, when applicable, will be added at the end of the part number (e.g. SDINADF4-32G-XXX or SDINADF4-32G-XXXQ).
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