Mobile LPDDR3 SDRAM

AWL3A1632-12D2LK35CS

Features

- Density: 16Gb
- Data rate: 800Mhz(1600Mbps)
- 8n prefetch DDR architecture
- Array configuration
  – 512 Meg x 32 (DDP)
- Interface: HSUL_12
- Burst lengths(BL):8
- Burst type(BT)
- Read latency(RL):3,6,8,9,10,11,12

Key Options

- Power supply:
  V_{DD1} =1.8V
  V_{DD2} =1.2V
  V_{DDCA}=1.2V
  V_{DDQ} =1.2V
- Array configuration
  – 512 Meg x 32 (DDP)
- Packaging
  – 11mm x 11.5mm x 0.85mm, 178-ball FBGA
- Operating temperature range
  – From 0°C to +75°C

Part Numbering Information

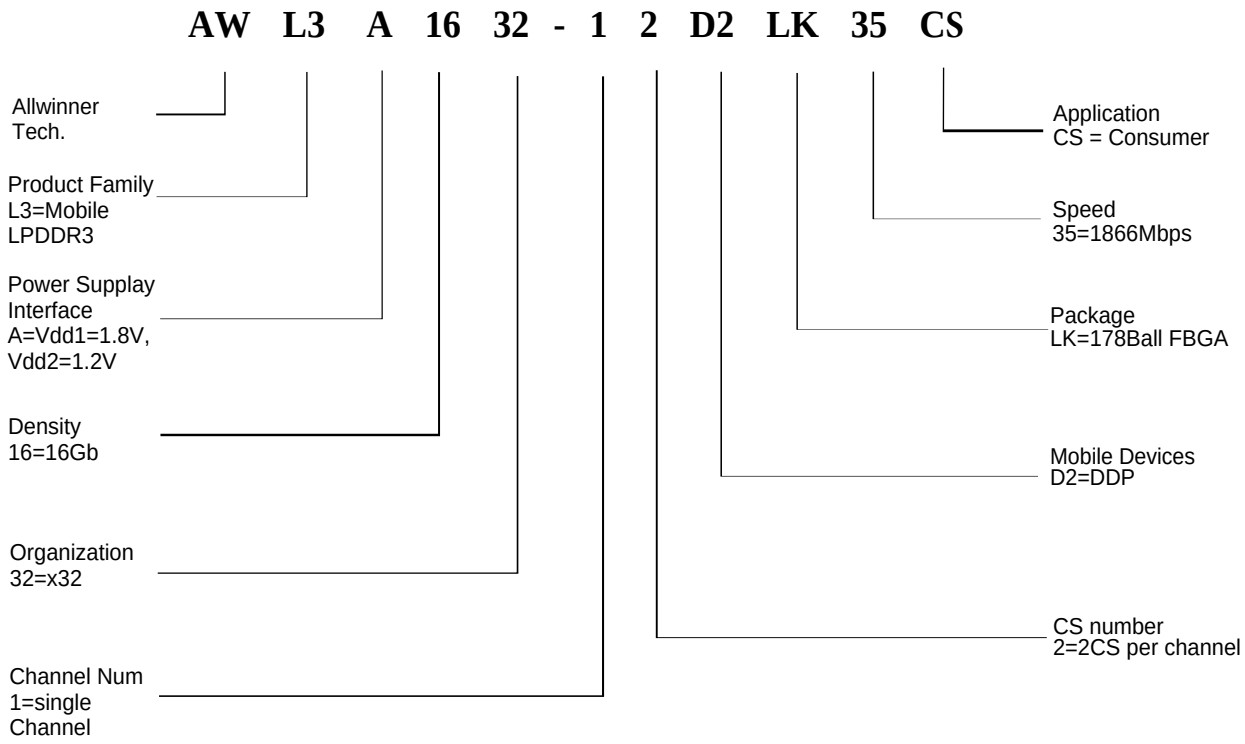
Low Power memory devices are available in different configurations and densities.

Table 1: Ordering Information

Base Part Number	Capacity	Organization	Die Num.	Package Size	Ball Pitch
AWL3A1632-12D2L32CS	16Gb	256 x 32 x 2	DDP	178-ball FBGA 11mm x 11.5mm x0.85mm	0.80mm 0.65mm

Part Numbering System

Figure 1: Part Numbering



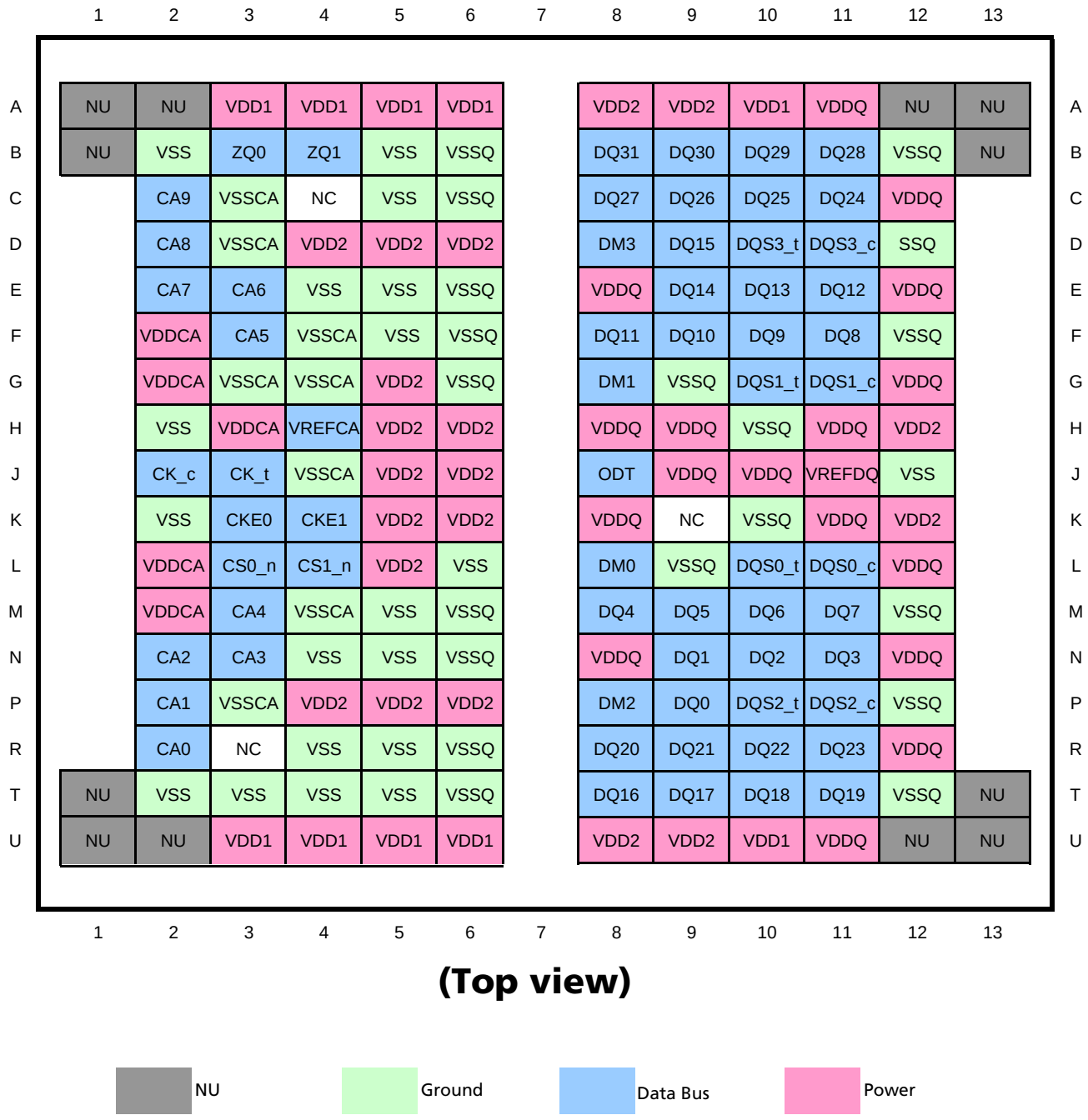
Pin Descriptions

The pin description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See Bond Pad tables for information specific to this device.

Table 2: Pin Descriptions

Symbol	Type	Description
CA[9:0]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
CK_t, CK_c	Input	**Clock:** Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE[1:0]	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled on the rising edge of CK.
CS[1:0]_n	Input	**Chip select:** Considered part of the command code and is sampled on the rising edge of CK.
DM[3:0]	Input	**Input data mask:** Input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
ODT	Input	**On-die termination:** Enables and disables termination on the DRAM DQ bus according to the specified mode register settings. For packages that do not support ODT, the ODT signal may be grounded internally.
DQ[31:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[3:0]_t, DQS[3:0]_c	I/O	**Data strobe:** Bidirectional (used for read and write data) and complementary (DQS_t and DQS_c). It is edge-aligned output with read data and centered input with write data. DQS[3:0]_t/DQS[3:0]_c is DQS for each of the four data bytes, respectively.
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ ground:** Isolated on the die for improved noise immunity.
V_{DDCA}	Supply	**Command/address power supply:** Command/address power supply.
V_{SSCA}	Supply	**Command/address ground:** Isolated on the die for improved noise immunity.
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{SS}	Supply	**Common ground.**
V_{REFCA}, V_{REFDQ}	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers.
ZQ[1:0]	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}
NU	–	**Not usable:** Do not connect.
NC	–	**No connect:** Not internally connected.
(NC)	–	**No connect:** Balls indicated as (NC) are no connects; however, they could be connected together internally.

Figure 2: Ball Assignments

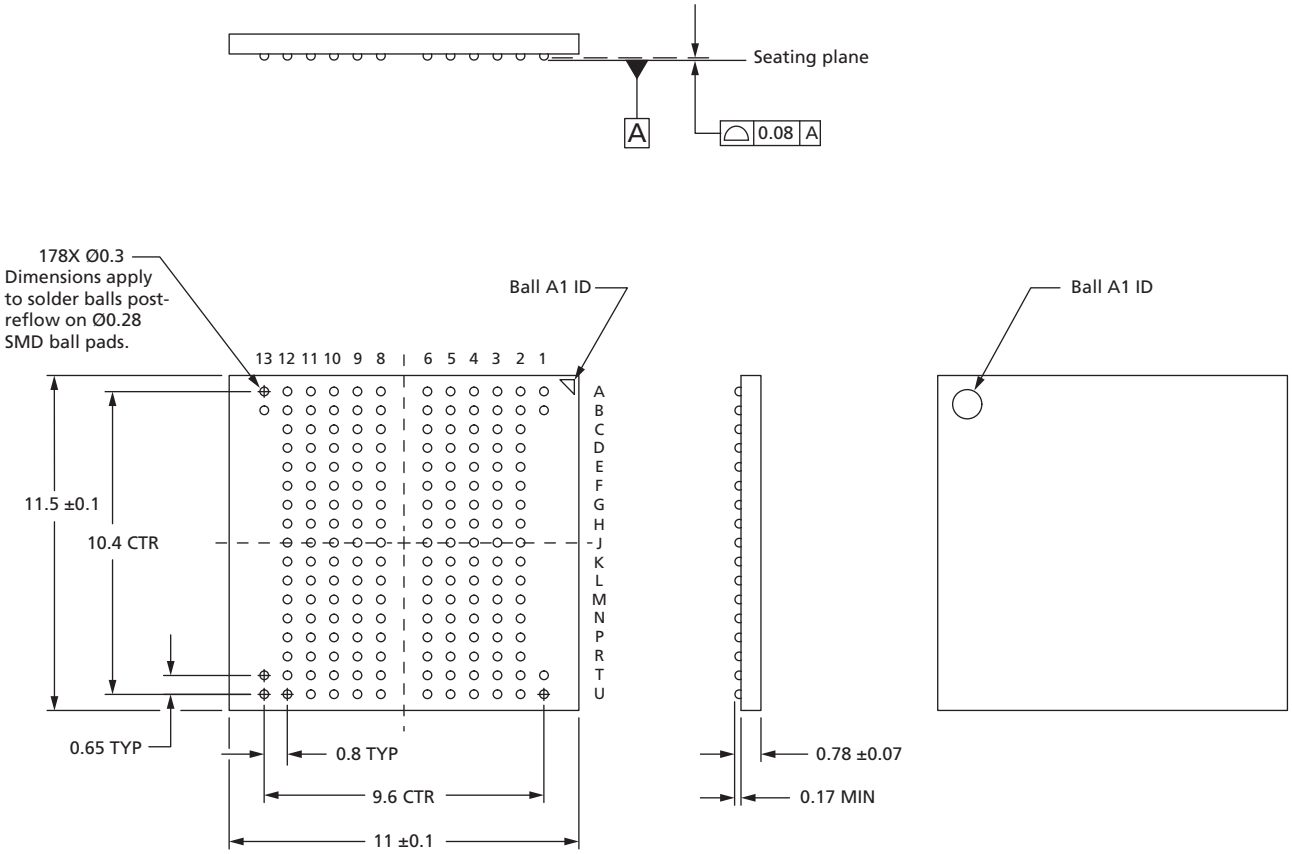


	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NU	NU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	NU	NU
B	NU	VSS	ZQ0	ZQ1	VSS	VSSQ		DQ31	DQ30	DQ29	DQ28	VSSQ	NU
C		CA9	VSSCA	NC	VSS	VSSQ		DQ27	DQ26	DQ25	DQ24	VDDQ	
D		CA8	VSSCA	VDD2	VDD2	VDD2		DM3	DQ15	DQS3_t	DQS3_c	SSQ	
E		CA7	CA6	VSS	VSS	VSSQ		VDDQ	DQ14	DQ13	DQ12	VDDQ	
F		VDDCA	CA5	VSSCA	VSS	VSSQ		DQ11	DQ10	DQ9	DQ8	VSSQ	
G		VDDCA	VSSCA	VSSCA	VDD2	VSSQ		DM1	VSSQ	DQS1_t	DQS1_c	VDDQ	
H		VSS	VDDCA	VREFCA	VDD2	VDD2		VDDQ	VDDQ	VSSQ	VDDQ	VDD2	
J		CK_c	CK_t	VSSCA	VDD2	VDD2		ODT	VDDQ	VDDQ	VREFDQ	VSS	
K		VSS	CKE0	CKE1	VDD2	VDD2		VDDQ	NC	VSSQ	VDDQ	VDD2	
L		VDDCA	CS0_n	CS1_n	VDD2	VSS		DM0	VSSQ	DQS0_t	DQS0_c	VDDQ	
M		VDDCA	CA4	VSSCA	VSS	VSSQ		DQ4	DQ5	DQ6	DQ7	VSSQ	
N		CA2	CA3	VSS	VSS	VSSQ		VDDQ	DQ1	DQ2	DQ3	VDDQ	
P		CA1	VSSCA	VDD2	VDD2	VDD2		DM2	DQ0	DQS2_t	DQS2_c	VSSQ	
R		CA0	NC	VSS	VSS	VSSQ		DQ20	DQ21	DQ22	DQ23	VDDQ	
T	NU	VSS	VSS	VSS	VSS	VSSQ		DQ16	DQ17	DQ18	DQ19	VSSQ	NU
U	NU	NU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	NU	NU

(Top view)

NU Ground Data Bus Power

Figure 3: Package Drawing 178Ball



Note: 1. All dimensions are in millimeters.

Figure 4: Dual-Rank, Dual-Die, Single-Channel Package Block Diagram

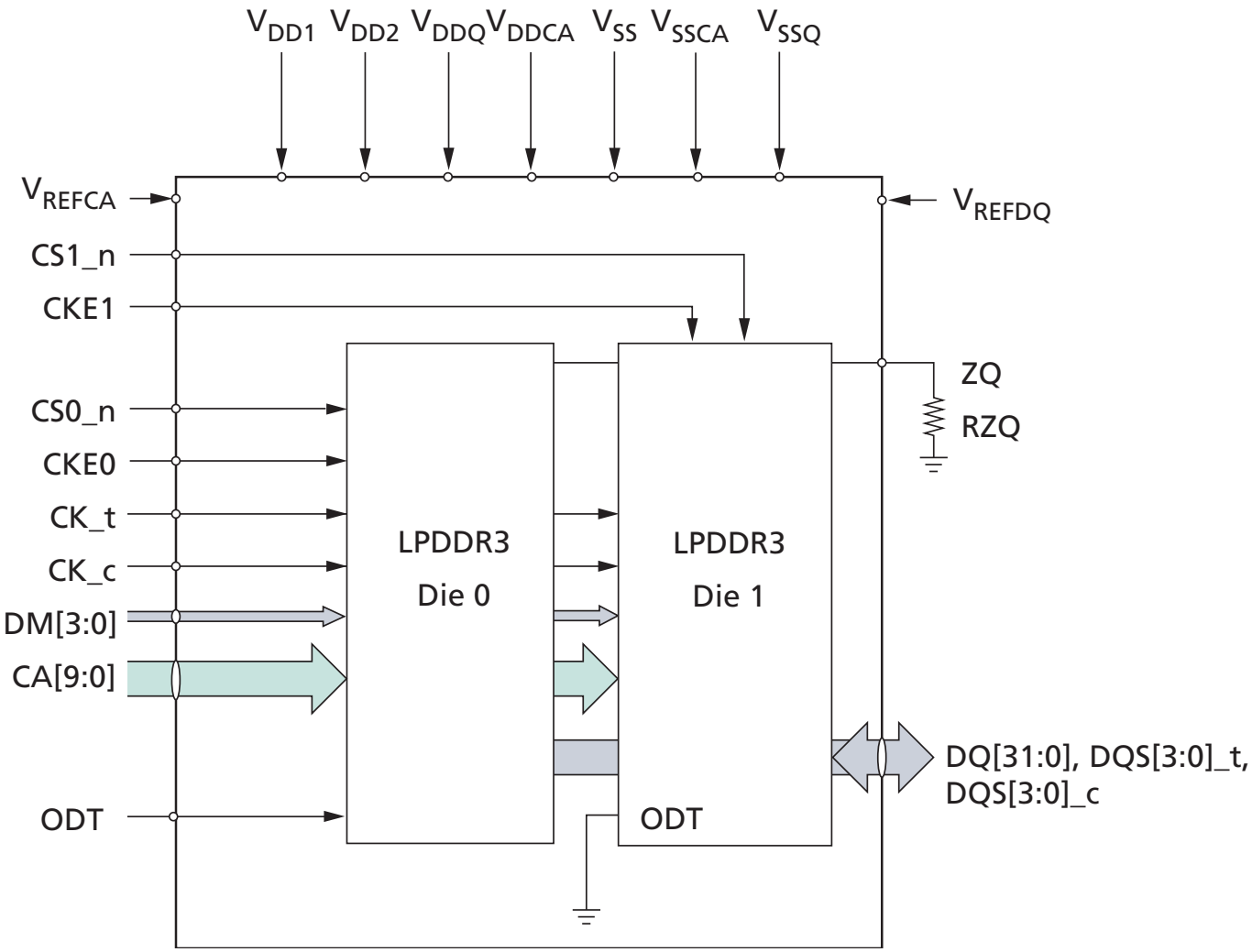


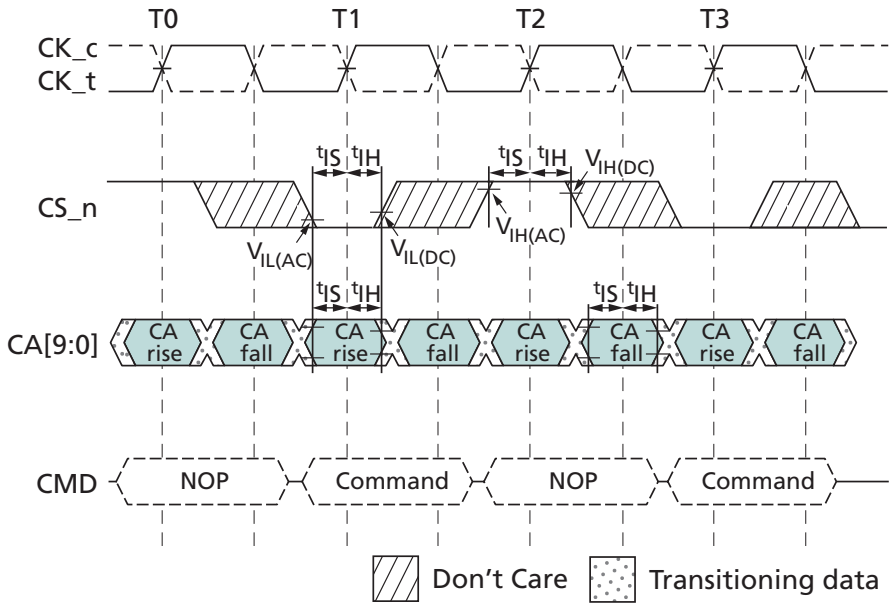
Table 3: Configuration Addressing – Single-Channel Package

Architecture		512 Meg x 32
Density per package		16Gb
Die per package		2
Ranks (CS_n) per channel		2
Die per rank	CS0_n	1
	CS1_n	1
Configuration per rank (CS_n)	CS0_n	32 Meg x 32 x 8 banks
	CS1_n	32 Meg x 32 x 8 banks
Row addressing		32K A[14:0]
Column addressing/CS_n	CS0_n	1KA[9:0]
	CS1_n	1KA[9:0]

Commands and Timing

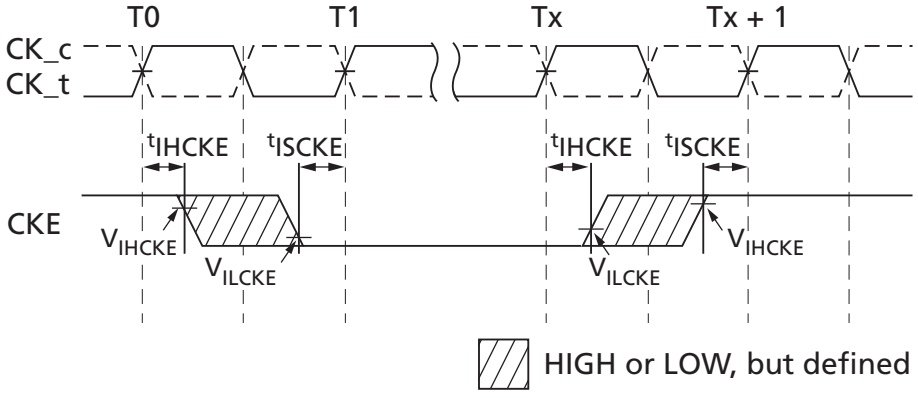
The setup and hold timings shown in the figures below apply for all commands.

Figure 5: Command and Input Setup and Hold



Note: 1. Setup and hold conditions also apply to the CKE pin. For timing diagrams related to the CKE pin, see the Power-Down section.

Figure 6: CKE Input Setup and Hold

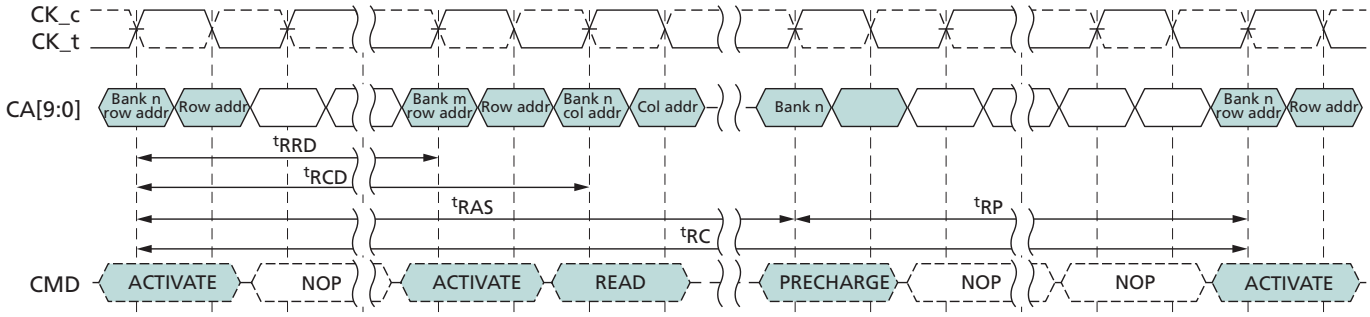


Notes: 1. After CKE is registered LOW, the CKE signal level is maintained below V_{ILCKE} for ^{t}CKE specification (LOW pulse width).
2. After CKE is registered HIGH, the CKE signal level is maintained above V_{IHCKE} for ^{t}CKE (HIGH pulse width).

ACTIVATE Command

The ACTIVATE command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA[2:0] are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at ^{t}RCD after the ACTIVATE command is issued. After a bank has been activated, it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as ^{t}RAS and ^{t}RP, respectively. The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (^{t}RC). The minimum time interval between ACTIVATE commands to different banks is ^{t}RRD.

Figure 7: ACTIVATE Command



Note: 1. A PRECHARGE ALL command uses ^{t}RPab timing, and a single-bank PRECHARGE command uses ^{t}RPpb timing. In this figure, ^{t}RP denotes either an all-bank PRECHARGE or a single-bank PRECHARGE.

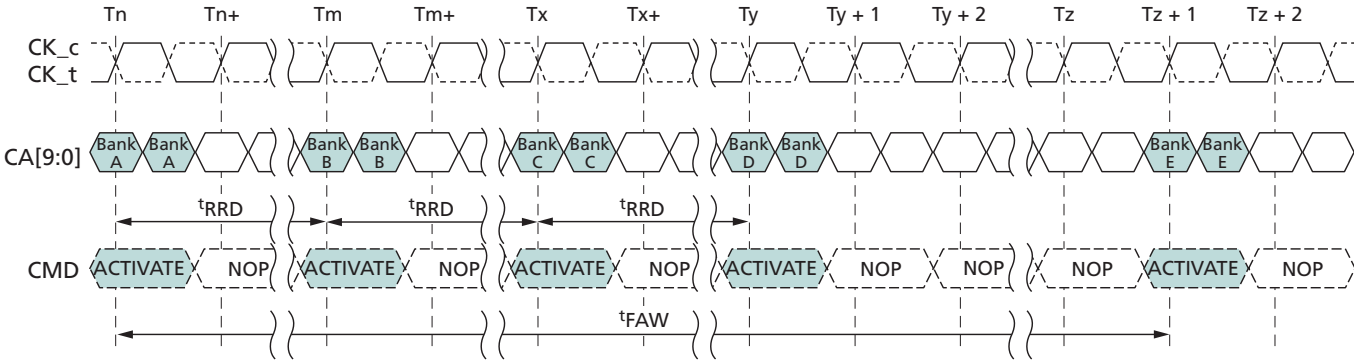
8-Bank Device Operation

Certain restrictions must be taken into consideration when operating 8-bank devices; one restricts the number of sequential ACTIVATE commands that can be issued and one provides additional RAS precharge time for a PRECHARGE ALL command.

The 8-Bank Device Sequential Bank Activation Restriction: No more than four banks can be activated (or refreshed, in the case of REFpb) in a rolling ^{t}FAW window. The number of clocks in a ^{t}FAW period depends on the clock frequency, which may vary. If the clock frequency is not changed over this period, convert to clocks by dividing ^{t}FAW[ns] by ^{t}CK[ns] and then rounding up to the next integer value. As an example of the rolling window, if RU(^{t}FAW/^{t}CK) is 10 clocks, and an ACTIVATE command is issued in clock *n*, no more than three further ACTIVATE commands can be issued at or between clock *n* + 1 and *n* + 9. REFpb also counts as bank activation for purposes of ^{t}FAW. If the clock is changed during the ^{t}FAW period, the rolling ^{t}FAW window may be calculated in clock cycles by adding together the time spent in each clock period. The ^{t}FAW requirement is met when the previous *n* clock cycles exceeds the ^{t}FAW time.

The 8-Bank Device PRECHARGE ALL Provision: ^{t}RP for a PRECHARGE ALL command must equal ^{t}RPab, which is greater than ^{t}RPpb.

Figure 8: ^{t}FAW Timing



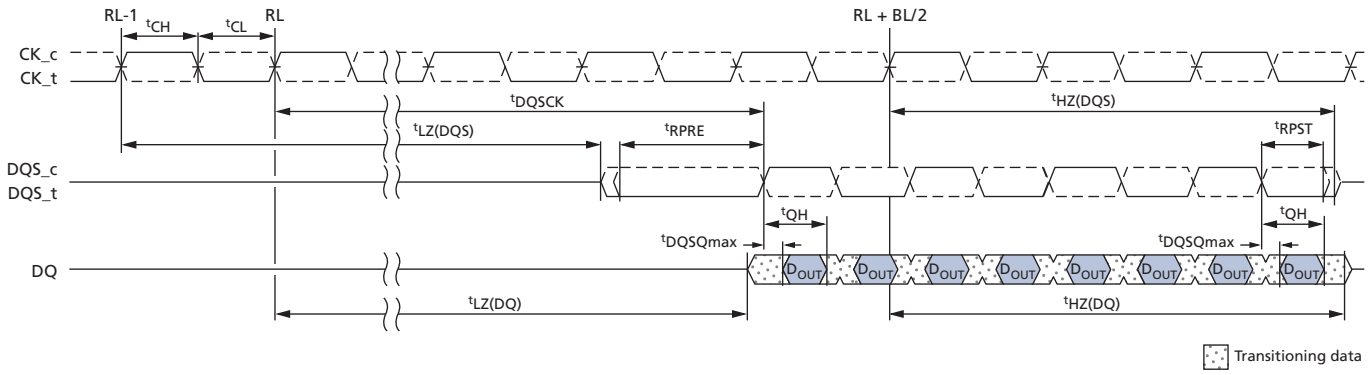
Read and Write Access Modes

After a bank is activated, a READ or WRITE command can be issued with CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW). A single READ or WRITE command initiates a burst READ or burst WRITE operation on successive clock cycles. Burst interrupts are not allowed.

Burst READ Command

The burst READ command is initiated with CS_n LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the ^{t}DQSCK delay is measured. The first valid data is available RL × ^{t}CK + ^{t}DQSCK + ^{t}DQSQ after the rising edge of the clock when the READ command is issued. The data strobe output is driven LOW ^{t}RPRE before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers. Pin input timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

Figure 9: READ Output Timing



Note: 1. ^{t}DQSCK can span multiple clock periods.

Figure 10: Burst READ – RL = 12, BL = 8, ^{t}DQSCK > ^{t}CK

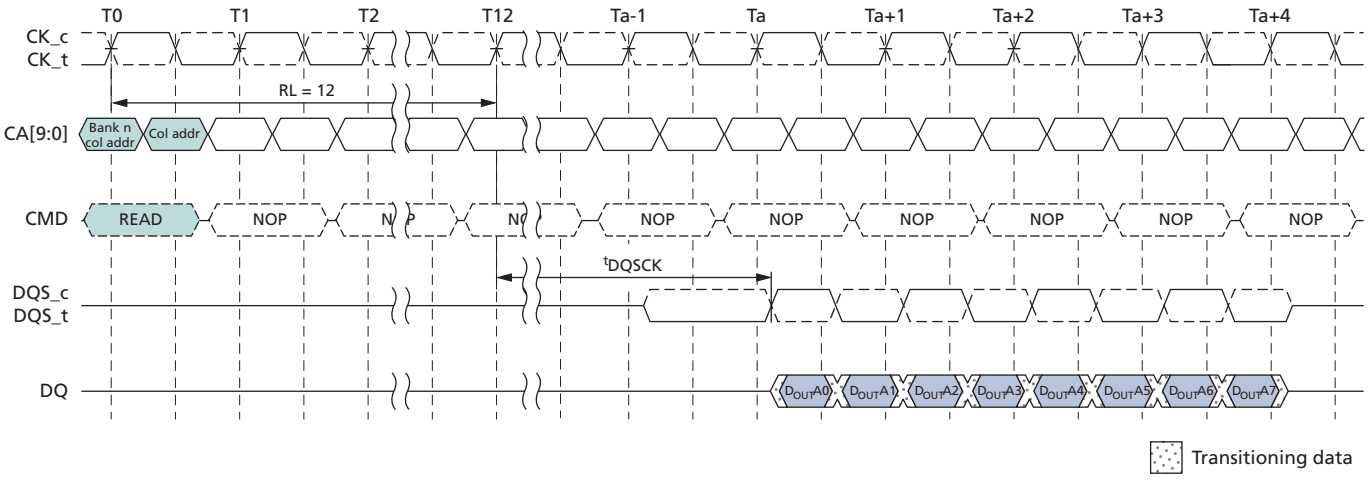


Figure 11: Burst READ – RL = 12, BL = 8, ^{t}DQSCK < ^{t}CK

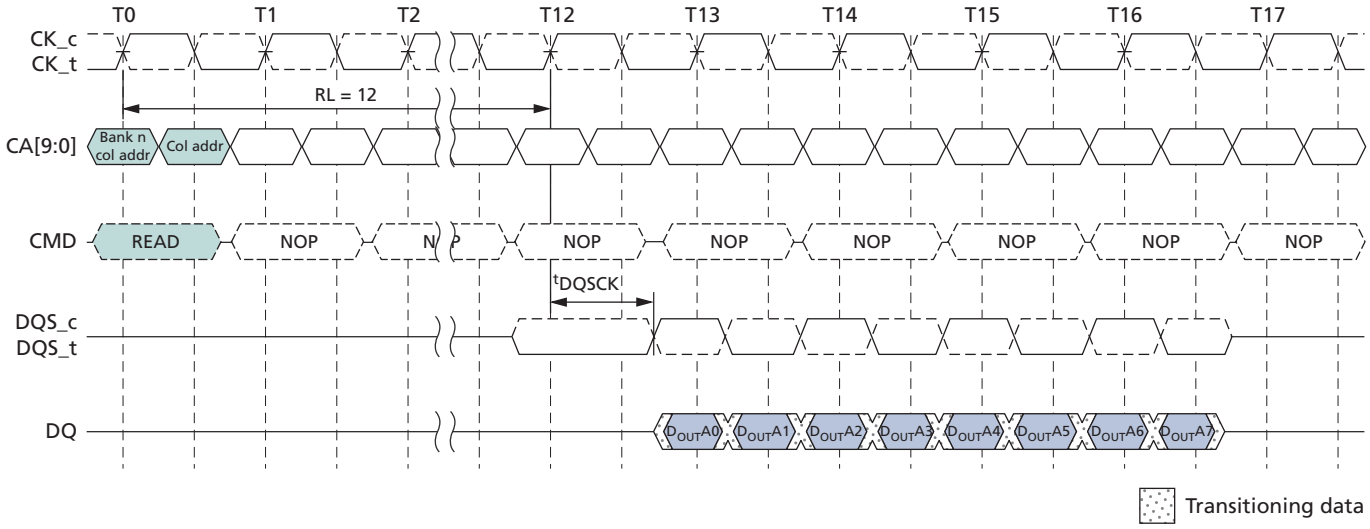
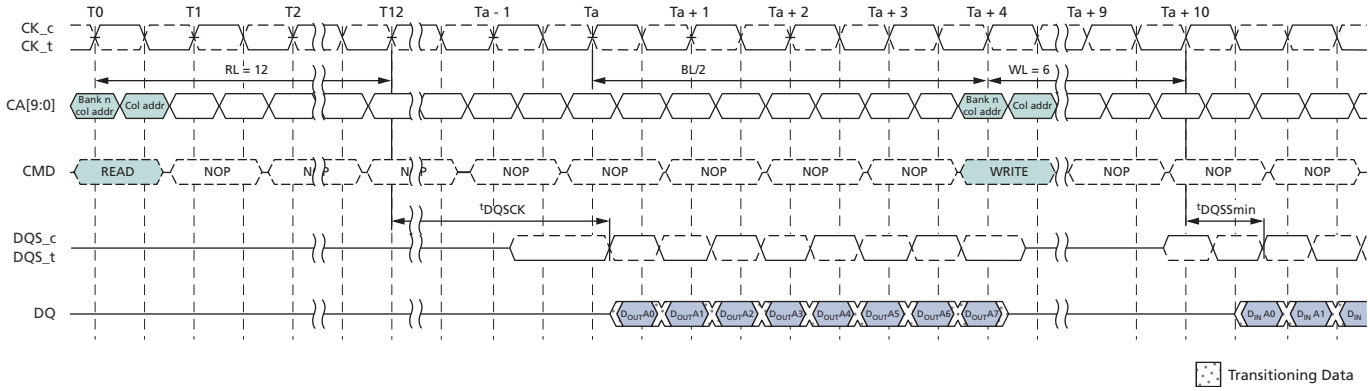
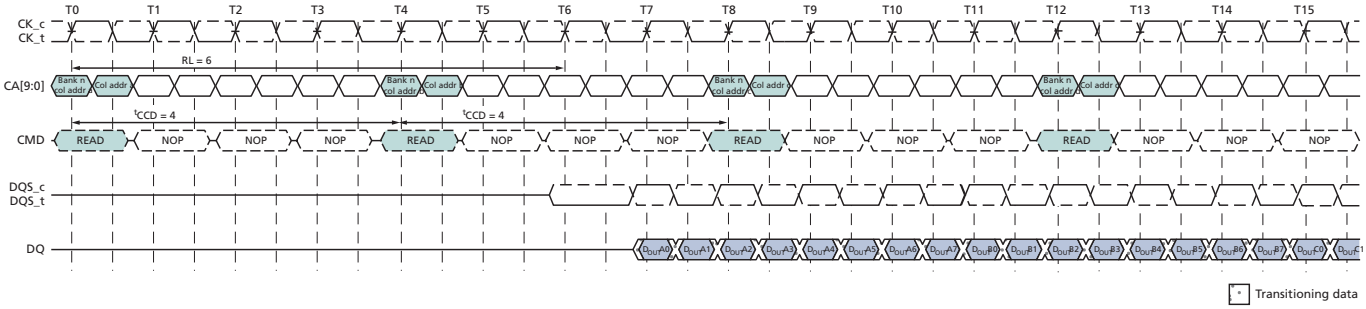


Figure 12: Burst READ Followed by Burst WRITE – RL = 12, WL = 6, BL = 8



The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + 1 - WL clock cycles.

Figure 13: Seamless Burst READ – RL = 6, BL = 8, ^{t}CCD = 4

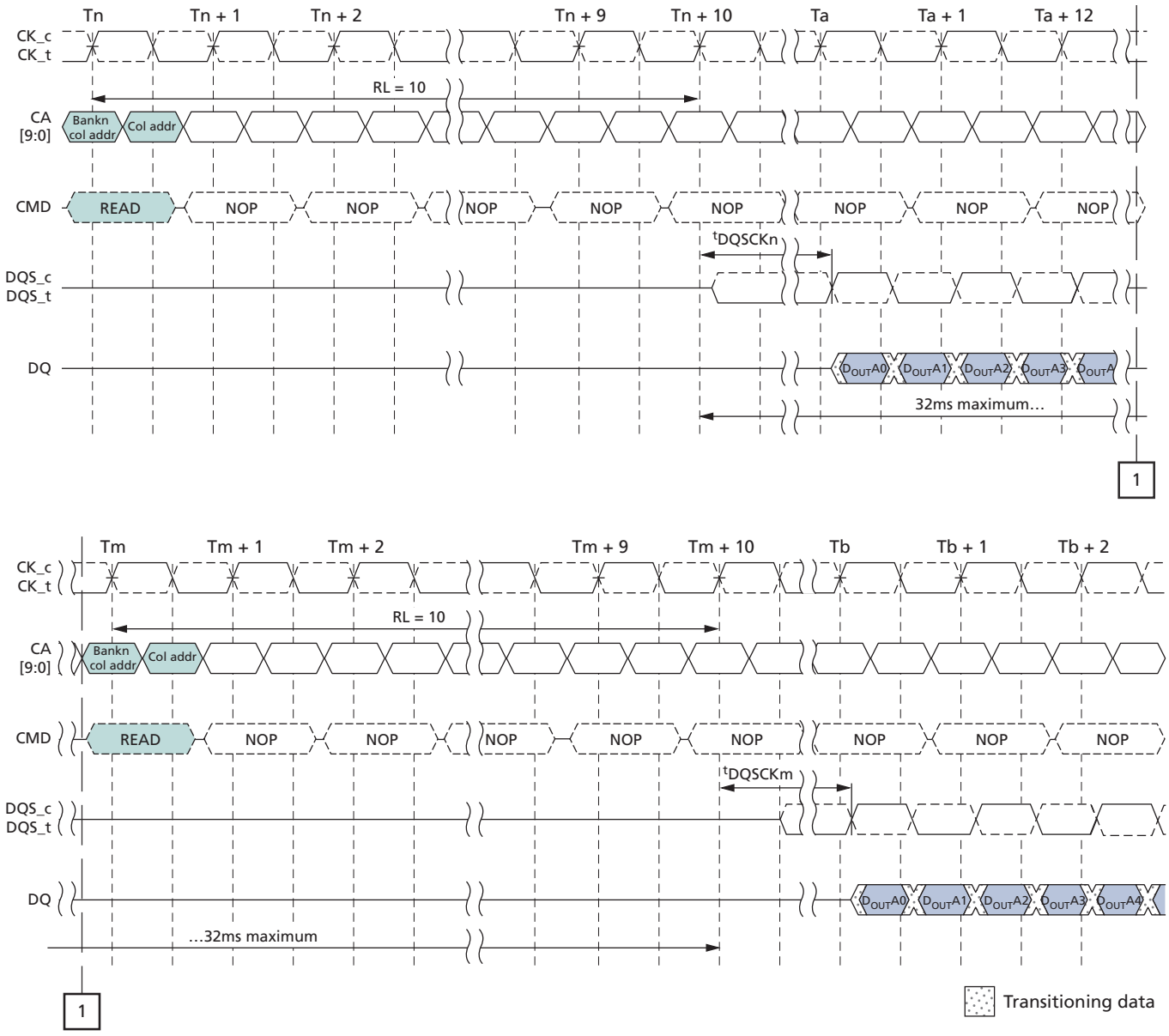


The seamless burst READ operation is supported by enabling a READ command at every fourth clock cycle for BL = 8 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

^{t}DQSCK Delta Timing

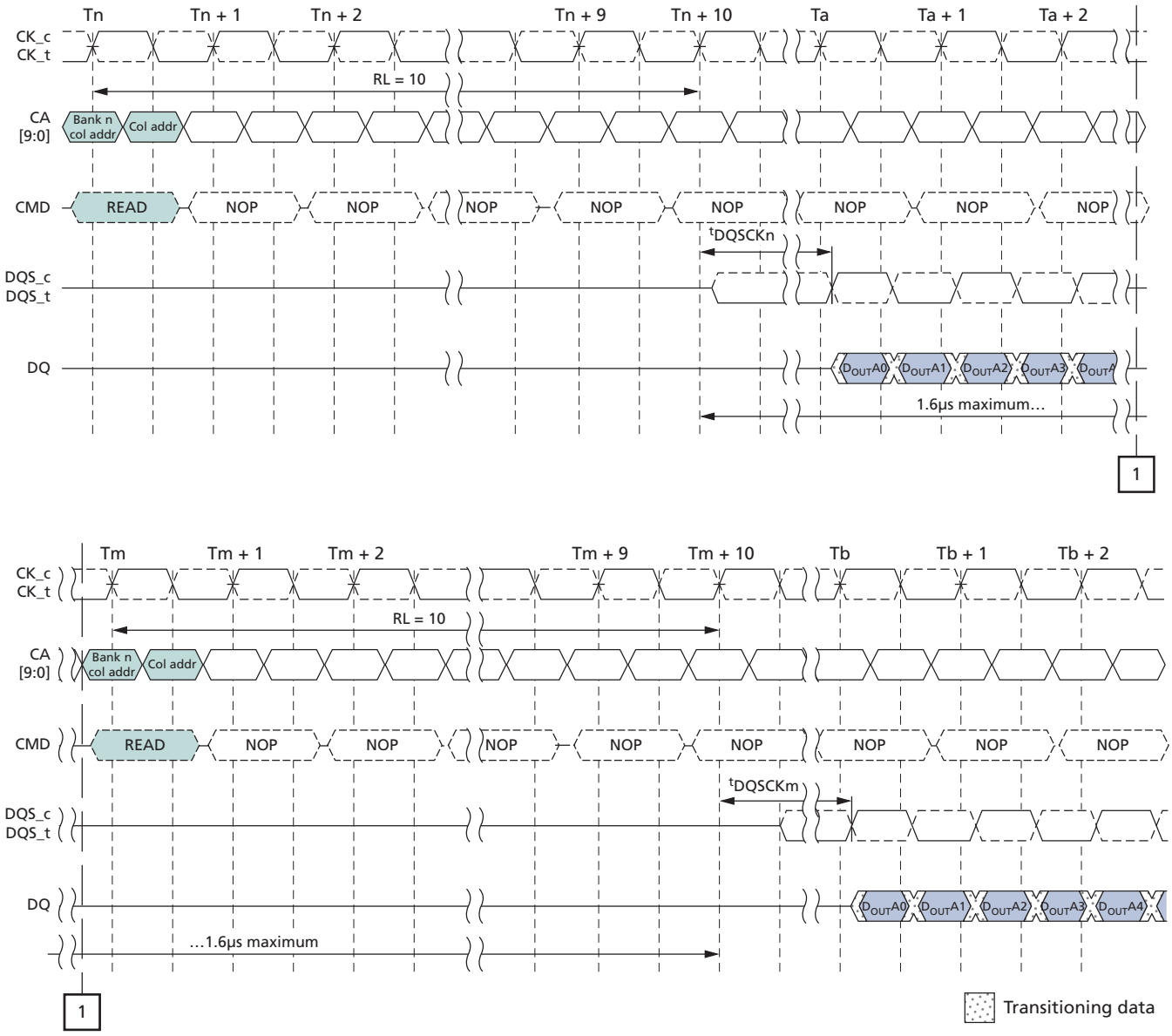
To allow the system to track variations in ^{t}DQSCK output across multiple clock cycles, three parameters are provided: ^{t}DQSCKDL (delta long), ^{t}DQSCKDM (delta medium), and ^{t}DQSCKDS (delta short). Each of these parameters defines the change in ^{t}DQSCK over a short, medium, or long rolling window, respectively. The definition for each ^{t}DQSCK-delta parameter is shown in the figures below.

Figure 14: ^{t}DQSCKDL Timing



Notes:
1. ^{t}DQSCKDL = (^{t}DQSCK*n* - ^{t}DQSCK*m*).
2. ^{t}DQSCKDL (MAX) is defined as the maximum of ABS (^{t}DQSCK*n* - ^{t}DQSCK*m*) for any (^{t}DQSCK*n*, ^{t}DQSCK*m*) pair within any 32ms rolling window.

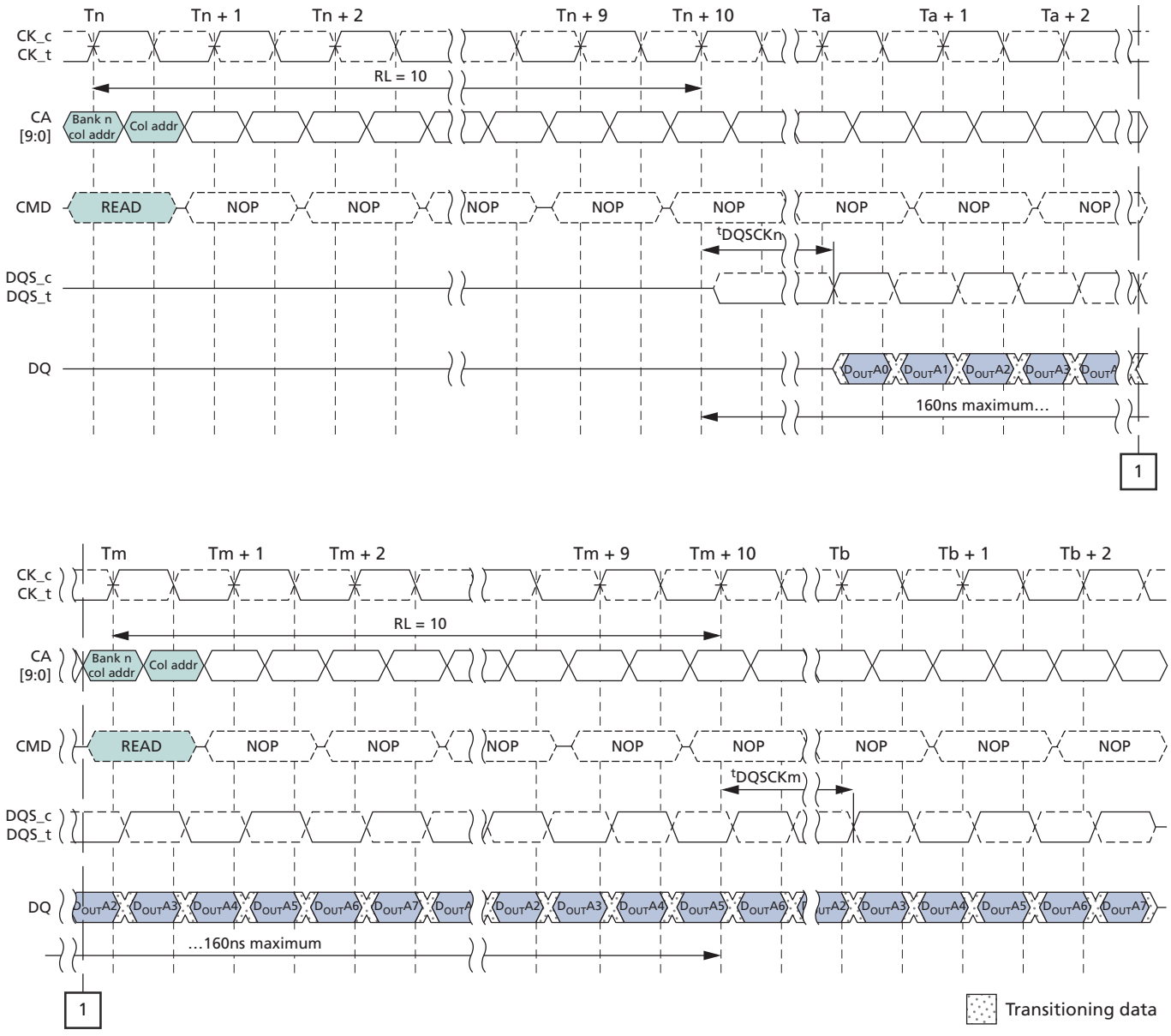
Figure 15: ^{t}DQSCKDM Timing



Notes: 1. ^{t}DQSCKDM = (^{t}DQSCK*n* - ^{t}DQSCK*m*).

2. ^{t}DQSCKDM (MAX) is defined as the maximum of ABS (^{t}DQSCK*n* - ^{t}DQSCK*m*) for any (^{t}DQSCK*n*, ^{t}DQSCK*m*) pair within any 1.6µs rolling window.

Figure 16: ^{t}DQSCKDS Timing



Notes:
1. ^{t}DQSCKDS = (^{t}DQSCK*n* - ^{t}DQSCK*m*).
2. ^{t}DQSCKDS (MAX) is defined as the maximum of ABS (^{t}DQSCK*n* - ^{t}DQSCK*m*) for any (^{t}DQSCK*n*, ^{t}DQSCK*m*) pair for READs within a consecutive burst, within any 160ns rolling window.

Burst WRITE Command

The burst WRITE command is initiated with CS_n LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the ^{t}DQSS delay is measured. The first valid data must be driven WL × ^{t}CK + ^{t}DQSS from the rising edge of the clock from which the WRITE command is issued. The data strobe signals (DQS) must be driven as shown in Figure 25 (page 56). The burst cycle data bits must be applied to the DQ pins ^{t}DS prior to the associated edge of the DQS and held valid until ^{t}DH after that edge. Burst data is sampled on successive edges of the DQS_t until the burst length is completed. After a burst WRITE operation, ^{t}WR must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

Figure 17: Data Input (WRITE) Timing

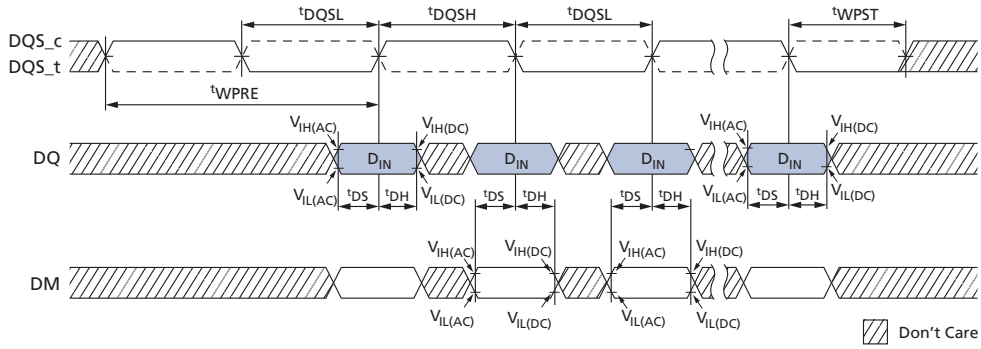


Figure 18: Burst WRITE

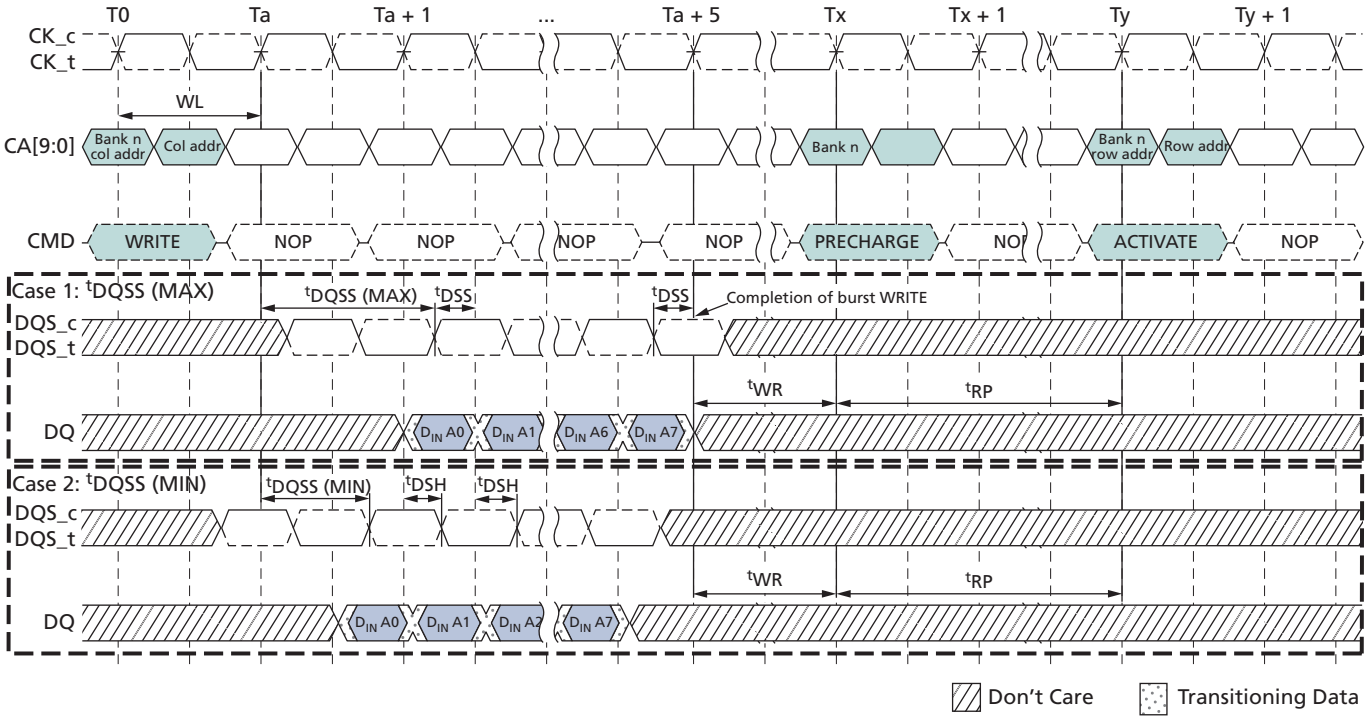


Figure 19: Method for Calculating tWPRE Transitions and Endpoints

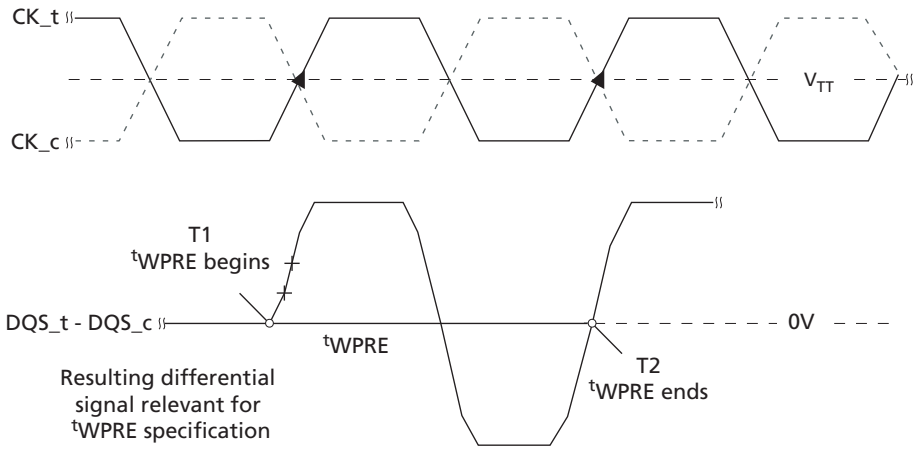


Figure 20: Method for Calculating ^{t}WPST Transitions and Endpoints

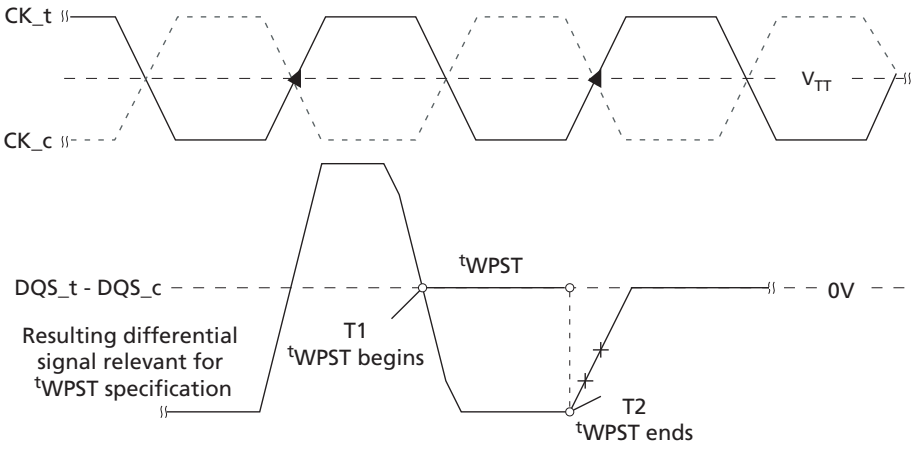
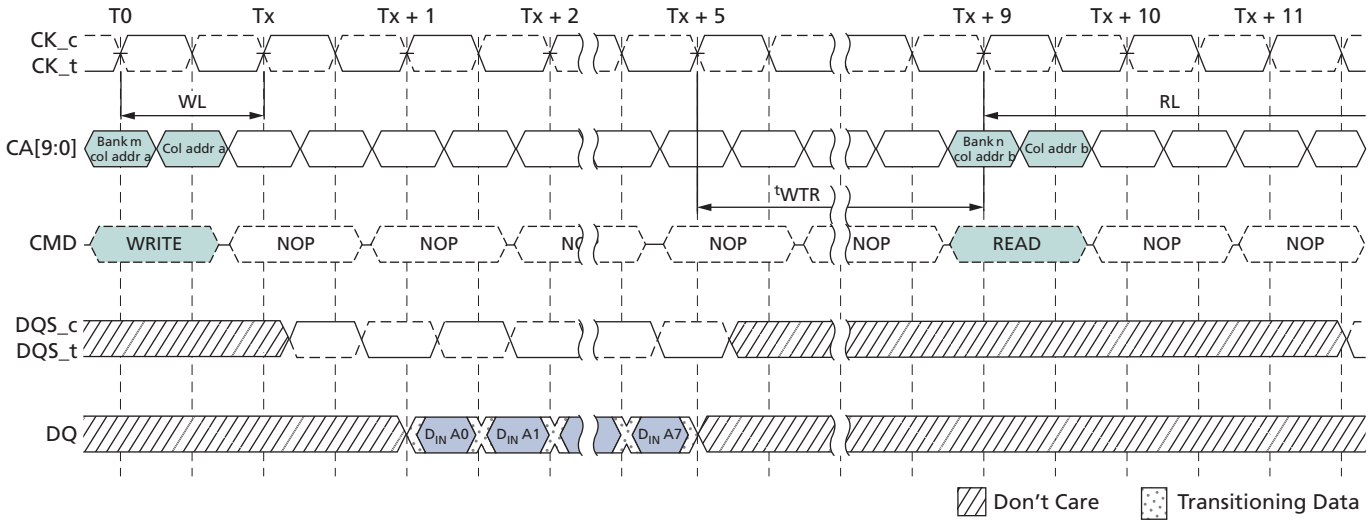
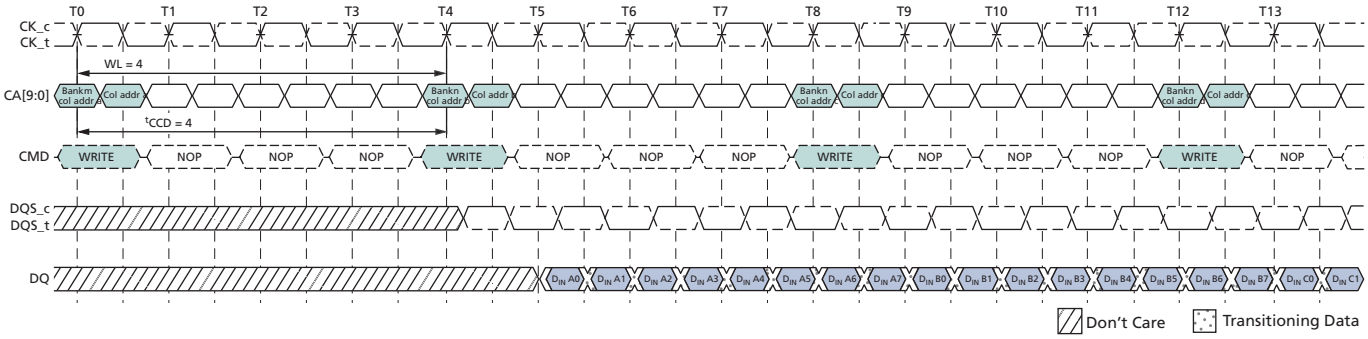


Figure 21: Burst WRITE Followed by Burst READ



Notes:
1. The minimum number of clock cycles from the burst WRITE command to the burst READ command for any bank is [WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)].
2. ^{t}WTR starts at the rising edge of the clock after the last valid input data.

Figure 22: Seamless Burst WRITE – WL = 4, BL = 8, ^{t}CCD = 4



Note: 1. The seamless burst WRITE operation is supported by enabling a WRITE command every four clocks for BL = 8 operation. This operation is supported for any activated bank.

Write Data Mask

LPDDR3 devices support one write data mask (DM) pin for each data byte (DQ), which is consistent with LPDDR2 devices. Each DM can mask its respective DQ for any given cycle of the burst. Data mask timings match data bit timing, but are inputs only. Internal data mask loading is identical to data bit loading to ensure matched system timing.

Figure 23: Data Mask Timing

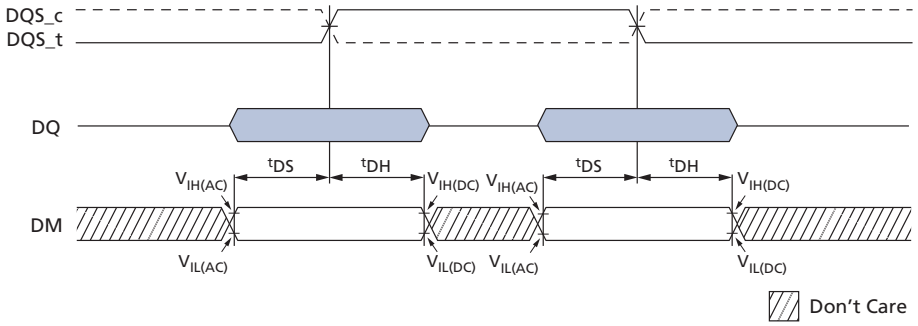
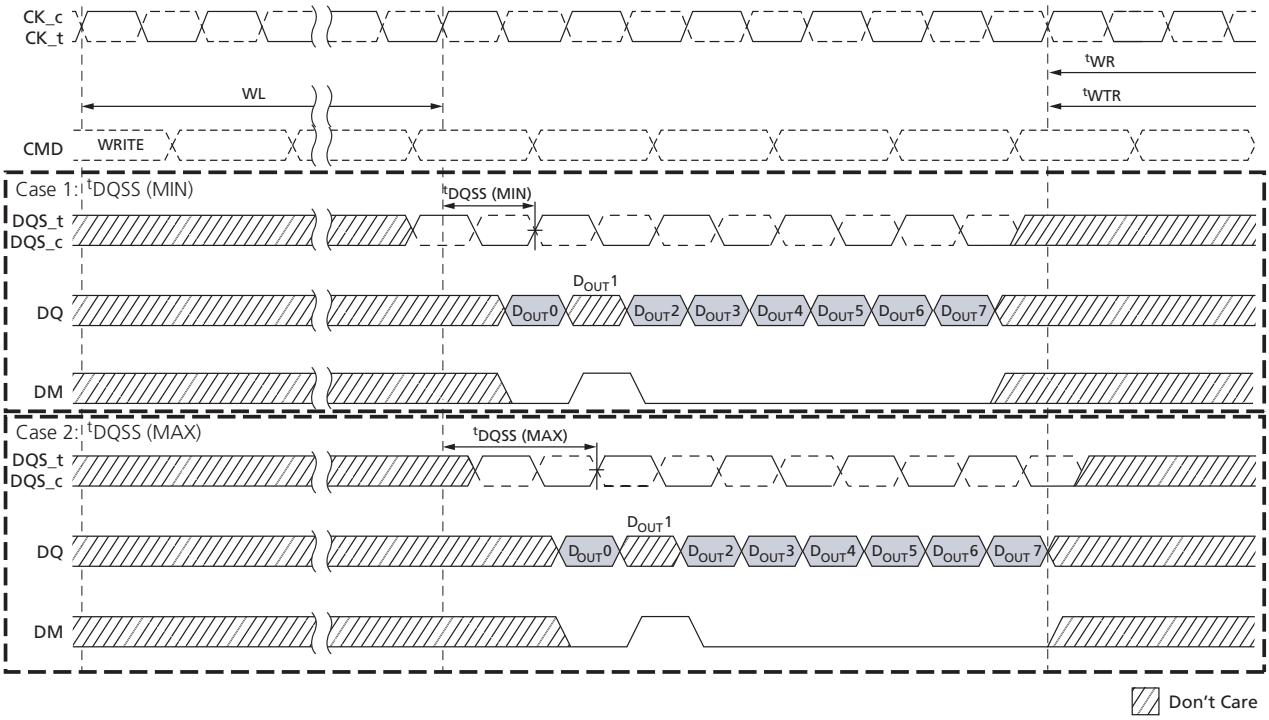


Figure 24: Write Data Mask – Second Data Bit Masked



PRECHARGE Command

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bits BA0, BA1, and BA2 are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access ^{t}RPab after an all-bank PRECHARGE command is issued, or ^{t}RPpb after a single-bank PRECHARGE command is issued.

To ensure that LPDDR3 devices can meet the instantaneous current demand required to operate, the row precharge time (^{t}RP) for an all bank PRECHARGE (^{t}RPab) will be longer than the row precharge time for a single-bank PRECHARGE (^{t}RPpb). ACTIVATE to PRECHARGE timing is shown in the ACTIVATE Command figure.

Table 4: Bank Selection for PRECHARGE by Address Bits

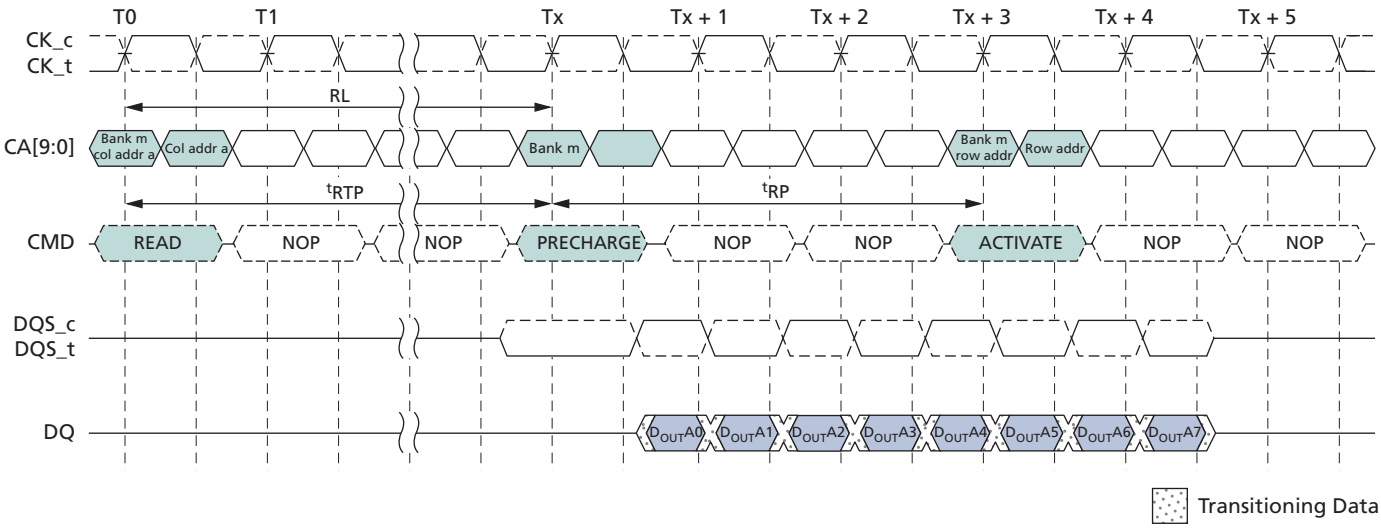
AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 8-Bank Device
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	Don’t Care	Don’t Care	Don’t Care	All banks

Burst READ Operation Followed by PRECHARGE

For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clock cycles after a READ command. A new bank ACTIVATE command can be issued to the same bank after the row precharge time (^{t}RP) has elapsed. A PRECHARGE command cannot be issued until after ^{t}RAS is satisfied.

For LPDDR3 devices, the minimum READ-to-PRECHARGE time (^{t}RTP) must also satisfy a minimum analog time from the rising clock edge that initiates the last 8-bit prefetch of a READ command. ^{t}RTP begins BL/2 - 4 clock cycles after the READ command. For LPDDR3 READ-to-PRECHARGE timings, see the PRECHARGE and Auto Precharge Clarification table.

Figure 25: Burst READ Followed by PRECHARGE – BL = 8, RU(^{t}RTP(MIN)/^{t}CK) = 2



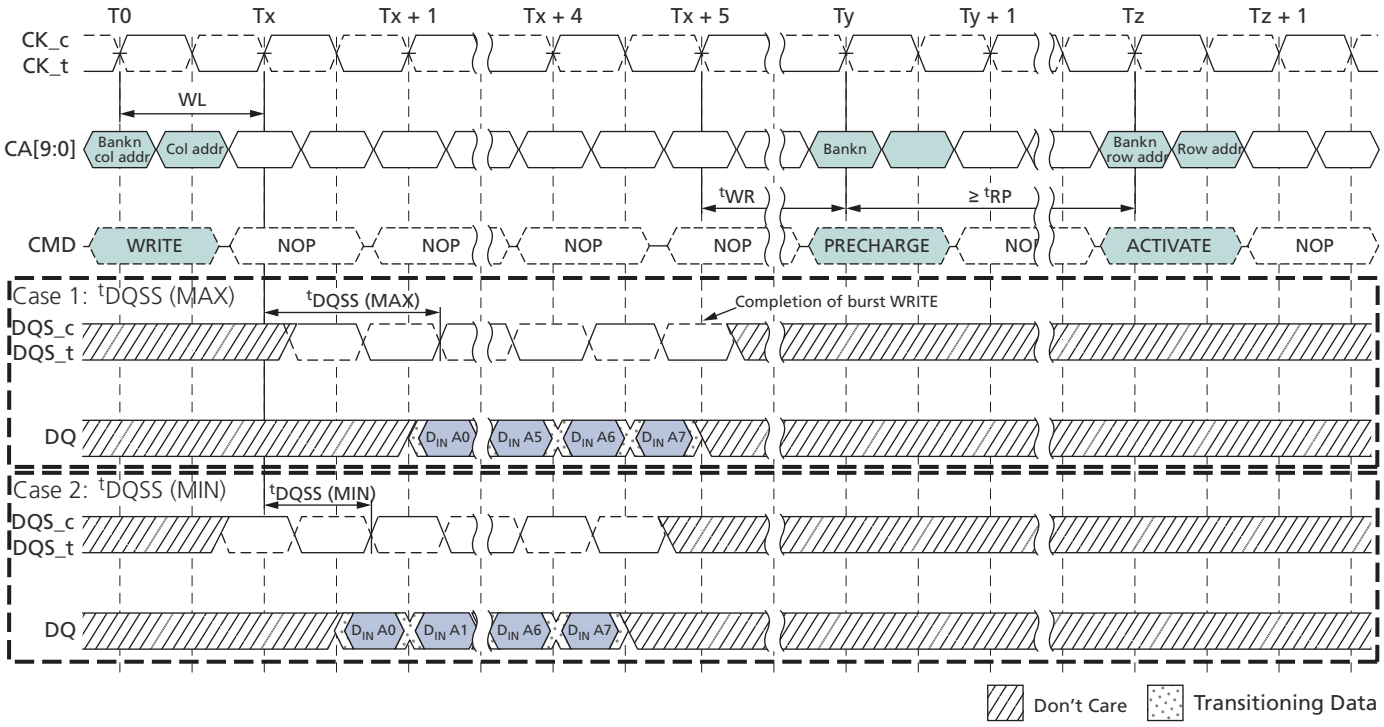
Burst WRITE Followed by PRECHARGE

For WRITE cycles, a WRITE recovery time (^{t}WR) must be provided before a PRECHARGE command can be issued. This delay is referenced from the last valid burst input data to the completion of the burst WRITE. The PRECHARGE command must not be issued prior to the ^{t}WR delay. For LPDDR3 WRITE-to-PRECHARGE timings, see the PRECHARGE and Auto Precharge Clarification table.

LPDDR3 devices write data to the array in prefetch multiples (prefetch = 8). An internal WRITE operation can begin only after a prefetch group has been completely latched, so ^{t}WR starts at prefetch bondaries.

The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(^{t}WR/^{t}CK) clock cycles.

Figure 26: Burst WRITE Followed by PRECHARGE – BL = 8



Auto Precharge

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge function. When a READ or WRITE command is issued to the device, the AP bit (CA0f) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, a normal READ or WRITE burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

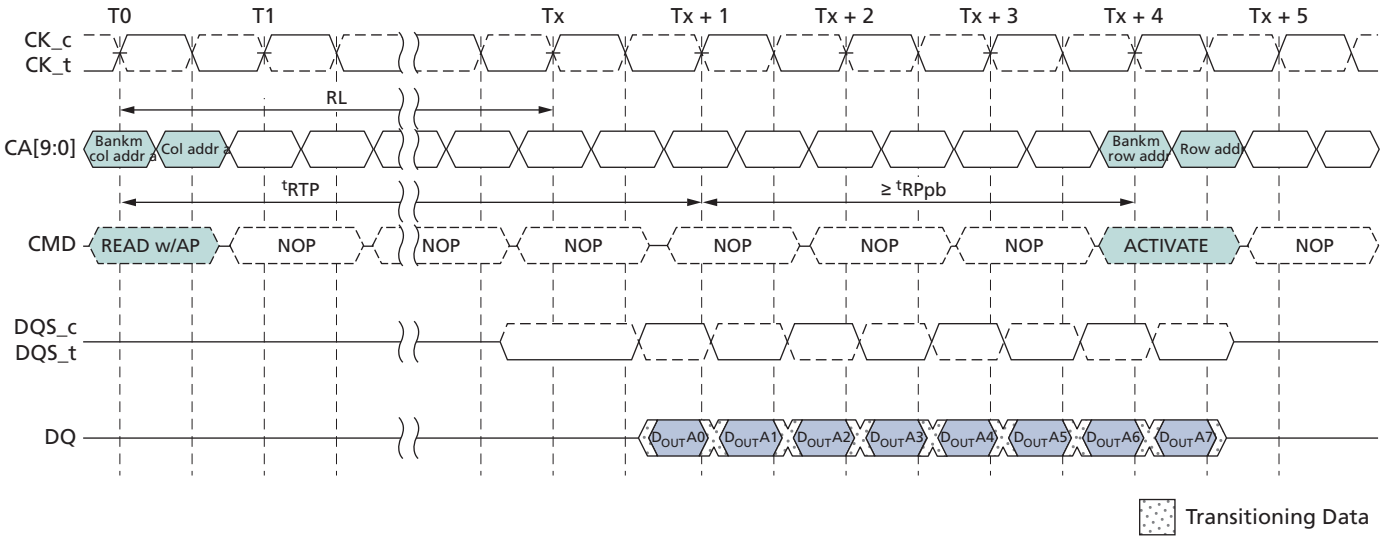
Burst READ with Auto Precharge

If AP (CA0f) is HIGH when a READ command is issued, the READ with auto precharge function is engaged. The device starts an auto precharge on the rising edge of the clock, BL/2 or BL/2 - 4 + RU(^{t}RTP/^{t}CK) clock cycles later than the READ with auto precharge command, whichever is greater. For LPDDR3 auto precharge calculations, see the PRECHARGE and Auto Precharge Clarification table.

Following an auto precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:

- The RAS precharge time (^{t}RP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (^{t}RC) from the previous bank activation has been satisfied.

Figure 27: LPDDR3 – Burst READ with Auto Precharge



Burst WRITE with Auto Precharge

If AP (CA0f) is HIGH when a WRITE command is issued, the WRITE with auto precharge function is engaged. The device starts an auto precharge at the clock rising edge ^{t}WR cycles after the completion of the burst WRITE.

Following a WRITE with auto precharge, an ACTIVATE command can be issued to the same bank if the following two conditions are met:

- The RAS precharge time (^{t}RP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (^{t}RC) from the previous bank activation has been satisfied.

Figure 28: Burst WRITE with Auto Precharge – BL = 8

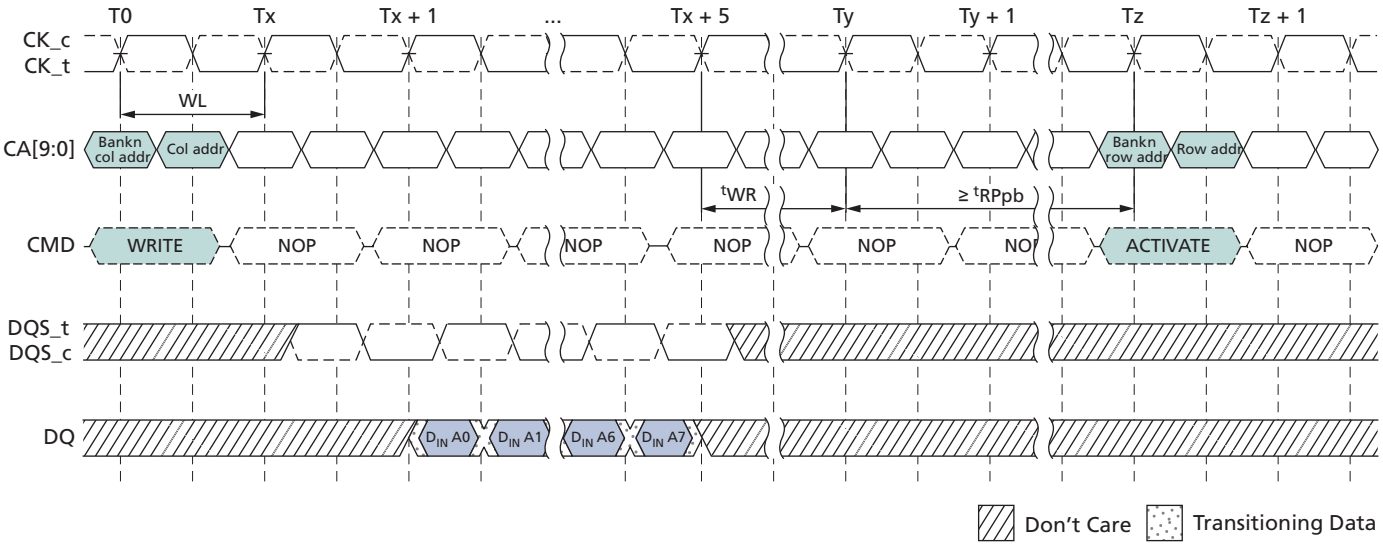


Table 5: PRECHARGE and Auto Precharge Clarification

From Command	To Command	Minimum Delay Between Commands	Unit	Notes
READ	PRECHARGE to same bank as READ	BL/2 + MAX (4, RU(^{t}RTP/^{t}CK)) - 4	CLK	1
	PRECHARGE ALL	BL/2 + MAX (4, RU(^{t}RTP/^{t}CK)) - 4		1
READ w/AP	PRECHARGE to same bank as READ w/AP	BL/2 + MAX (4, RU(^{t}RTP/^{t}CK)) - 4	CLK	1, 2
	PRECHARGE ALL	BL/2 + MAX(4, RU(^{t}RTP/^{t}CK)) - 4		1
	ACTIVATE to same bank as READ w/AP	BL/2 + MAX(4, RU(^{t}RTP/^{t}CK)) - 4 + RU(^{t}RPpb/^{t}CK)		1
	WRITE or WRITE w/AP (same bank)	Illegal		3
	WRITE or WRITE w/AP (different bank)	RL + BL/2 + RU(^{t}DQSCKmax/^{t}CK) - WL + 1		3
	READ or READ w/AP (same bank)	Illegal		3
	READ or READ w/AP (different bank)	BL/2		3
WRITE	PRECHARGE to same bank as WRITE	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	CLK	1
	PRECHARGE ALL	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1		1
WRITE w/AP	PRECHARGE to same bank as WRITE w/AP	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	CLK	1
	PRECHARGE ALL	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1		1
	ACTIVATE to same bank as WRITE w/AP	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1 + RU(^{t}RPpb/^{t}CK)		1
	WRITE or WRITE w/AP (same bank)	Illegal		3
	WRITE or WRITE w/AP (different bank)	BL/2		3
	READ or READ w/AP (same bank)	Illegal		3
	READ or READ w/AP (different bank)	WL + BL/2 + RU(^{t}WTR/^{t}CK) + 1		3
PRECHARGE	PRECHARGE to same bank as PRECHARGE	1	CLK	1
	PRECHARGE ALL	1		1
PRECHARGE ALL	PRECHARGE	1	CLK	1
	PRECHARGE ALL	1		1

Notes:
1. For a given bank, the PRECHARGE period should be counted from the latest PRECHARGE command, which will be either a one-bank PRECHARGE command or a PRECHARGE ALL command, issued to that bank. The PRECHARGE period is satisfied after ^{t}RP, depending on the latest PRECHARGE command issued to that bank.
2. Any command issued during the specified minimum delay time is illegal.
3. After a READ with auto precharge command, seamless READ operations to different banks are supported. After a WRITE with auto precharge command, seamless WRITE operations to different banks are supported. READ with auto precharge and WRITE with auto precharge commands must not be interrupted or truncated.

REFRESH Command

The REFRESH command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. Per-bank REFRESH is initiated with CA3 LOW at the rising edge of the clock. All-bank REFRESH is initiated with CA3 HIGH at the rising edge of the clock.

A per-bank REFRESH command (REFpb) performs a per-bank REFRESH operation to the bank scheduled by the bank counter in the memory device. The bank sequence for per-bank REFRESH is fixed to be a sequential round-robin: 0-1-2-3-4-5-6-7-0-1-.... The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh.

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions have been met (see the REFRESH Command Scheduling Separation Requirements table):

- ^{t}RFCab has been satisfied after the prior REFab command
- ^{t}RFCpb has been satisfied after the prior REFpb command
- ^{t}RP has been satisfied after the prior PRECHARGE command to that bank
- ^{t}RRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command)

The target bank is inaccessible during per-bank REFRESH cycle time (^{t}RFCpb); however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, the following conditions must be met (see the REFRESH Command Scheduling Separation Requirements table):

- ^{t}RFCpb must be satisfied before issuing a REFab command
- ^{t}RFCpb must be satisfied before issuing an ACTIVATE command to the same bank
- ^{t}RRD must be satisfied before issuing an ACTIVATE command to a different bank
- ^{t}RFCpb must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE ALL command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met (see the REFRESH Command Scheduling Separation Requirements table):

- ^{t}RFCab has been satisfied following the prior REFab command
- ^{t}RFCpb has been satisfied following the prior REFpb command
- ^{t}RP has been satisfied following the prior PRECHARGE commands

When an all-bank REFRESH cycle has completed, all banks will be idle. After issuing REFab:

- ^{t}RFCab latency must be satisfied before issuing an ACTIVATE command
- ^{t}RFCab latency must be satisfied before issuing a REFab or REFpb command

Table 6: REFRESH Command Scheduling Separation Requirements

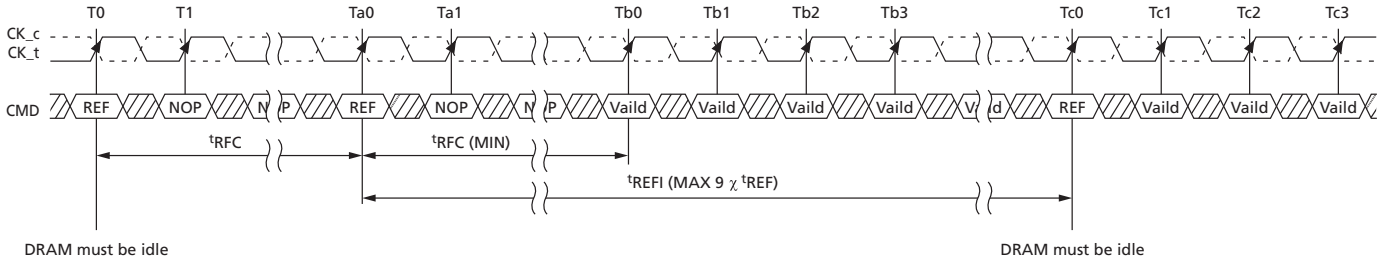
Symbol	Minimum Delay From	To	Notes
^{t}RFCab	REFab	REFab	
		ACTIVATE command to any bank	
		REFpb	
^{t}RFCpb	REFpb	REFab	
		ACTIVATE command to same bank as REFpb	
		REFpb	
^{t}RRD	REFpb	ACTIVATE command to a different bank than REFpb	
	ACTIVATE	REFpb	1
		ACTIVATE command to a different bank than the prior ACTIVATE command	

Note: 1. A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited. REFpb is supported only if it affects a bank that is in the idle state.

In general, an all bank REFRESH command needs to be issued to the device regularly every ^{t}REFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling in the refresh command. A maximum of eight REFRESH commands can be postponed during operation of the device, but at no point in time are more than a total of eight REFRESH commands allowed to be postponed. In the case where eight REFRESH commands are postponed in a row, the resulting maximum interval between the surrounding REFRESH commands is limited to 9 × ^{t}REFI. A maximum of eight additional REFRESH commands can be issued in advance (pulled in), with each one reducing the number of regular REFRESH commands required later by one. Note that pulling in more than eight REFRESH commands in advance does not reduce the number of regular REFRESH commands required later; therefore, the resulting maximum interval between two surrounding REFRESH commands is limited to 9 x ^{t}REFI. At any given time, a maximum of 16 REFRESH commands can be issued within 2 x ^{t}REFI.

For per bank refresh, a maximum of 8 × 8 per bank REFRESH commands can be postponed or pulled in for scheduling efficiency. At any given time, a maximum of 2 × 8 per bank REFRESH commands may be issued within 2 × ^{t}REFI.

Figure 29: REFRESH Command Timing



Notes:
1. Only NOP commands are allowed after the REFRESH command is registered until ^{t}RFC (MIN) expires.
2. The time interval between two REFRESH commands may be extended to a maximum of 9 ×^{t}REFI.

Figure 30: Postponing REFRESH Commands

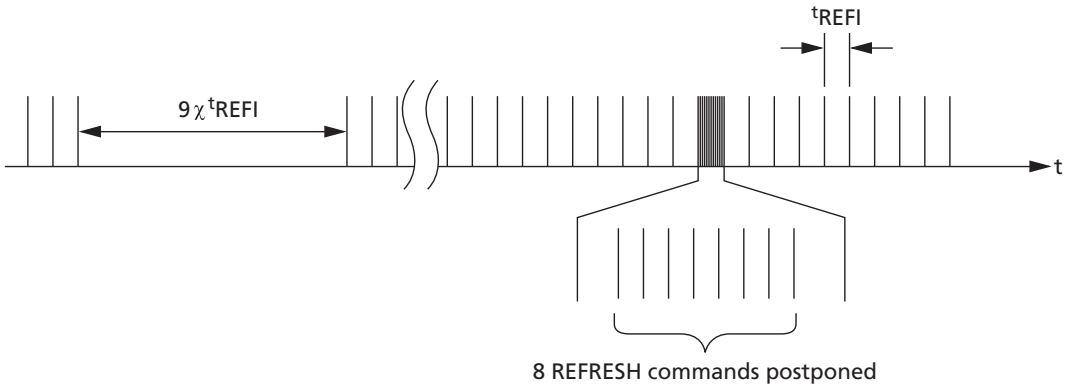
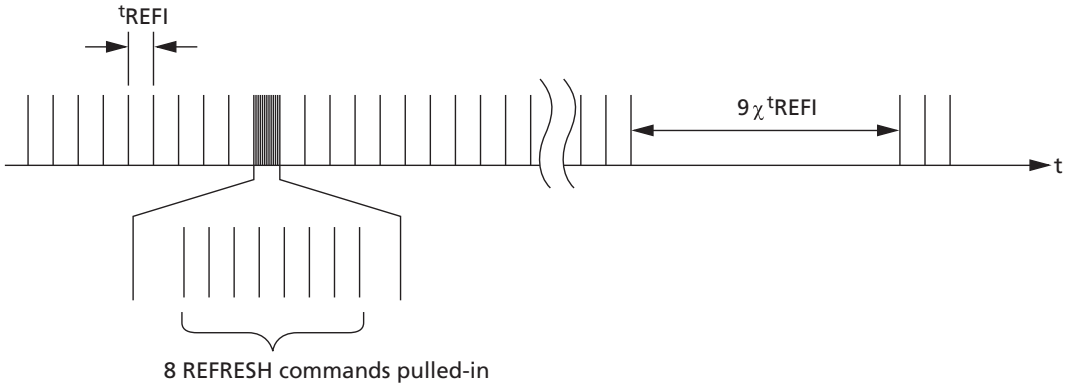


Figure 31: Pulling In REFRESH Commands



REFRESH Requirements

Minimum REFRESH Commands

LPDDR3 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window (^{t}REFW = 32ms @ MR4[2:0] = 011 or $T_C \leq 85^{\circ}C$). For actual values per density and the resulting average refresh interval (^{t}REFI), see the Refresh Requirement Parameters (Per Density) table.

For ^{t}REFW and ^{t}REFI refresh multipliers at different MR4 settings, see the MR4 Device Temperature (MA[7:0] = 04h) and the MR4 Op-Code Bit Definitions tables.

When using per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

REFRESH Requirements and Self Refresh

Self refresh mode may be entered with a maximum of eight REFRESH commands being postponed. After exiting self refresh mode with one or more REFRESH commands postponed, additional REFRESH commands may be postponed, but the total number of postponed refresh commands (before and after the self refresh) must never exceed eight. During self refresh mode, the number of postponed or pulled-in REFRESH commands does not change.

An internally timed refresh event can be missed when CKE is raised for exit from self refresh mode. After exiting self refresh, the device requires a minimum of one extra REFRESH command before it is put back into self refresh mode.

Figure 32: All-Bank REFRESH Operation

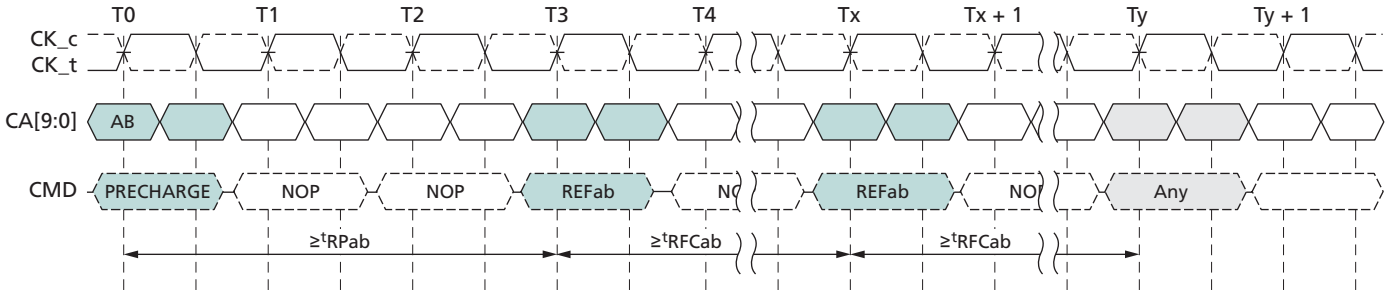
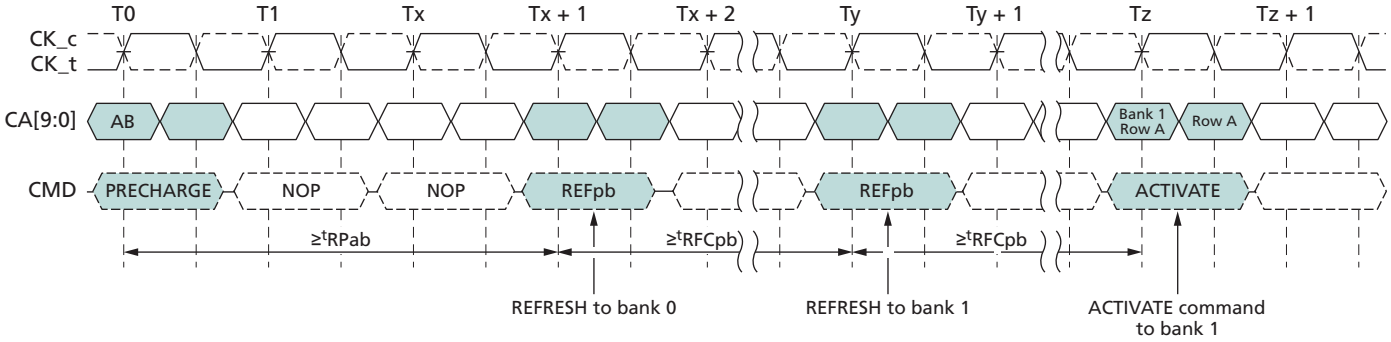


Figure 33: Per-Bank REFRESH Operation



Notes:
1. In the beginning of this example, the REFpb bank counter points to bank 0.
2. Operations to banks other than the bank being refreshed are supported during the ^{t}RFCpb period.

SELF REFRESH Operation

The SELF REFRESH command can be used to retain data in the array, even if the rest of the system is powered-down. When in the self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate SELF REFRESH operation. The SELF REFRESH command is executed by taking CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the clock cycle preceding a SELF REFRESH command. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress.

To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW; this timing period is defined as ^{t}CPDED. CKE LOW will result in deactivation of input receivers after ^{t}CPDED has expired. After the power-down command is registered, CKE must be held LOW to keep the device in self refresh mode.

Mobile LPDDR3 devices can operate in self refresh mode in both the standard and extended temperature ranges. These devices also manage self refresh power consumption when the operating temperature changes, resulting in the lowest possible power consumption across the operating temperature range. See the I_{DD} Specification Parameters and Operating Conditions table for details.

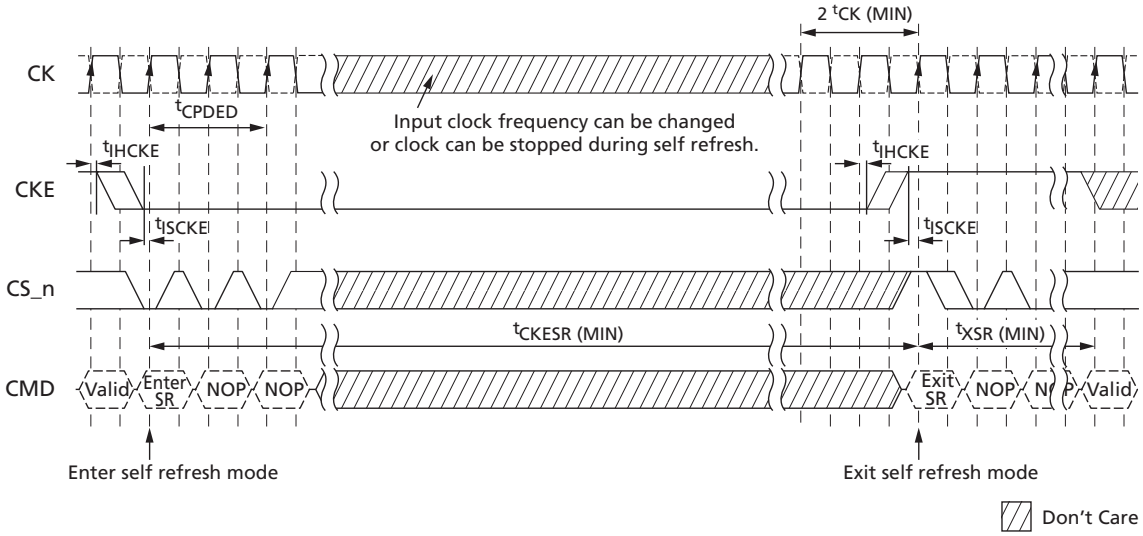
After the device has entered self refresh mode, all external signals other than CKE are "Don't Care." For proper SELF REFRESH operation, power supply pins (V_{DD1}, V_{DD2}, V_{DDQ}, and V_{DDCA}) must be at valid levels. V_{DDQ} can be turned off during self refresh. If V_{DDQ} is turned off, V_{REFDQ} must also be turned off. Prior to exiting self refresh, both V_{DDQ} and V_{REFDQ} must be within their respective minimum/maximum operating ranges (see AC and DC Operating Conditions). V_{REFDQ} can be at any level between 0 and V_{DDQ}; V_{REFCA} can be at any level between 0 and V_{DDCA} during self refresh.

Before exiting self refresh, V_{REFDQ} and V_{REFCA} must be within specified limits (see the AC and DC Logic Input Measurement Levels for Single-Ended Signals section). After entering self refresh mode, the device initiates at least one all-bank REFRESH command internally during ^{t}CKESR. The clock is internally disabled during SELF REFRESH operation to save power. The device must remain in self refresh mode for at least ^{t}CKESR. The user can change the external clock frequency or halt the external clock one clock after self refresh entry is registered; however, the clock must be restarted and stable before the device can exit SELF REFRESH operation.

Exiting self refresh requires a series of commands. First, the clock must be stable prior to CKE returning HIGH. After the self refresh exit is registered, a minimum delay, at least equal to the self refresh exit interval (^{t}XSR), must be satisfied before a valid command can be issued to the device. This provides completion time for any internal refresh in progress. For proper operation, CKE must remain HIGH throughout ^{t}XSR. NOP commands must be registered on each rising clock edge during ^{t}XSR. For the description of ODT operation and specifications during self-refresh entry and exit, see "On Die Termination" section.

Using self refresh mode introduces the possibility that an internally timed refresh event could be missed when CKE is driven HIGH for exit from self refresh mode. Upon exiting self refresh, at least one REFRESH command (one all-bank command or eight per-bank commands) must be issued before issuing a subsequent SELF REFRESH command.

Figure 34: SELF REFRESH Operation



Notes:
1. Input clock frequency can be changed or stopped during self refresh, provided that upon exiting self-refresh, a minimum of two cycles of stable clocks are provided, and the clock frequency is between the minimum and maximum frequencies for the particular speed grade.
2. The device must be in the all-banks-idle state prior to entering self refresh mode.
3. ^{t}XSR begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command can be issued only after ^{t}XSR is satisfied. NOPs must be issued during ^{t}XSR.

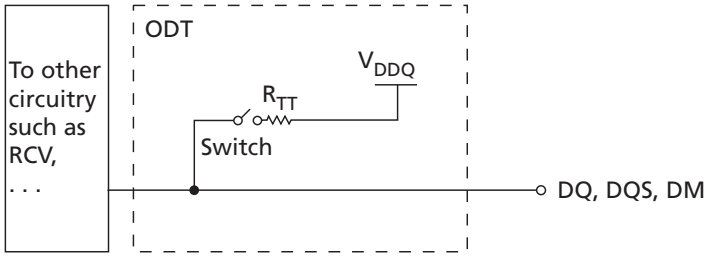
On-Die Termination (ODT)

On-die termination (ODT) is a feature that enables the device to enable/disable and turn on/off termination resistance for each DQ, DQS, and DM signal via the ODT control pin. ODT is designed to improve signal integrity of the memory channel by enabling the DRAM controller to independently turn on/off the internal termination resistance for any or all DRAM devices. The ODT pin directly controls ODT operation and is not sampled by the clock.

ODT is turned off and not supported in self refresh and deep power-down modes. The device will also disable termination during READ operations. ODT operation can be enabled optionally during power-down mode via a mode register. Note that if ODT is enabled during power-down mode, V_{DDQ} may not be turned off during power down. The DRAM will also disable termination during READ operations.

A simple functional representation of the ODT feature is shown below.

Figure 35:Functional Representation of On-Die Termination



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information. The value of R_{TT} (ODT termination resistance value) is determined by the settings of several mode register bits. The ODT pin will be ignored if MR11 is programmed to disable ODT in self refresh, in deep power-down, in CKE power-down (mode register option), and during READ operations.

ODT Mode Register

ODT mode is enabled if MR11[1:0] are non-zero. In this case, the value of R_{TT} is determined by the settings of those bits. ODT mode is disabled if MR11[1:0] are zero. MR11[2] determines whether ODT will operate during power-down mode if enabled through MR11[1:0].

Asychronous ODT

When enabled, the ODT feature is controlled asynchronously based on the status of the ODT pin. ODT is off under any of the following conditions:

- ODT is disabled through MR11[1:0]
- Device is performing a READ operation (READ or MRR)
- Device is in power-down mode and MR11[2] is zero
- Device is in self refresh or deep power-down mode
- Device is in CA training mode

In asynchronous ODT mode, the following timing parameters apply when ODT operation is controlled by the ODT pin ^{t}ODToff, ^{t}ODTon.

Minimum R_{TT} turn-on time (^{t}ODTon [MIN]) is the point in time when the device termination circuit leaves High-Z state and ODT resistance begins to turn on. Maximum R_{TT} turn-on time (^{t}ODTon,max) is the point in time when ODT resistance is fully on. ^{t}ODTon (MIN) and ^{t}ODTon (MAX) are measured from ODT pin HIGH.

Minimum R_{TT} turn-off time (^{t}ODToff [MIN]) is the point in time when the device termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (^{t}ODToff [MAX]) is the point in time when the on-die termination has reached High-Z. ^{t}ODToff,min and ^{t}ODToff (MAX) are measured from ODT pin LOW.

ODT During READ Operations (READ or MRR)

During READ operations, the device will disable termination and disable ODT control through the ODT pin. After READ operations are completed, ODT control is resumed through the ODT pin (if ODT mode is enabled).

ODT During Power-Down

When MR11[2] is zero, termination control through the ODT pin will be disabled when the DRAM enters power-down. After a power-down entry is registered, termination will be disabled within a time window specified by ^{t}ODTd (MIN) (MAX). ODT pin control is resumed when power-down is exited (if ODT mode is enabled). Between the POWER-DOWN EXIT command and until ^{t}XP is satisfied, termination will transition from disabled to control by the ODT pin. When ^{t}XP is satisfied, the ODT pin is used to control termination.

Minimum R_{TT} disable time (^{t}ODTd [MIN]) is the point in time when the device termination circuit is no longer controlled by the ODT pin. Maximum ODT disable time (^{t}ODTd [MAX]) is the point in time when ODT will be in High-Z.

When MR11[2] is enabled and MR11[1:0] are non-zero, ODT operation is supported during CKE power-down with ODT control through the ODT pin.

ODT During Self Refresh

The device disables the ODT function during self refresh. After a SELF REFRESH command is registered, termination will be disabled within a time window specified by ^{t}ODTd (MIN) (MAX). During self refresh exit, ODT control through the ODT pin is resumed (if ODT mode is enabled). Between the SELF REFRESH EXIT command and until ^{t}XSR is satisfied, termination will transition from disabled to control by the ODT pin. When ^{t}XSR is satisfied, the ODT pin is used to control termination.

ODT During Deep Power-Down

The device disables the ODT function during deep power-down. After a DEEP POWER-DOWN command is registered, termination will be disabled within a time window specified by ^{t}ODTd (MIN) (MAX).

ODT During CA Training and Write Leveling

During CA training mode, the device will disable ODT and ignore the state of the ODT control pin. For ODT operation during write leveling mode, refer to the DRAM Termination Function in Write-Leveling Mode table for termination activation and deactivation for DQ and DQS_t/DQS_c. If ODT is enabled, the ODT pin must be HIGH in write leveling mode.

Table 7: DRAM Termination Function in Write-Leveling Mode

ODT Pin	DQS Termination	DQ Termination
De-asserted	OFF	OFF
Asserted	ON	OFF

Table 8: ODT States Truth Table

	Write	Read/DQ Calibration	ZQ Calibration	CA Training	Write Leveling
DQ termination	Enabled	Disabled	Disabled	Disabled	Disabled
DQS termination	Enabled	Disabled	Disabled	Disabled	Enabled

Figure 36: Asynchronous ODT Timing – RL = 12

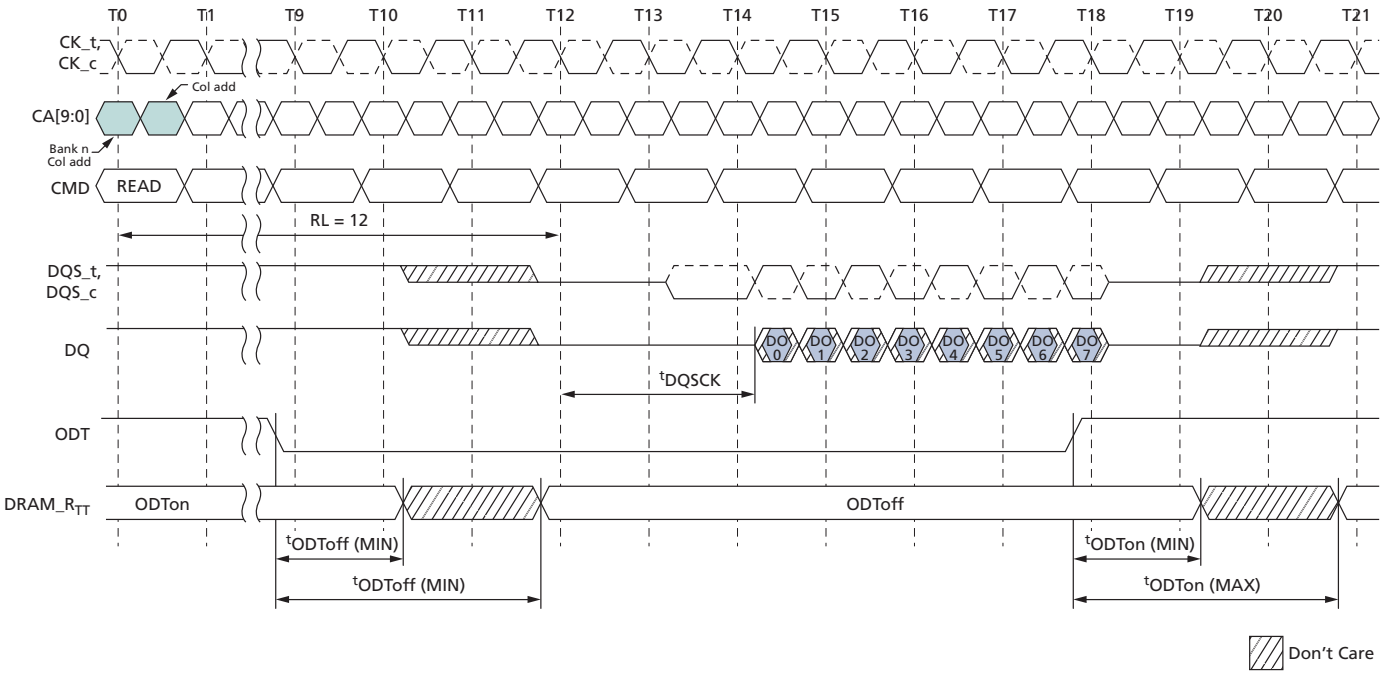
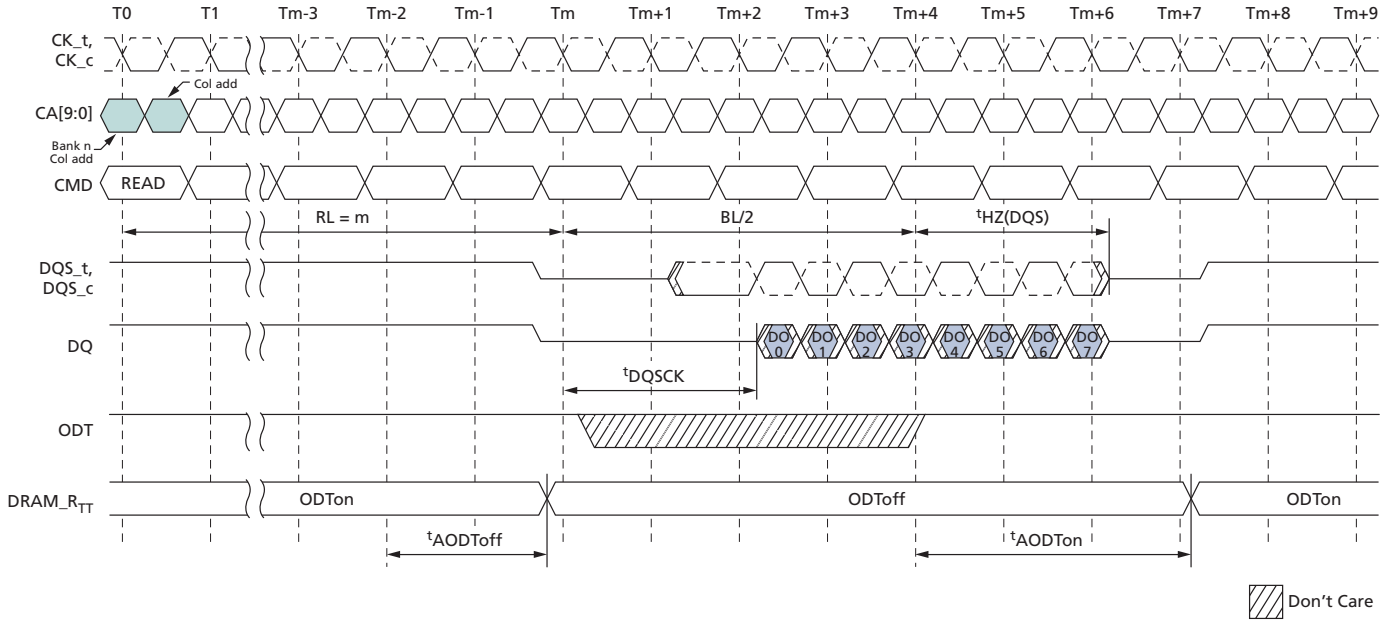
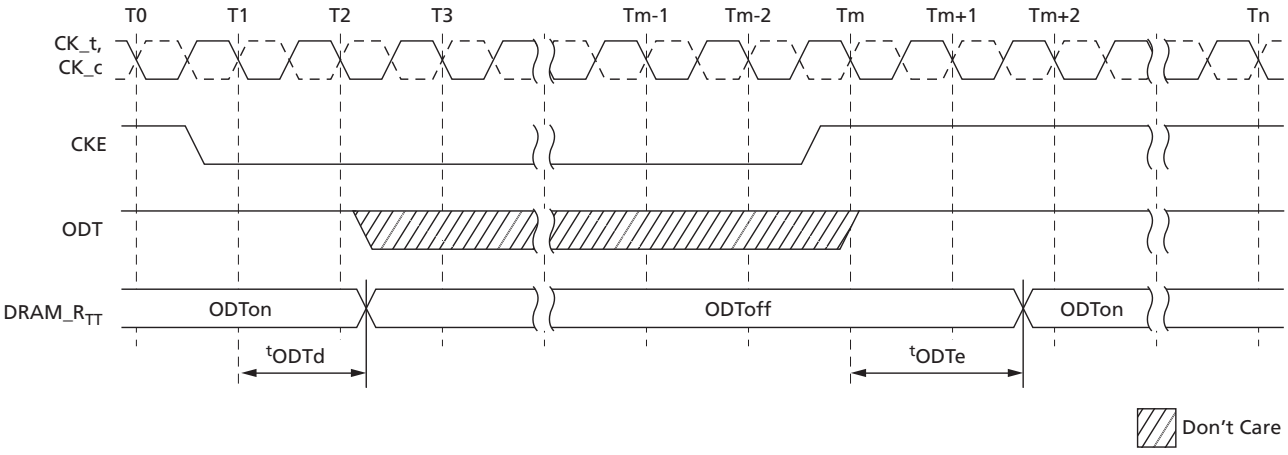


Figure 37: Automatic ODT Timing During READ Operation – RL = *m*



Notes:
1. The automatic R_{TT} turn-off delay, ^{t}AODToff, is referenced from the rising edge of RL - 2 clock at T_{m-2}.
2. The automatic R_{TT} turn-on delay, ^{t}AODTon, is referenced from the rising edge of RL + BL/2 clock at T_{m+4}.

Figure 38: ODT Timing During Power-Down, Self Refresh, Deep Power-Down Entry/Exit



Note:
1. Upon exiting of deep power-down mode, a complete power-up initialization sequence is required.

Power-Down

Power-down is entered synchronously when CKE is registered LOW and CS_n is HIGH at the rising edge of clock. A NOP command must be driven in the clock cycle following the POWER-DOWN command. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations, such as ROW ACTIVATION, PRECHARGE, AUTO PRECHARGE, or REFRESH are in progress, but the power-down I_{DD} specification is not applied until such operations are complete.

Entering power-down deactivates the input and output buffers, excluding CKE. To ensure enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW. this timing period is defined as ^{t}CPDED. CKE LOW results in deactivation of input receivers after ^{t}CPDED has expired. In power-down mode, CKE must be held LOW; all other input signals are “Don’t Care.” CKE LOW must be maintained until ^{t}CKE is satisfied, and V_{REFCA} must be maintained at a valid level during power-down.

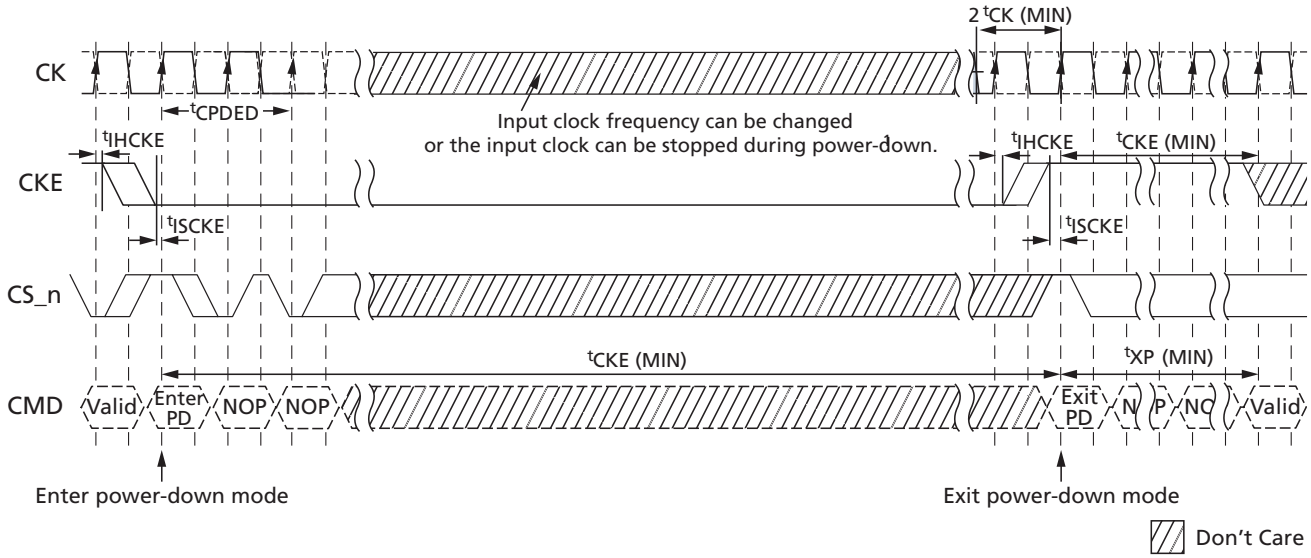
V_{DDQ} can be turned off during power-down. If V_{DDQ} is turned off, V_{REFDQ} must also be turned off. Prior to exiting power-down, both V_{DDQ} and V_{REFDQ} must be within their respective minimum/maximum operating ranges (see the AC and DC Operating Conditions section).

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in the REFRESH Command section.

The power-down state is exited when CKE is registered HIGH. The controller must drive CS_n HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until ^{t}CKE is satisfied. A valid, executable command can be applied with power-down exit latency ^{t}XP after CKE goes HIGH. Power-down exit latency is defined in the AC Timing table.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when a row is active in any bank, this mode is referred to as active power-down. For the description of ODT operation and specifications during power-down entry and exit, see the On-Die Termination section.

Figure 39: Power-Down Entry and Exit Timing



Note: 1. Input clock frequency can be changed or the input clock stopped during power-down, provided that the clock frequency is between the minimum and maximum specified frequencies for the speed grade in use and that prior to power-down exit, a minimum of two stable clocks complete.

Figure 40: CKE Intensive Environment

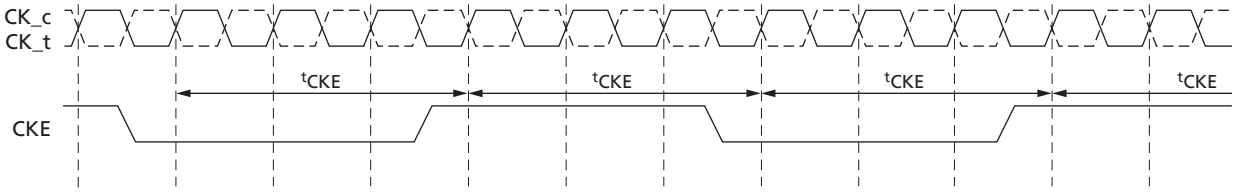
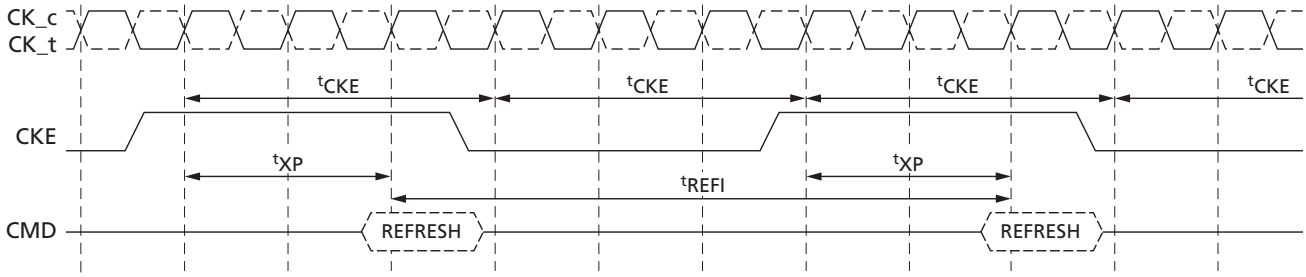
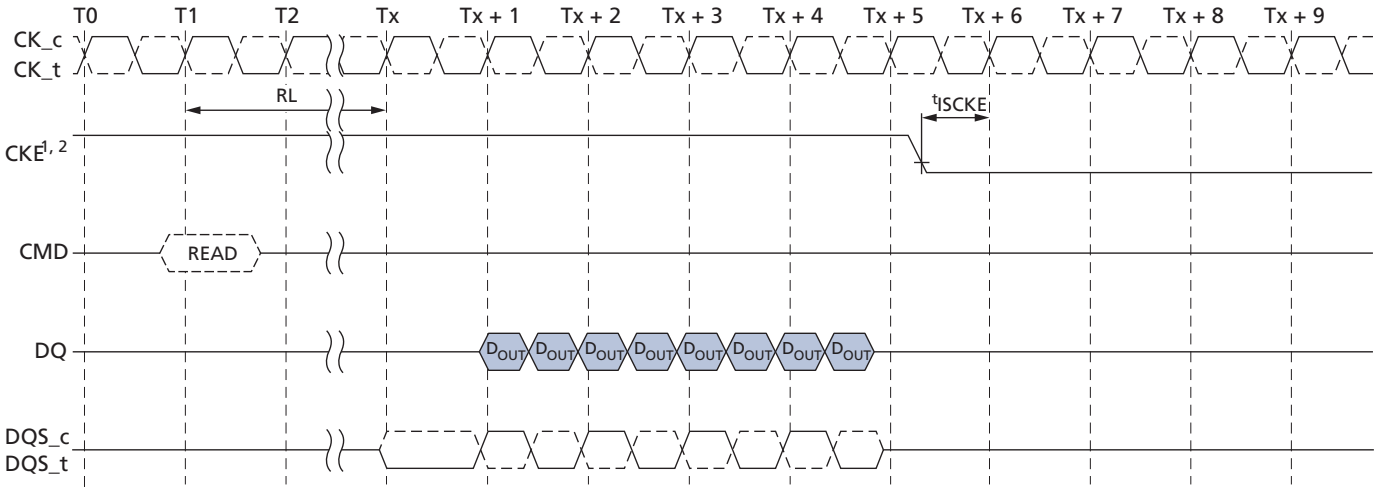


Figure 41: REFRESH to REFRESH Timing in CKE Intensive Environments



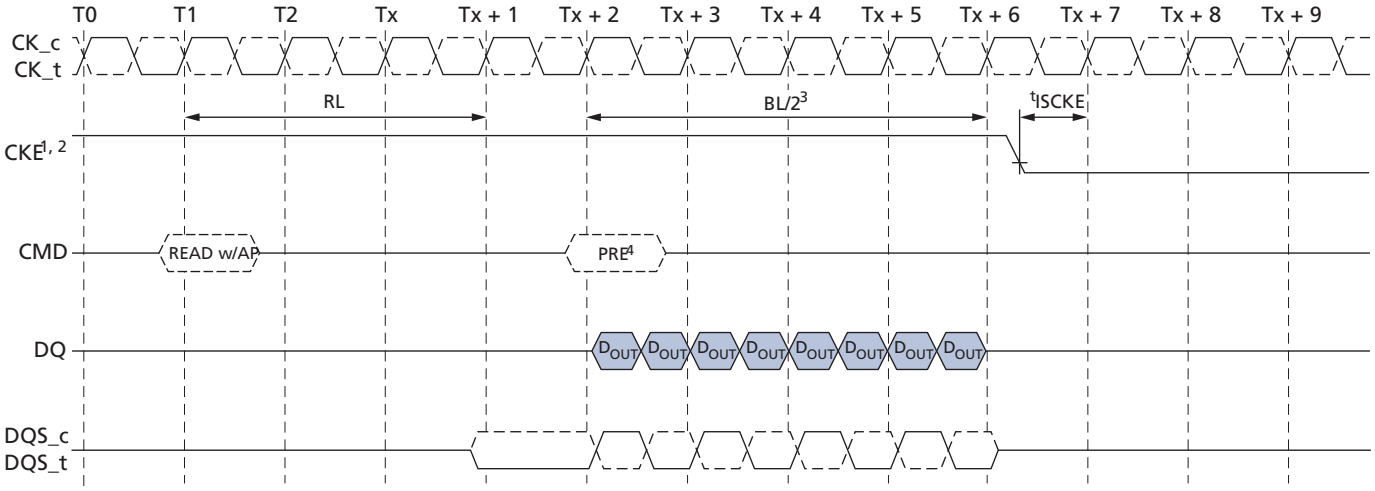
Note: 1. The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

Figure 42: READ to Power-Down Entry



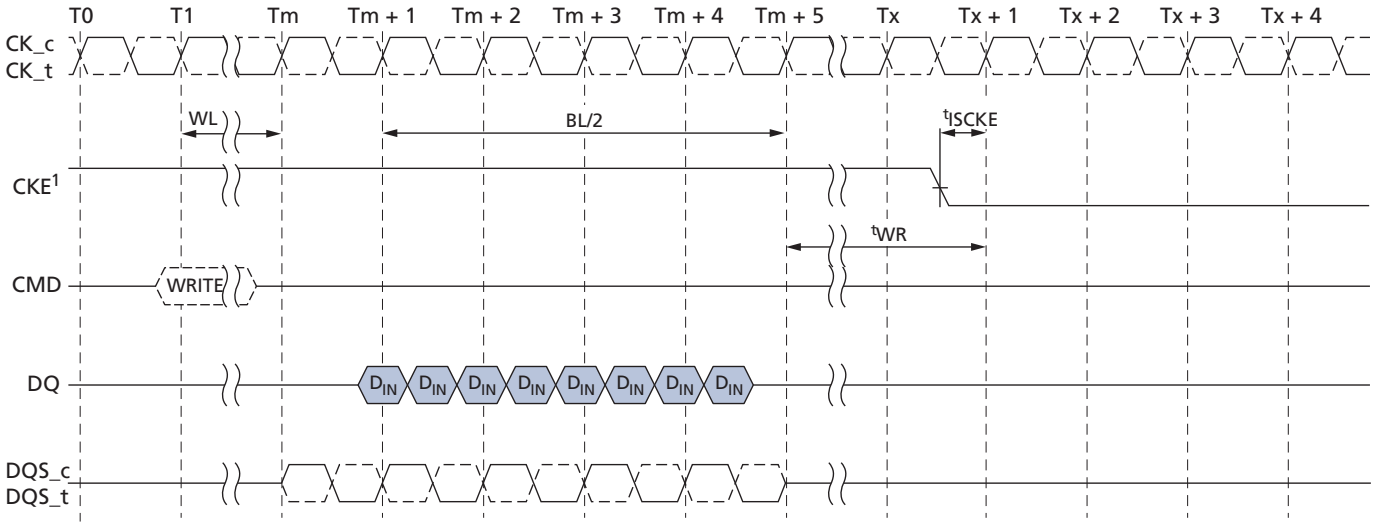
Notes: 1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at {RL + RU[tDQSCK(MAX)/tCK] + BL/2 + 1} clock cycles after the clock on which the READ command is registered.

Figure 43: READ with Auto Precharge to Power-Down Entry



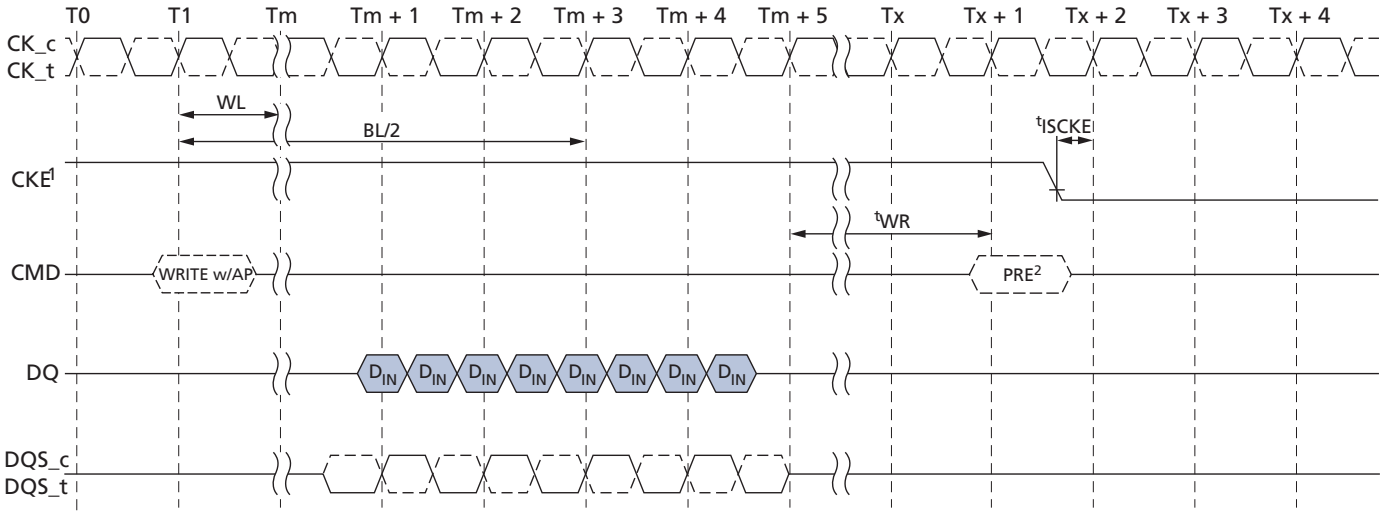
Notes:
1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at [RL + RU(^{t}DQSCK/^{t}CK) + BL/2 + 1] clock cycles after the clock on which the READ command is registered.
3. BL/2 with ^{t}RTP = 7.5ns and ^{t}RAS (MIN) is satisfied.
4. Start internal PRECHARGE.

Figure 44: WRITE to Power-Down Entry



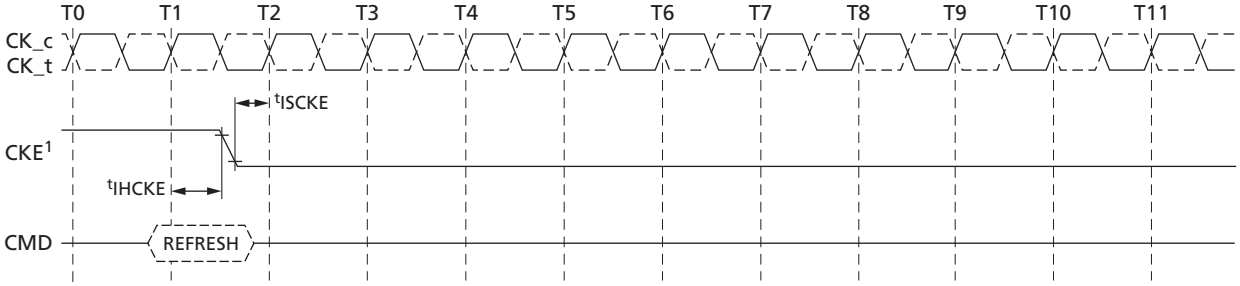
Note:
1. CKE can be registered LOW at [WL + 1 + BL/2 + RU(^{t}WR/^{t}CK)] clock cycles after the clock on which the WRITE command is registered.

Figure 45: WRITE with Auto Precharge to Power-Down Entry



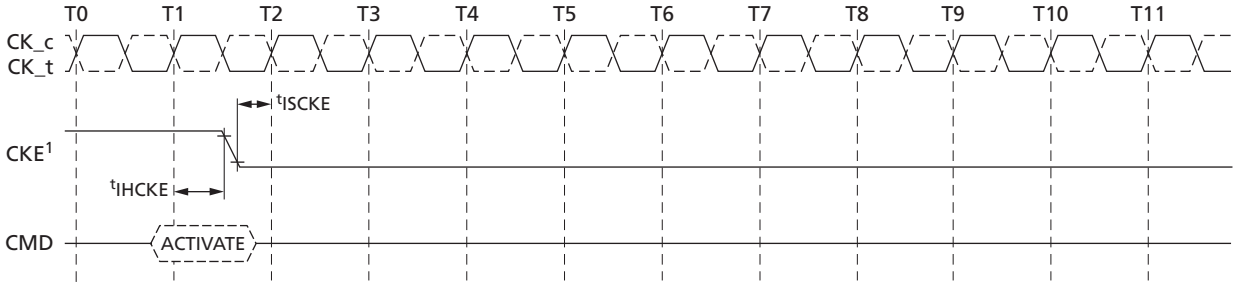
Notes:
1. CKE can be registered LOW at [WL + 1 + BL/2 + RU(^{t}WR/^{t}CK) + 1] clock cycles after the WRITE command is registered.
2. Start internal PRECHARGE.

Figure 46: REFRESH Command to Power-Down Entry



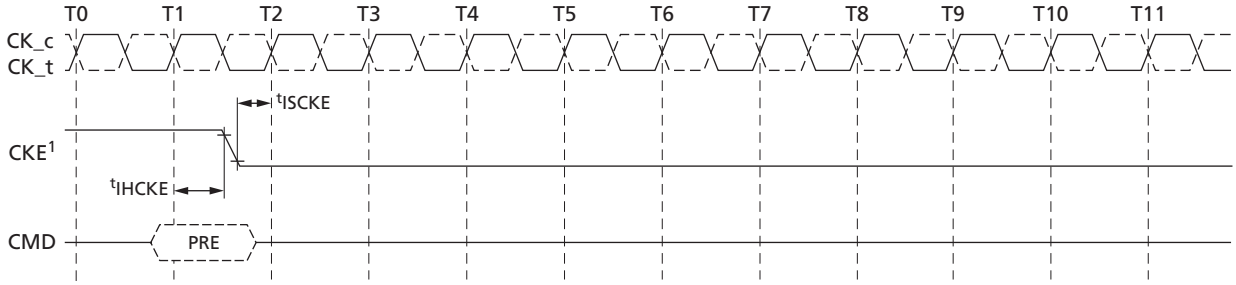
Note:
1. CKE can go LOW ^{t}IHCKE after the clock on which the REFRESH command is registered.

Figure 47: ACTIVATE Command to Power-Down Entry



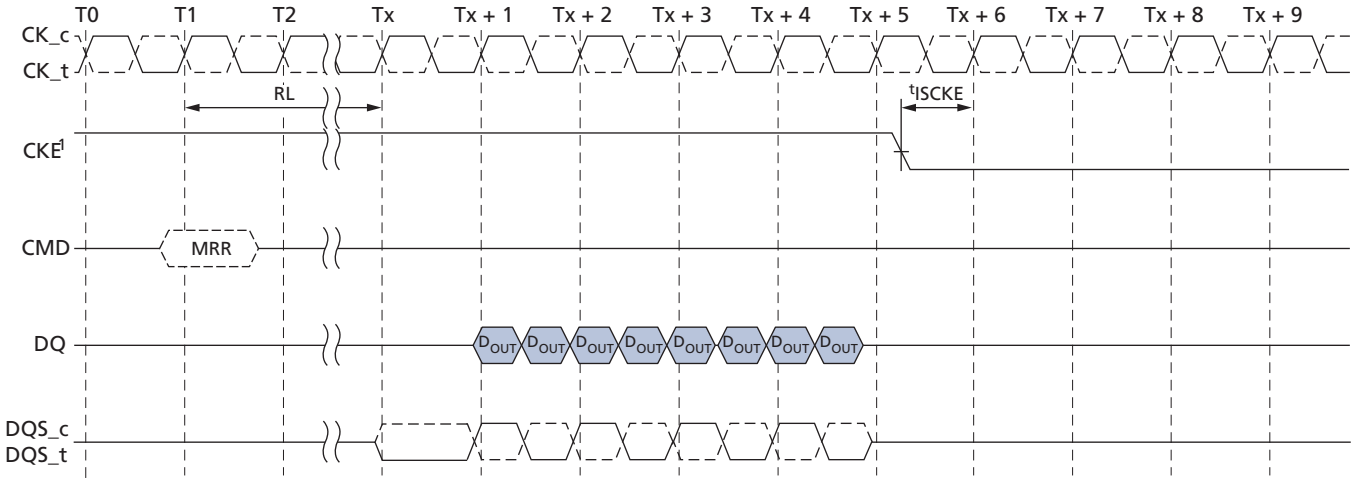
Note: 1. CKE can go LOW at ^{t}IHCKE after the clock on which the ACTIVATE command is registered.

Figure 48: PRECHARGE Command to Power-Down Entry



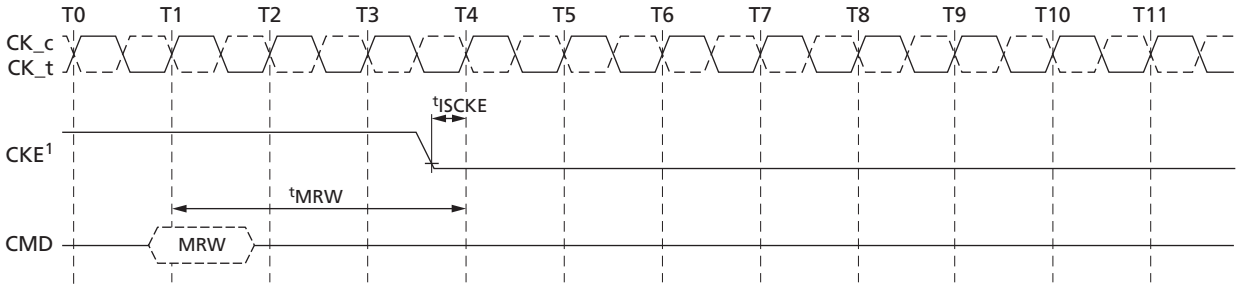
Note: 1. CKE can go LOW ^{t}IHCKE after the clock on which the PRECHARGE command is registered.

Figure 49: MRR Power-Down Entry



Note: 1. CKE can be registered LOW at [RL + RU(^{t}DQSCK/^{t}CK)+ BL/2 + 1] clock cycles after the clock on which the MRR command is registered.

Figure 50: MRW Command to Power-Down Entry



Note: 1. CKE can be registered LOW ^{t}MRW after the clock on which the MRW command is registered.

Deep Power-Down

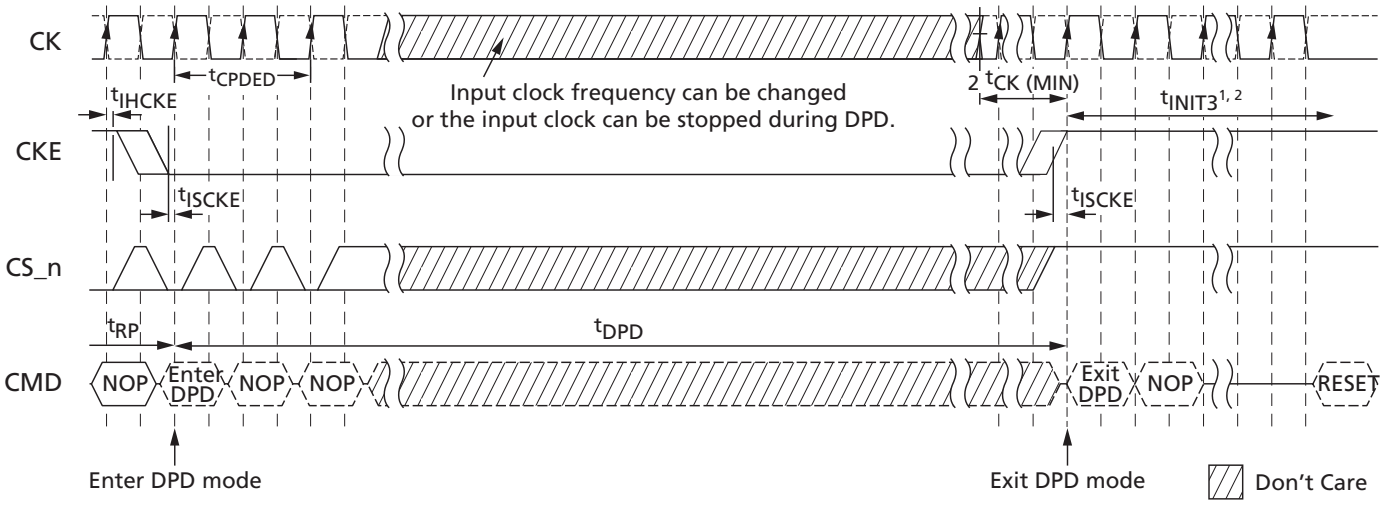
Deep power-down (DPD) is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of the clock. All banks must be in the idle state with no activity on the data bus prior to entering DPD mode. During DPD, CKE must be held LOW. The contents of the device will be lost upon entering DPD mode.

In DPD mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry are disabled within the device. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW; this timing period is defined as ^{t}CPDED. CKE LOW will result in deactivation of command and address receivers after ^{t}CPDED has expired. V_{REFDQ} can be at any level between 0 and V_{DDQ}, and V_{REFCA} can be at any level between 0 and V_{DDCA}

during DPD. All power supplies, including V_{REF}, must be within the specified limits prior to exiting DPD (see AC and DC Operating Conditions).

DPD mode is exited when CKE is registered HIGH while meeting ^{t}ISCKE, and the clock must be stable. The device must be fully reinitialized using the power-up initialization sequence. For a description of ODT operation and specifications during DPD entry and exit, see the ODT During Deep Power-Down section.

Figure 51: Deep Power-Down Entry and Exit Timing



Notes:
1. The initialization sequence can start at any time after Tx + 1.
2. ^{t}INIT3 and Tx + 1 refer to timings in the initialization sequence. For details, see the Mode Register Definition section.

AC Timing

Table 9: AC Timing

Notes 1–3 apply to all parameters and conditions

Parameter	Symbol	Min/Max	Data Rate				Unit	Notes
			1333	1600	1866	2133		
Maximum frequency	–	–	T.B.D	800	T.B.D	T.B.D	MHz	
Clock Timing								
Average clock period	^{t}CK(avg)	MIN	T.B.D	1.25	T.B.D	T.B.D	ns	
		MAX	100					
Average HIGH pulse width	^{t}CH(avg)	MIN	0.45				^{t}CK(avg)	
		MAX	0.55					
Average LOW pulse width	^{t}CL(avg)	MIN	0.45				^{t}CK(avg)	
		MAX	0.55					
Absolute clock period	^{t}CK(abs)	MIN	^{t}CK(avg) MIN + ^{t}JIT(per) MIN				ns	
Absolute clock HIGH pulse width	^{t}CH(abs)	MIN	0.43				^{t}CK(avg)	
		MAX	0.57					
Absolute clock LOW pulse width	^{t}CL(abs)	MIN	0.43				^{t}CK(avg)	
		MAX	0.57					
Clock period jitter (with supported jitter)	^{t}JIT(per), allowed	MIN	T.B.D	–70	T.B.D	T.B.D	ps	
		MAX	T.B.D	70	T.B.D	T.B.D		
Maximum clock jitter between two consecutive clock cycles (with allowed jitter)	^{t}JIT(cc), allowed	MAX	T.B.D	140	T.B.D	T.B.D	ps	
Duty cycle jitter (with supported jitter)	^{t}JIT(duty), allowed	MIN	min((^{t}CH(abs),min - ^{t}CH(avg),min), (^{t}CL(abs),min - ^{t}CL(avg),min)) × ^{t}CK(avg)				ps	
		MAX	max((^{t}CH(abs),max - ^{t}CH(avg),max), (^{t}CL(abs),max - ^{t}CL(avg),max)) × ^{t}CK(avg)					
Cumulative errors across 2 cycles	^{t}ERR(2per), allowed	MIN	T.B.D	-103	T.B.D	T.B.D	ps	
		MAX	T.B.D	103	T.B.D	T.B.D		
Cumulative errors across 3 cycles	^{t}ERR(3per), allowed	MIN	T.B.D	-122	T.B.D	T.B.D	ps	
		MAX	T.B.D	122	T.B.D	T.B.D		
Cumulative errors across 4 cycles	^{t}ERR(4per), allowed	MIN	T.B.D	-136	T.B.D	T.B.D	ps	
		MAX	T.B.D	136	T.B.D	T.B.D		
Cumulative errors across 5 cycles	^{t}ERR(5per), allowed	MIN	T.B.D	-147	T.B.D	T.B.D	ps	
		MAX	T.B.D	147	T.B.D	T.B.D		
Cumulative errors across 6 cycles	^{t}ERR(6per), allowed	MIN	T.B.D	-155	T.B.D	T.B.D	ps	
		MAX	T.B.D	155	T.B.D	T.B.D		
Cumulative errors across 7 cycles	^{t}ERR(7per), allowed	MIN	T.B.D	-163	T.B.D	T.B.D	ps	
		MAX	T.B.D	163	T.B.D	T.B.D		
Cumulative errors across 8 cycles	^{t}ERR(8per), allowed	MIN	T.B.D	-169	T.B.D	T.B.D	ps	
		MAX	T.B.D	169	T.B.D	T.B.D		

Table 10: AC Timing (Continued)

Notes 1–3 apply to all parameters and conditions

Parameter	Symbol	Min/Max	Data Rate				Unit	Notes
			1333	1600	1866	2133		
Cumulative errors across 9 cycles	^{t}ERR(9per), allowed	MIN	T.B.D	-175	T.B.D	T.B.D	ps	
		MAX	T.B.D	175	T.B.D	T.B.D		
Cumulative errors across 10 cycles	^{t}ERR(10per), allowed	MIN	T.B.D	-180	T.B.D	T.B.D	ps	
		MAX	T.B.D	180	T.B.D	T.B.D		
Cumulative errors across 11 cycles	^{t}ERR(11per), allowed	MIN	T.B.D	-184	T.B.D	T.B.D	ps	
		MAX	T.B.D	184	T.B.D	T.B.D		
Cumulative errors across 12 cycles	^{t}ERR(12per), allowed	MIN	T.B.D	-188	T.B.D	T.B.D	ps	
		MAX	T.B.D	188	T.B.D	T.B.D		
Cumulative errors across n = 13, 14, 15…, 19, 20 cycles	^{t}ERR(nper), allowed	MIN	^{t}ERR(nper),allowed MIN = (1 + 0.68ln(n)) × ^{t}JIT(per), allowed MIN				ps	
		MAX	^{t}ERR (nper), allowed MAX = (1 + 0.68ln(n)) × ^{t}JIT(per), allowed MAX					
ZQ Calibration Parameters								
Initialization calibration time	^{t}ZQINIT	MIN	1				µs	
Long calibration time	^{t}ZQCL	MIN	360				ns	
Short calibration time	^{t}ZQCS	MIN	90				ns	
Calibration RESET time	^{t}ZQRESET	MIN	MAX (50ns, 3nCK)				ns	
READ Parameters[4]								
DQS output access time from CK	^{t}DQSCK	MIN	2500				ps	
		MAX	5500					
DQSCK delta short	^{t}DQSCKDS	MAX	T.B.D	220	T.B.D	T.B.D	ps	5
DQSCK delta medium	^{t}DQSCKDM	MAX	T.B.D	511	T.B.D	T.B.D	ps	6
DQSCK delta long	^{t}DQSCKDL	MAX	T.B.D	614	T.B.D	T.B.D	ps	7
DQS-DQ skew	^{t}DQSQ	MAX	T.B.D	135	T.B.D	T.B.D	ps	
DQS output HIGH pulse width	^{t}QSH	MIN	^{t}CH(abs) - 0.05				^{t}CK(avg)	
DQS output LOW pulse width	^{t}QSL	MIN	^{t}CL(abs) - 0.05				^{t}CK(avg)	
DQ/DQS output hold time from DQS	^{t}QH	MIN	MIN (^{t}QSH, ^{t}QSL)				ps	
READ preamble	^{t}RPRE	MIN	0.9				^{t}CK(avg)	8, 9
READ postamble	^{t}RPST	MIN	0.3				^{t}CK(avg)	8, 10
DQS Low-Z from clock	^{t}LZ(DQS)	MIN	^{t}DQSCK (MIN) - 300				ps	8
DQ Low-Z from clock	^{t}LZ(DQ)	MIN	^{t}DQSCK (MIN) - 300				ps	8
DQS High-Z from clock	^{t}HZ(DQS)	MAX	^{t}DQSCK (MAX) - 100				ps	8
DQ High-Z from clock	^{t}HZ(DQ)	MAX	^{t}DQSCK (MAX) + (1.4 × ^{t}DQSQ (MAX))				ps	8
WRITE Parameters[4]								

Table 11: AC Timing (Continued)

Notes 1–3 apply to all parameters and conditions

Parameter	Symbol	Min/Max	Data Rate				Unit	Notes
			1333	1600	1866	2133		
DQ and DM input hold time (V_{REF} based)	^{t}DH	MIN	T.B.D	150	T.B.D	T.B.D	ps	
DQ and DM input setup time (V_{REF} based)	^{t}DS	MIN	T.B.D	150	T.B.D	T.B.D	ps	
DQ and DM input pulse width	^{t}DIPW	MIN	0.35				^{t}CK(avg)	
Write command to first DQS latching transition	^{t}DQSS	MIN	0.75				^{t}CK(avg)	
		MAX	1.25					
DQS input high-level width	^{t}DQSH	MIN	0.4				^{t}CK(avg)	
DQS input low-level width	^{t}DQSL	MIN	0.4				^{t}CK(avg)	
DQS rising edge to CK falling edge and DQS falling edge to CK rising edge setup time	^{t}DSS	MIN	0.2				^{t}CK(avg)	
CK rising edge to DQS falling edge and CK falling edge to DQS rising edge hold time	^{t}DSH	MIN	0.2				^{t}CK(avg)	
Write postamble	^{t}WPST	MIN	0.4				^{t}CK(avg)	
Write preamble	^{t}WPRE	MIN	0.8				^{t}CK(avg)	
CKE Input Parameters								
CKE minimum pulse width (HIGH and LOW pulse width)	^{t}CKE	MIN	MAX (7.5ns, 3nCK)				^{t}CK(avg)	
CKE input setup time	^{t}ISCKE	MIN	0.25				^{t}CK(avg)	11
CKE input hold time	^{t}IHCKE	MIN	0.25				^{t}CK(avg)	12
Command path disable delay	^{t}CPDED	MIN	2				^{t}CK(avg)	
Command Address Input Parameters[4]								
Address and control input setup time	^{t}ISCA	MIN	T.B.D	150	T.B.D	T.B.D	ps	13
Address and control input hold time	^{t}IHCA	MIN	T.B.D	150	T.B.D	T.B.D	ps	13
CS_n input hold time	^{t}ISCS	MIN	T.B.D	270	T.B.D	T.B.D	ps	13
CS_n input hold time	^{t}IHCS	MIN	T.B.D	270	T.B.D	T.B.D	ps	13
Address and control input pulse width	^{t}IPWCA	MIN	0.35				^{t}CK(avg)	
CS_n input pulse width	^{t}IPWCS	MIN	0.7				^{t}CK(avg)	
Boot Parameters (10–55 MHz)[14, 15, 16]								
Clock cycle time	^{t}CKb	MAX	100				ns	
		MIN	18					
CKE input setup time	^{t}ISCKEb	MIN	2.5				ns	
CKE input hold time	^{t}IHCKEb	MIN	2.5				ns	

Table 12: AC Timing (Continued)

Notes 1–3 apply to all parameters and conditions

Parameter	Symbol	Min/Max	Data Rate				Unit	Notes
			1333	1600	1866	2133		
Address and control input setup time	tISb	MIN	1150				ps	
Address and control input hold time	tIHb	MIN	1150				ps	
DQS output data access time from CK	tDQSCKb	MIN	2				ns	
		MAX	10					
Data strobe edge to output data edge	tDQSQb	MAX	1.2				ns	
Mode Register Parameters								
MODE REGISTER WRITE command period (MRW command to MRW command interval)	tMRW	MIN	10				tCK(avg)	
MODE REGISTER SET command delay (MRW command to non-MRW command interval)	tMRD	MIN	MAX (14nx, 10nCK)				ns	
MODE REGISTER READ command period	tMRR	MIN	4				tCK(avg)	
Additional time after tXP has expired until MRR command may be issued	tMRRI	MIN	tRCD (MIN)				ns	
Core Parameters[17]								
READ latency	RL	MIN	T.B.D	12	T.B.D	T.B.D	tCK(avg)	
WRITE latency (set A)	WL	MIN	T.B.D	6	T.B.D	T.B.D	tCK(avg)	
WRITE latency (set B)	WL	MIN	T.B.D	9	T.B.D	T.B.D	tCK(avg)	
ACTIVATE-to- ACTIVATE command period	tRC	MIN	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)				ns	
CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	tCKESR	MIN	MAX (15ns, 3nCK)				ns	
SELF REFRESH exit to next valid command delay	tXSR	MIN	MAX (tRFCab + 10ns, 2nCK)				ns	
Exit power-down to next valid command delay	tXP	MIN	MAX (7.5ns, 2nCK)				ns	
CAS-to-CAS delay	tCCD	MIN	4				tCK(avg)	
Internal READ to PRECHARGE command delay	tRTP	MIN	MAX (7.5ns, 4nCK)				ns	
RAS-to-CAS delay	tRCD	MIN	MAX (18ns, 3nCK)				ns	

Table 13: AC Timing (Continued)

Notes 1–3 apply to all parameters and conditions

Parameter	Symbol	Min/Max	Data Rate				Unit	Notes
			1333	1600	1866	2133		
Row precharge time (single bank)	^{t}RPpb	MIN	MAX (18ns, 3nCK)				ns	
Row precharge time (all banks)	^{t}RPpab	MIN	MAX (21ns, 3nCK)				ns	
Row active time	^{t}RAS	MIN	MAX (42ns, 3nCK)				ns	
		MAX	70				µs	
WRITE recovery time	^{t}WR	MIN	MAX (15ns, 3nCK)				ns	
Internal WRITE-to- READ command delay	^{t}WTR	MIN	MAX (7.5ns, 4nCK)				ns	
Active bank A to active bank B	^{t}RRD	MIN	MAX (10ns, 2nCK)				ns	
Four-bank ACTIVATE window	^{t}FAW	MIN	MAX (50ns, 8nCK)				ns	
Minimum deep power-down time	^{t}DPD	MIN	500				µs	
ODT Parameters								
Asynchronous R_{TT} turn-on dely from ODT input	^{t}ODTon	MIN	1.75				ns	
		MAX	3.5					
Asynchronous R_{TT} turn-off delay from ODT input	^{t}ODToff	MIN	1.75				ns	
		MAX	3.5					
Automatic R_{TT} turn-on delay after READ data	^{t}AODTon	MAX	^{t}DQSCK + 1.4 × ^{t}DQSQmax + ^{t}CK(avg,min)				ps	
Automatic R_{TT} turn-off delay after READ data	^{t}AODToff	MIN	^{t}DQSCKmin - 300				ps	
R_{TT} disable delay from power-down, self refresh, and deep power-down entry	^{t}ODTd	MAX	12				ns	
R_{TT} enable delay from power-down and self refresh exit	^{t}ODTe	MAX	12				ns	
CA Training Parameters								
First CA calibration command following CA training entry	^{t}CAMRD	MIN	20				^{t}CK(avg)	
First CA calibration command following CKE LOW	^{t}CAENT	MIN	10				^{t}CK(avg)	
CA calibration exit command following CKE HIGH	^{t}CAEXT	MIN	10				^{t}CK(avg)	
CKE LOW following CA calibration mode entry	^{t}CACKEL	MIN	10				^{t}CK(avg)	
CKE HIGH following last CA calibration results	^{t}CACKEH	MIN	10				^{t}CK(avg)	

Table 14: AC Timing (Continued)

Notes 1–3 apply to all parameters and conditions

Parameter	Symbol	Min/Max	Data Rate				Unit	Notes
			1333	1600	1866	2133		
Data out delay after CA training calibration command entry	tADR	MAX	20				ns	
MRW CA exit command to DQ tri-state	tMRZ	MIN	3				ns	
CA calibration command to CA calibration command delay	tCACD	MIN	RU(tADR/tCK) + 2				tCK(avg)	
Write Leveling Parameters								
DQS delay after write leveling mode is programmed	tWLDQSEN	MIN	25				ns	
		MAX	–					
First DQS edge after write leveling mode is programmed	tWLMRD	MIN	40				ns	
		MAX	–					
Write leveling output delay	tWLO	MIN	0				ns	
		MAX	20					
Write leveling hold time	tWLH	MIN	T.B.D	175	T.B.D	T.B.D	ps	
Write leveling setup time	tWLS	MIN	T.B.D	175	T.B.D	T.B.D	ps	
Temperature Derating Parameters								
DQS output access time from CK (derated)	tDQSCK	MAX	5620				ps	
RAS-to-CAS delay (derated)	tRCD	MIN	tRCD + 1.875				ns	
ACTIVATE-to- ACTIVATE command period (derated)	tRC	MIN	tRC + 1.875				ns	
Row active time (derated)	tRAS	MIN	tRAS + 1.875				ns	
Row precharge time (derated)	tRP	MIN	tRP + 1.875				ns	
Active bank A to active bank B (derated)	tRRD	MIN	tRRD + 1.875				ns	

I_{DD} Specifications

Table 15: I_{DD} Specifications(Dual Die , Single Channel)

V_{DD1} = 1.70–1.95V; V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V

Symbol	Supply	Speed			Unit	Parameter/Condition
		1333	1600	1866		
I_{DD01}	V_{DD1}	TBD	TBD	TBD	mA	Operating one bank active-precharge current ^{t}CK = ^{t}CK(avg) MIN; ^{t}RC = ^{t}RC (MIN); CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
$_{DD02}$	V_{DD2}	TBD	TBD	TBD		
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		
I_{DD2P1}	V_{DD1}	TBD	TBD	TBD	mA	Idle power-down standby current ^{t}CK = ^{t}CK(avg) MIN; CKE is LOW; CS_n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
I_{DD2P2}	V_{DD2}	TBD	TBD	TBD		
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		
I_{DD2PS1}	V_{DD1}	TBD	TBD	TBD	mA	Idle power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE; ODT disabled
I_{DD2PS2}	V_{DD2}	TBD	TBD	TBD		
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		
I_{DD2N1}	V_{DD1}	TBD	TBD	TBD	mA	Idle non power-down standby current ^{t}CK = ^{t}CK(avg) MIN; CKE is HIGH; CS_n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
$_{DD2N2}$	V_{DD2}	TBD	TBD	TBD		
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		
I_{DD2NS1}	V_{DD1}	TBD	TBD	TBD	mA	Idle non power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE; ODT disabled
I_{DD2NS2}	V_{DD2}	TBD	TBD	TBD		
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		
I_{DD3P1}	V_{DD1}	TBD	TBD	TBD	mA	Active power-down standby current ^{t}CK = ^{t}CK(avg) MIN; CKE is LOW; CS_n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
$_{DD3P2}$	V_{DD2}	TBD	TBD	TBD		
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		
I_{DD3PS1}	V_{DD1}	TBD	TBD	TBD	mA	Active power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE; ODT disabled
I_{DD3PS2}	V_{DD2}	TBD	TBD	TBD		
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		

Table 16: I_{DD} Specifications(Dual Die,Single Channel)(Continued)

V_{DD1} = 1.70–1.95V; V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V

Symbol	Supply	Speed			Unit	Parameter/Condition
		1333	1600	1866		
I_{DD3N1}	V_{DD1}	TBD	TBD	TBD	mA	Active non power-down standby current ^{t}CK = ^{t}CK(avg) MIN; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
I_{DD3N2}	V_{DD2}	TBD	TBD	TBD		
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		
I_{DD3NS1}	V_{DD1}	TBD	TBD	TBD	mA	Active non power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE; ODT disabled
I_{DD3NS2}	V_{DD2}	TBD	TBD	TBD		
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		
I_{DD4R1}	V_{DD1}	TBD	TBD	TBD	mA	Operating burst read current ^{t}CK = ^{t}CK(avg) MIN; CS_n is HIGH between valid commands; One bank active; BL = 8; RL = RL (MIN); CA bus inputs are SWITCHING; 50% data change each burst transfer; ODT disabled Values in parenthesis are for x16 bits
I_{DD4R2}	V_{DD2}	TBD	TBD	TBD		
$I_{DD4R,in}$	V_{DDCA}	TBD	TBD	TBD		
I_{DD4W1}	V_{DD1}	TBD	TBD	TBD	mA	Operating burst write current ^{t}CK = ^{t}CK(avg) MIN; CS_n is HIGH between valid commands; One bank active; BL = 8; WL = WL (MIN); CA bus inputs are SWITCHING; 50% data change each burst transfer; ODT disabled Values in parenthesis are for x16 bits
I_{DD4W2}	V_{DD2}	TBD	TBD	TBD		
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		
I_{DD51}	V_{DD1}	TBD	TBD	TBD	mA	All bank auto-refresh burst current ^{t}CK = ^{t}CK(avg) MIN; CKE is HIGH between valid commands; ^{t}RC = $^{t}RFCab$ (MIN); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
I_{DD52}	V_{DD2}	TBD	TBD	TBD		
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		
I_{DD5AB1}	V_{DD1}	TBD	TBD	TBD	mA	All bank auto-refresh average current ^{t}CK = ^{t}CK(avg) MIN; CKE is HIGH between valid commands; ^{t}RC = $^{t}REFI$; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
I_{DD5AB2}	V_{DD2}	TBD	TBD	TBD		
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		

Table 17: I_{DD} Specifications(Dual Die,Single Channel)(Continued)

V_{DD1} = 1.70–1.95V; V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V

Symbol	Supply	Speed			Unit	Parameter/Condition
		1333	1600	1866		
I_{DD5PB1}	V_{DD1}	TBD	TBD	TBD	mA	Per bank auto-refresh average current $^{t}CK = {}^{t}CK(avg)$ MIN; CKE is HIGH between valid commands; $^{t}RC = {}^{t}REFIpb$; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
I_{DD5PB2}	V_{DD2}	TBD	TBD	TBD		
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	TBD	TBD	TBD		

Notes: 1. Published I_{DD} values are the maximum of the distribution of the arithmetic mean.
2. I_{DD} current specifications are tested after the device is properly initialized.

Table 18: I_{DD6} Partial-Array Self Refresh Current at 25°C

V_{DD1} = 1.70–1.95V; V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V

PASR	Supply	Value	Unit	Parameter/Conditions
Full array	V_{DD1}	TBD	µA	Self-refresh current CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; ODT disabled
	V_{DD2}	TBD		
	V_{DDCA} + V_{DDQ}	TBD		
1/2 array	V_{DD1}	TBD		
	V_{DD2}	TBD		
	V_{DDCA} + V_{DDQ}	TBD		
1/4 array	V_{DD1}	TBD		
	V_{DD2}	TBD		
	V_{DDCA} + V_{DDQ}	TBD		
1/8 array	V_{DD1}	TBD		
	V_{DD2}	TBD		
	V_{DDCA} + V_{DDQ}	TBD		

Note: 1. I_{DD6} 25°C is the maximum of the distribution of the arithmetic mean.

Figure 52: Functional Block Diagram

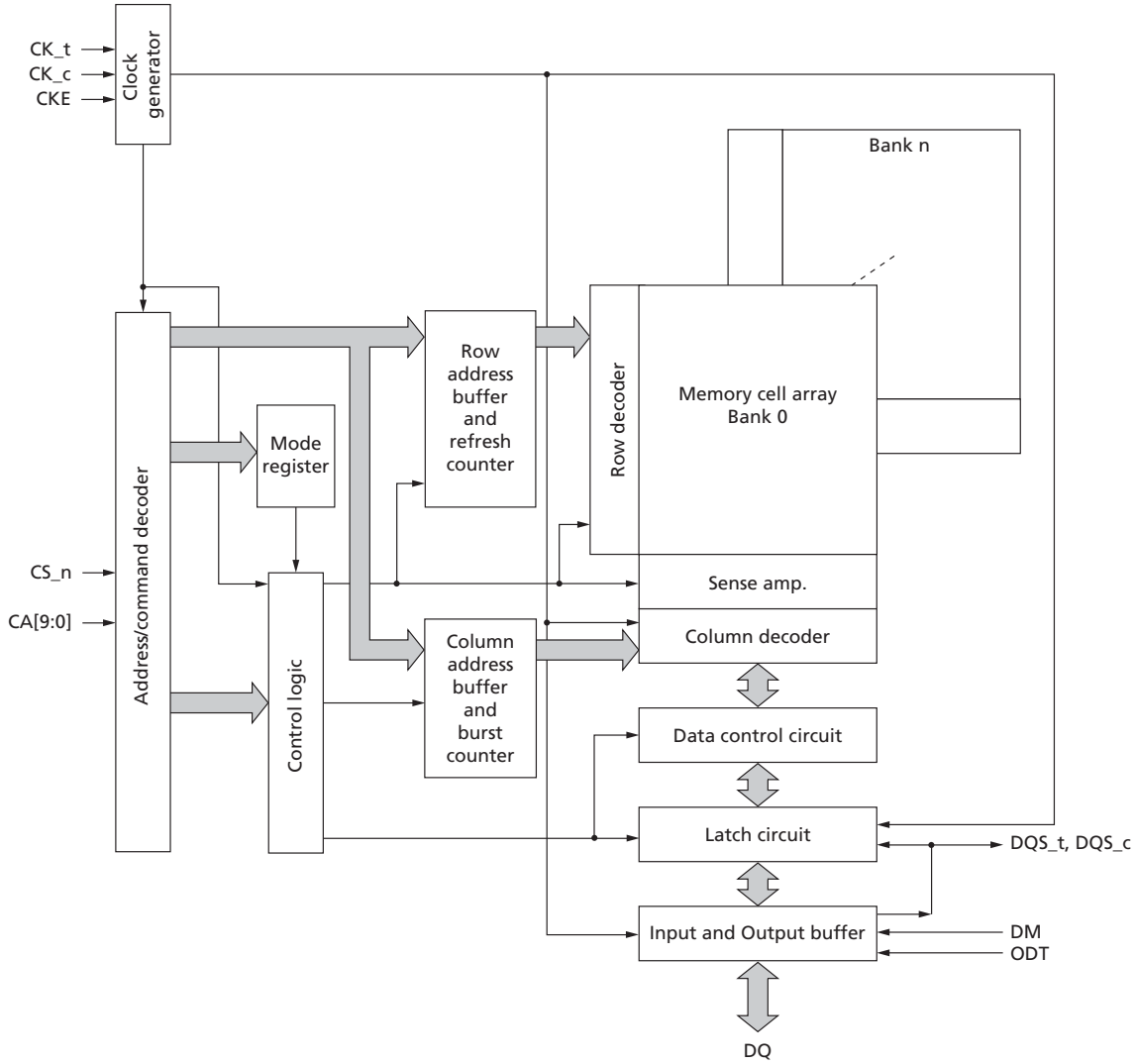
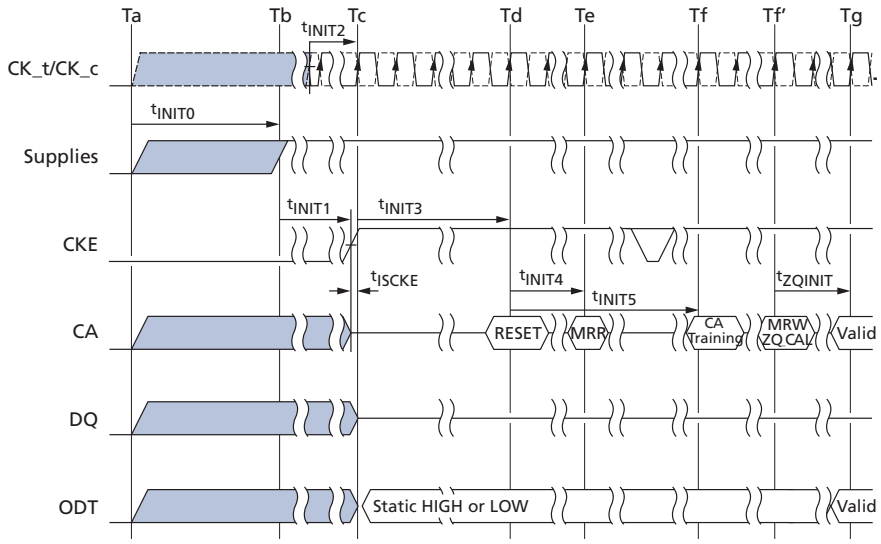


Figure 53: Voltage Ramp and Initialization Sequence



Notes:
1. High-Z on the CA bus indicates a valid NOP.
2. For ^{t}INIT values, see the Initialization Timing Parameters table.
3. After RESET command time (Tf), R_{TT} is disabled until ODT function is enabled by MRW to MR11 following Tg.
4. CA training is optional.

Table 19: Initialization Timing Parameters

Parameter	Min	Max	Unit	Comment
^{t}INIT0	–	20	ms	Maximum voltage ramp time (Note 1)
^{t}INIT1	100	–	ns	Minimum CKE LOW time after completion of voltage ramp
^{t}INIT2	5	–	^{t}CK	Minimum stable clock before first CKE HIGH
^{t}INIT3	200	–	µs	Minimum idle time after first CKE assertion
^{t}INIT4	1	–	µs	Minimum idle time after RESET command
^{t}INIT5	–	10	µs	Maximum duration of device auto initialization (Note 2)
^{t}ZQINIT	1	–	µs	ZQ initial calibration
^{t}CKb	18	100	ns	Clock cycle time during boot

Notes:
1. The ^{t}INIT0 maximum specification is not a tested limit and should be used as a general guideline. For voltage ramp times exceeding ^{t}INIT0 MAX, please contact the factory.
2. If the DAI bit is not read via MRR, the device will be in the idle state after ^{t}INIT5 (MAX) has expired.

Initialization After Reset (Without Voltage Ramp)

If the RESET command is issued before or after the power-up initialization sequence, the reinitialization procedure must begin at Td.

Table 20: LPDDR3 READ and WRITE Latency

Data Rate (Mb/p/s)	333	800	1066	1200	1333	1466	1600	1866	2133
^{t}CK(ns)	6	2.5	1.875	1.67	1.5	1.36	1.25	TBD	TBD
RL	3	6	8	9	10	11	12	TBD	TBD
WL (Set A)	1	3	4	5	6	6	6	TBD	TBD
WL (Set B)	1	3	4	5	8	9	9	TBD	TBD

AC and DC Operating Conditions

Operation or timing that is not specified is illegal. To ensure proper operation, the device must be initialized properly.

Table 21: Recommended DC Operating Conditions

Note 1 applies to entire table

Symbol	Min	Typ	Max	DRAM	Unit	Notes
V_{DD1}	1.70	1.80	1.95	Core power 1	V	2
V_{DD2}	1.14	1.20	1.30	Core power 2	V	
V_{DDCA}	1.14	1.20	1.30	Input buffer power	V	
V_{DDQ}	1.14	1.20	1.30	I/O buffer power	V	

Notes:
1. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 1 MHz at the DRAM package ball.
2. V_{DD1} uses significantly less power than V_{DD2}.

Table 22: Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input leakage current: For CA, CKE, CS_n, CK; Any input 0V ≤ V_{IN} ≤ V_{DDCA}; (All other pins not under test = 0V)	I_I	TBD	TBD	µA	1
V_{REF} supply leakage current: V_{REFDQ} = V_{DDQ}/2, or V_{REFCA} = V_{DDCA}/2; (All other pins not under test = 0V)	I_{VREF}	TBD	TBD	µA	2

Notes:
1. Although DM is for input only, the DM leakage must match the DQ and DQS output leakage specification.
2. The minimum limit requirement is for testing purposes. The leakage current on V_{REFCA} and V_{REFDQ} pins should be minimal.

Table 23: Operating Temperature Range

Notes 1 and 2 apply to entire table

Parameter/Condition	Symbol	Min	Max	Unit
Standard (WT) temperature range	T_{CASE}[1]	0	75	˚C
Wide temperature range		TBD	TBD	˚C

Notes:
1. Operating temperature is the case surface temperature at the center of the top side of the device. For measurement conditions, refer to the JESD51-2 standard.
2. Either the device operating temperature or the temperature sensor can be used to set an appropriate refresh rate, determine the need for AC timing derating, and/or monitor the operating temperature (see Temperature Sensor). When using the temperature sensor, the actual device case temperature may be higher than the T_{CASE} rating that applies for the operating temperature range. For example, T_{CASE} could be above +85˚C when the temperature sensor indicates a temperature of less than +85˚C.

AC and DC Logic Input Measurement Levels for Single-Ended Signals

Table 24: Single-Ended AC and DC Input Levels for CA and CS_n Inputs

Parameter	Symbol	1333/1600		1866/2133			
		Min	Max	Min	Max	Unit	Notes
AC input logic HIGH	$V_{IHCA(AC)}$	V_{REF} + 0.150	Note 2	V_{REF} + 0.135	Note 2	V	1, 2
AC input logic LOW	$V_{ILCA(AC)}$	Note 2	V_{REF} - 0.150	Note 2	V_{REF} - 0.135	V	1, 2
DC input logic HIGH	$V_{IHCA(DC)}$	V_{REF} + 0.100	V_{DDCA}	V_{REF} + 0.100	V_{DDCA}	V	1
DC input logic LOW	$V_{ILCA(DC)}$	V_{SSCA}	V_{REF} - 0.100	V_{SSCA}	V_{REF} - 0.100	V	1
Reference voltage for CA and CS_n inputs	$V_{REFCA(DC)}$	0.49 × V_{DDCA}	0.51 × V_{DDCA}	0.49 × V_{DDCA}	0.51 × V_{DDCA}	V	3, 4

Notes:
1. For CA and CS_n input-only pins. V_{REF} = $V_{REFCA(DC)}$.
2. See figure: Overshoot and Undershoot Definition.
3. The AC peak noise on V_{REFCA} could prevent V_{REFCA} from deviating more than ±1% V_{DDCA} from $V_{REFCA(DC)}$ (for reference, approximately ±12mV).
4. For reference, approximately V_{DDCA}/2 ±12mV.

Table 25: Single-Ended AC and DC Input Levels for CKE

Parameter	Symbol	Min	Max	Unit	Notes
CKE input HIGH level	V_{IHCKE}	0.65 × V_{DDCA}	Note 1	V	1
CKE input LOW level	V_{ILCKE}	Note 1	0.35 × V_{DDCA}	V	1

Note:
1. See figure: Overshoot and Undershoot Definition.

Table 26: Single-Ended AC and DC Input Levels for DQ and DM

Parameter	Symbol	1333/1600		1866/2133			
		Min	Max	Min	Max	Unit	Notes
AC input logic HIGH	$V_{IHDQ(AC)}$	V_{REF} + 0.150	Note 2	V_{REF} + 0.135	Note 2	V	1, 2, 5
AC input logic LOW	$V_{ILDQ(AC)}$	Note 2	V_{REF} - 0.150	Note 2	V_{REF} - 0.135	V	1, 2, 5
DC input logic HIGH	$V_{IHDQ(DC)}$	V_{REF} + 0.100	V_{DDQ}	V_{REF} + 0.100	V_{DDQ}	V	1
DC input logic LOW	$V_{ILDQ(DC)}$	V_{SSQ}	V_{REF} - 0.100	V_{SSQ}	V_{REF} - 0.100	V	1
Reference voltage for DQ and DM inputs	$V_{REFDQ(DC)}$	0.49 × V_{DDQ}	0.51 × V_{DDQ}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	3, 4
Reference voltage for DQ and DM inputs (DQ ODT enabled)	$V_{REFDQ(DC)}$ DQODT,enabled	V_{ODTR}/2 - 0.01 × V_{DDQ}	V_{ODTR}/2 + 0.01 × V_{DDQ}	V_{ODTR}/2 - 0.01 × V_{DDQ}	V_{ODTR}/2 + 0.01 × V_{DDQ}	V	3, 5, 6

Notes:
1. For DQ input-only pins. V_{REF} = $V_{REFDQ(DC)}$.
2. See figure: Overshoot and Undershoot Definition.
3. The AC peak noise on V_{REFDQ} could prevent V_{REFDQ} from deviating more than ±1% V_{DDQ} from $V_{REFDQ(DC)}$ (for reference, approximately ±12mV).
4. For reference, approximately V_{DDQ}/2 ±12mV.

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these conditions, or any other conditions outside those indicated in the operational sections of this document, is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

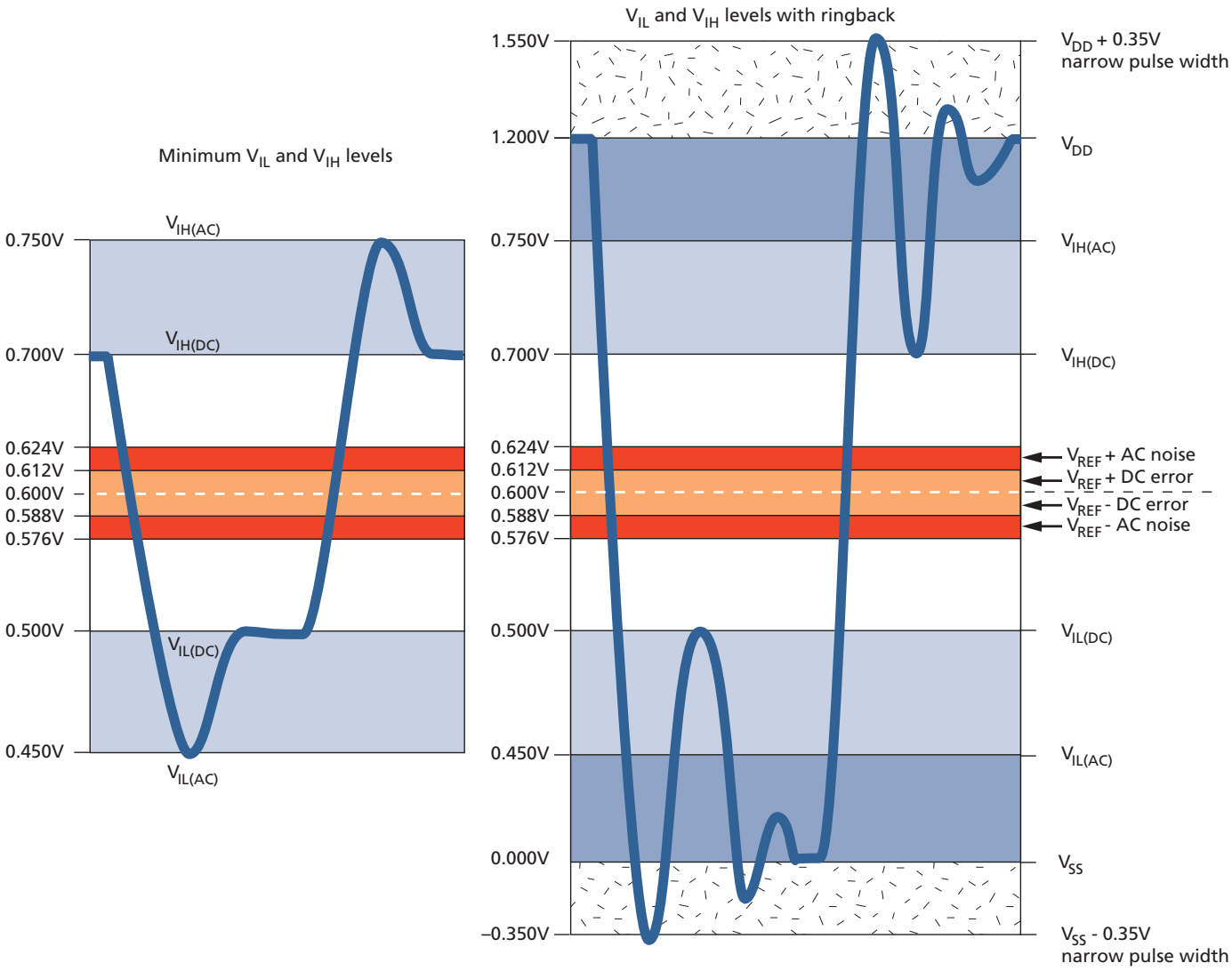
Table 27: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	–0.4	2.3	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	–0.4	1.6	V	1
V_{DDCA} supply voltage relative to V_{SSCA}	V_{DDCA}	–0.4	1.6	V	1, 2
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	–0.4	1.6	V	1, 3
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	1.6	V	
Storage temperature	T_{STG}	–55	125	˚C	4

Notes:
1. For information about relationships between power supplies, see the Power-Up and Initialization section.
2. $V_{REFCA} \leq 0.6 \times V_{DDCA}$; however, V_{REFCA} may be $\geq V_{DDCA}$, provided that $V_{REFCA} \leq 300mV$.
3. $V_{REFDQ} \leq 0.7 \times V_{DDQ}$; however, V_{REFDQ} may be $\geq V_{DDQ}$, provided that $V_{REFDQ} \leq 300mV$.
4. Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

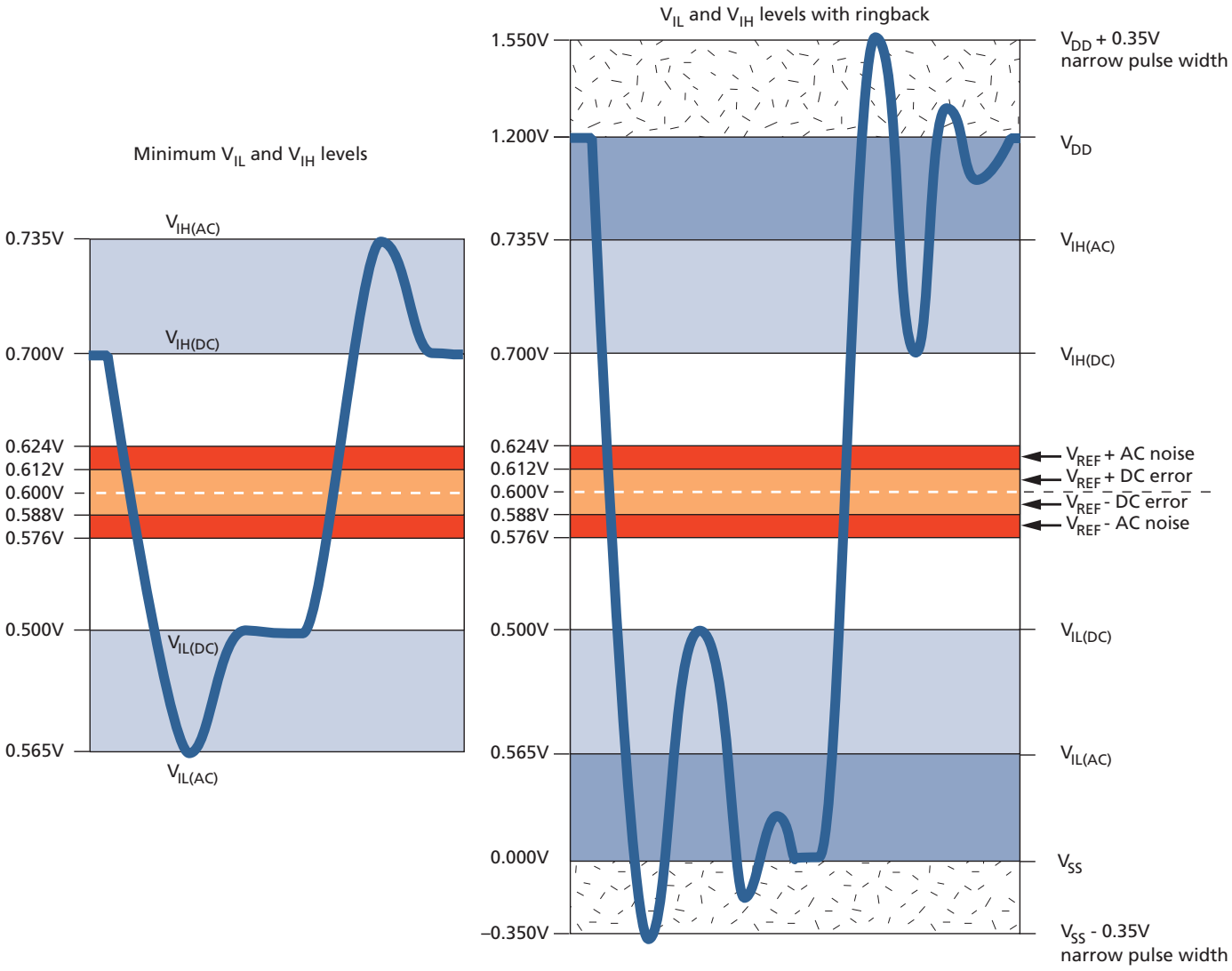
Input Signal

Figure 54: LPDDR3-1600 to LPDDR3-1333 Input Signal



Notes:
1. Numbers reflect typical values.
2. For CA[9:0], CK, and CS_n, V_{DD} stands for V_{DDCA}. For DQ, DM, DQS, and ODT, V_{DD} stands for V_{DDQ}.
3. For CA[9:0], CK, and CS_n, V_{SS} stands for V_{SSCA}. For DQ, DM, DQS, and ODT, V_{SS} stands for V_{SSQ}.

Figure 55: LPDDR3-2133 to LPDDR3-1866 Input Signal



Notes:
1. Numbers reflect typical values.
2. For CA[9:0], CK, and CS_n, V_{DD} stands for V_{DDCA}. For DQ, DM, DQS, and ODT, V_{DD} stands for V_{DDQ}.
3. For CA[9:0], CK, and CS_n, V_{SS} stands for V_{SSCA}. For DQ, DM, DQS, and ODT, V_{SS} stands for V_{SSQ}.

AC and DC Logic Input Measurement Levels for Differential Signals

Figure 56: Differential AC Swing Time and ^{t}DVAC

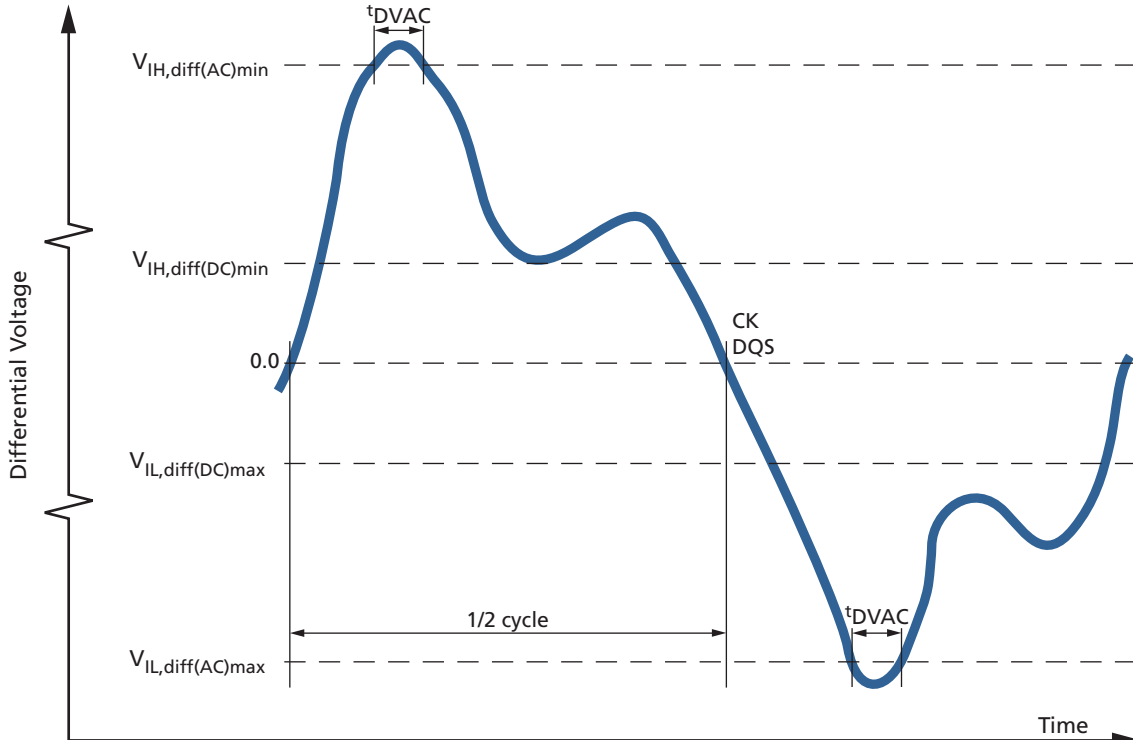


Table 28: Differential AC and DC Input Levels

For CK, $V_{REF} = V_{REFCA(DC)}$; For DQS, $V_{REF} = V_{REFDQ(DC)}$

Parameter	Symbol	LPDDR3		Unit	Notes
		Min	Max		
Differential input HIGH AC	$V_{IH,diff(AC)}$	2 × ($V_{IH(AC)}$ - V_{REF})	Note 1	V	2
Differential input LOW AC	$V_{IL,diff(AC)}$	Note 1	2 × ($V_{IL(AC)}$ - V_{REF})	V	2
Differential input HIGH DC	$V_{IH,diff(DC)}$	2 × ($V_{IH(DC)}$ - V_{REF})	Note 1	V	3
Differential input LOW DC	$V_{IL,diff(DC)}$	Note 1	2 × ($V_{IL(DC)}$ - V_{REF})	V	3

Notes:
1. These values are not defined; however, the single-ended signals CK and DQS must be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals, and must comply with the specified limitations for overshoot and undershoot (see figure: Overshoot and Undershoot Definition).
2. For CK, use $V_{IH}/V_{IL(AC)}$ of CA and V_{REFCA}; for DQS, use $V_{IH}/V_{IL(AC)}$ of DQ and V_{REFDQ}. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced voltage level also applies.
3. Used to define a differential signal slew rate.

Table 29: CK and DQS Time Requirements Before Ringback (tDVAC)

Slew Rate (V/ns)	tDVAC (ps) @ V_{IH}/$V_{IL,diff(AC)}$ = 300mV1333 Mb/s		tDVAC (ps) @ V_{IH}/$V_{IL,diff(AC)}$ = 300mV1600 Mb/s		tDVAC (ps) @ V_{IH}/$V_{IL,diff(AC)}$ = 270mV1866 Mb/s		tDVAC (ps) @ V_{IH}/$V_{IL,diff(AC)}$ = 270mV2133 Mb/s	
	Min	Max	Min	Max	Min	Max	Min	Max
>8.0	58	–	48	–	40	–	34	–
8.0	58	–	48	–	40	–	34	–
7.0	56	–	46	–	39	–	33	–
6.0	53	–	43	–	36	–	30	–
5.0	50	–	40	–	33	–	27	–
4.0	45	–	35	–	29	–	23	–
3.0	37	–	27	–	21	–	15	–
<3.0	37	–	27	–	21	–	15	–

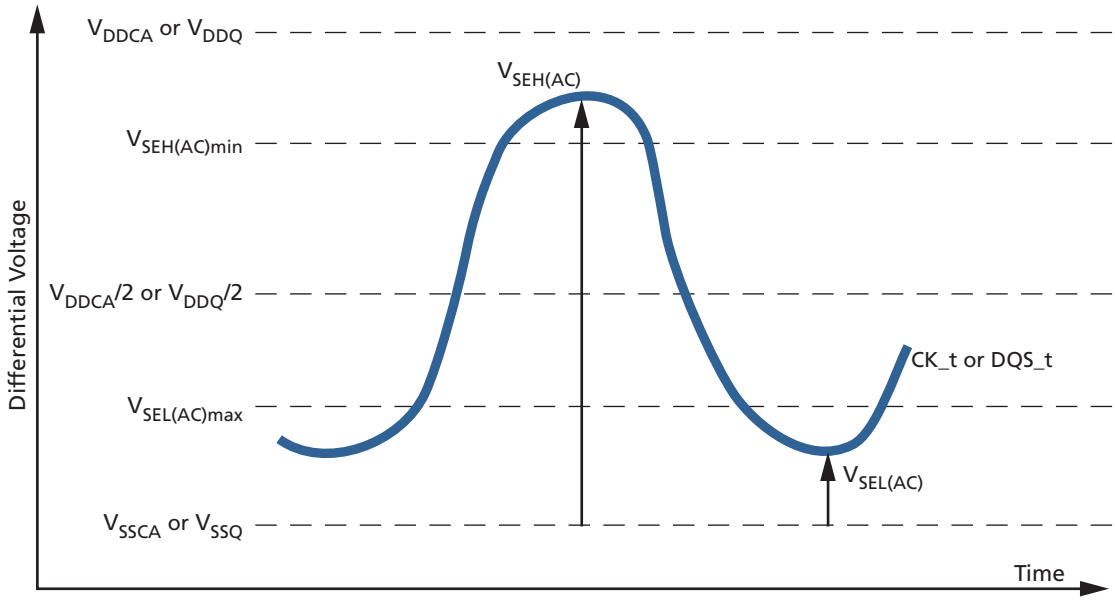
Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK and DQS) must also comply with certain requirements for single-ended signals.

CK must meet $V_{SEH(AC)min}$/$V_{SEL(AC)max}$ in every half cycle. DQS must meet $V_{SEH(AC)min}$/$V_{SEL(AC)max}$ in every half cycle preceding and following a valid transition.

The applicable AC levels for CA and DQ differ by speed bin.

Figure 57: Single-Ended Requirements for Differential Signals



Note: While CA and DQ signal requirements are referenced to V_{REF}, the single-ended components of differential signals also have a requirement with respect to $V_{DDQ}/2$ for DQS, and $V_{DDCA}/2$ for CK.

The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals, the requirement to reach $V_{SEL(AC)max}$ or $V_{SEH(AC)min}$ has no bearing on timing; however, this requirement adds a restriction on the common mode characteristics of these signals (see tables: Single-Ended AC and DC Input Levels for CA and CS_n Inputs; Single-Ended AC and DC Input Levels for DQ and DM).

Table 30: Single-Ended Levels for CK and DQS

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Single-ended HIGH level for strobes	$V_{SEH(AC150)}$	$(V_{DDQ}/2) + 0.150$	Note 1	V	2, 3
Single-ended HIGH level for CK		$(V_{DDCA}/2) + 0.150$	Note 1	V	2, 3
Single-ended LOW level for strobes	$V_{SEL(AC150)}$	Note 1	$(V_{DDQ}/2) - 0.150$	V	2, 3
Single-ended LOW level for CK		Note 1	$(V_{DDCA}/2) - 0.150$	V	2, 3
Single-ended HIGH level for strobes	$V_{SEH(AC135)}$	$(V_{DDQ}/2) + 0.135$	Note 1	V	2, 3
Single-ended HIGH level for CK		$(V_{DDCA}/2) + 0.135$	Note 1	V	2, 3
Single-ended LOW level for strobes	$V_{SEL(AC135)}$	Note 1	$(V_{DDQ}/2) + 0.135$	V	2, 3
Single-ended LOW level for CK		Note 1	$(V_{DDCA}/2) + 0.135$	V	2, 3

Notes:
1. These values are not defined; however, the single-ended signals CK and DQS[3:0] must be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals, and must comply with the specified limitations for overshoot and undershoot (see figure: Overshoot and Undershoot Definition).
2. For CK, use $V_{SEH}/V_{SEL(AC)}$ of CA; for strobes (DQS[3:0]), use $V_{IH}/V_{IL(AC)}$ of DQ.
3. $V_{IH(AC)}$ and $V_{IL(AC)}$ for DQ are based on V_{REFDQ}; $V_{SEH(AC)}$ and $V_{SEL(AC)}$ for CA are based on V_{REFCA}. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced level applies.

Differential Input Crosspoint Voltage

To ensure tight setup and hold times, as well as output skew parameters with respect to clock and strobe, each crosspoint voltage of differential input signals (CK, CK_c, DQS_t, and DQS_c) must meet the specifications in the table above. The differential input crosspoint voltage (V_{IX}) is measured from the actual crosspoint of the true signal and its and complement to the midlevel between V_{DD} and V_{SS}.

Figure 58: V_{IX} Definition

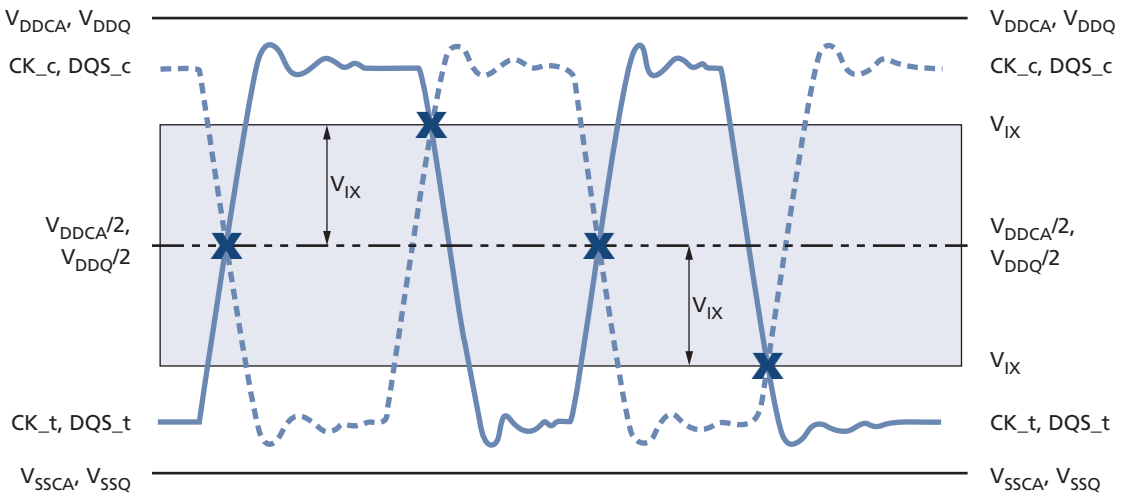


Table 31: Crosspoint Voltage for Differential Input Signals (CK, CK_c, DQS_t, DQS_c)

Parameter	Symbol	Min	Max	Unit	Notes
Differential input crosspoint voltage relative to $V_{DDCA}/2$ for CK	$V_{IXCA(AC)}$	–120	120	mV	1, 2
Differential input crosspoint voltage relative to $V_{DDQ}/2$ for DQS	$V_{IXDQ(AC)}$	–120	120	mV	1, 2

Notes:
1. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and it is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
2. For CK, $V_{REF} = V_{REFCA(DC)}$. For DQS, $V_{REF} = V_{REFDQ(DC)}$.

Input Slew Rate

Table 32: Differential Input Slew Rate Definition

Description	Measured[1]		Defined By
	From	To	
Differential input slew rate for rising edge (CK and DQS)	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$(V_{IH,diff,min} - V_{IL,diff,max}) / \Delta TR_{diff}$
Differential input slew rate for falling edge (CK and DQS)	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$(V_{IH,diff,min} - V_{IL,diff,max}) / \Delta TF_{diff}$

Note:
1. The differential signals (CK and DQS) must be linear between these thresholds.

Figure 59: Differential Input Slew Rate Definition for CK and DQS

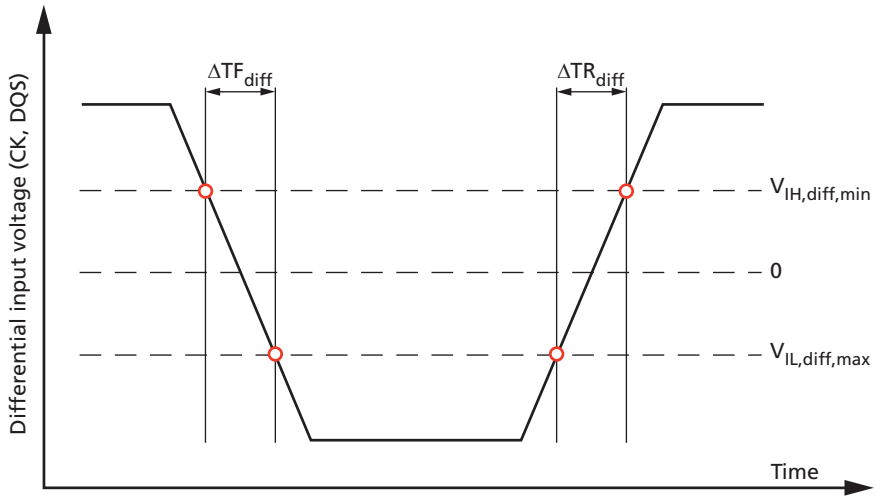


Figure 60: Typical Slew Rate and ^{t}VAC – ^{t}IS for CA and CS_n Relative to Clock

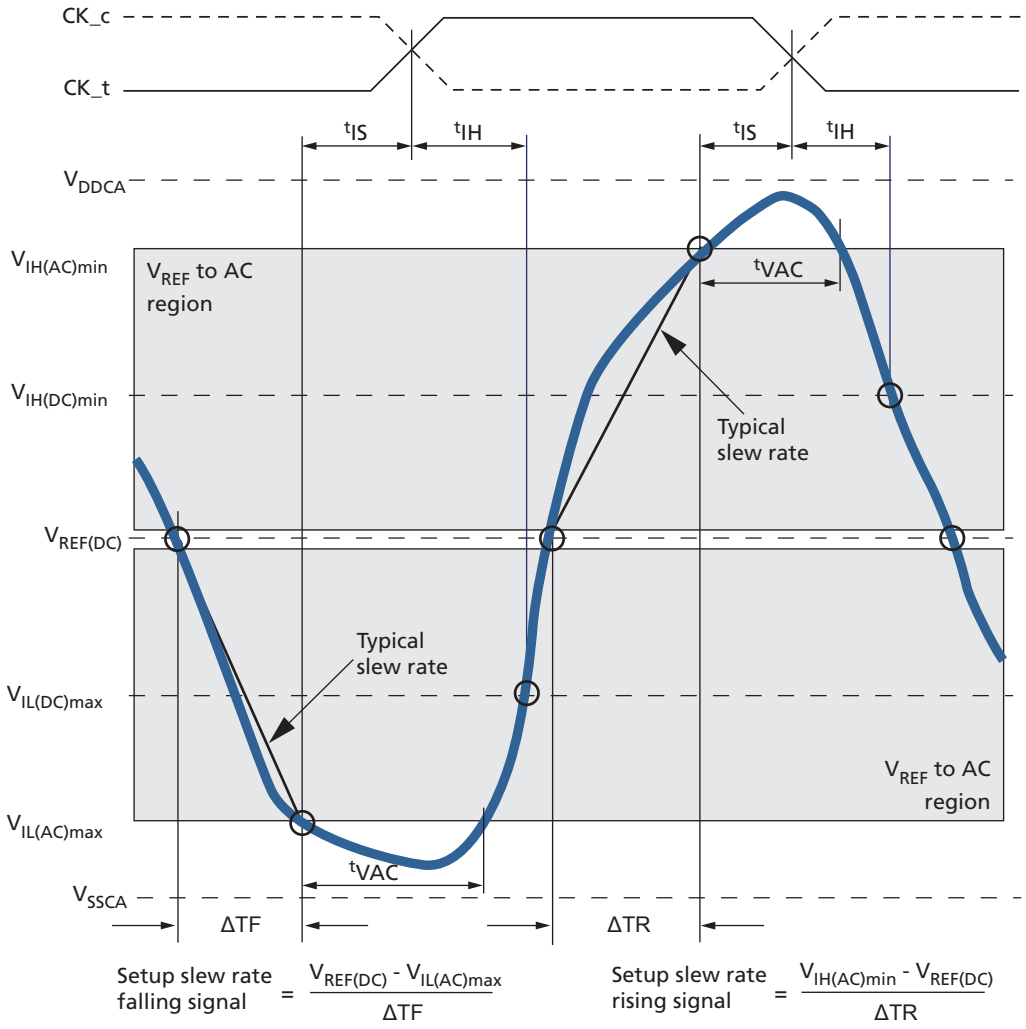
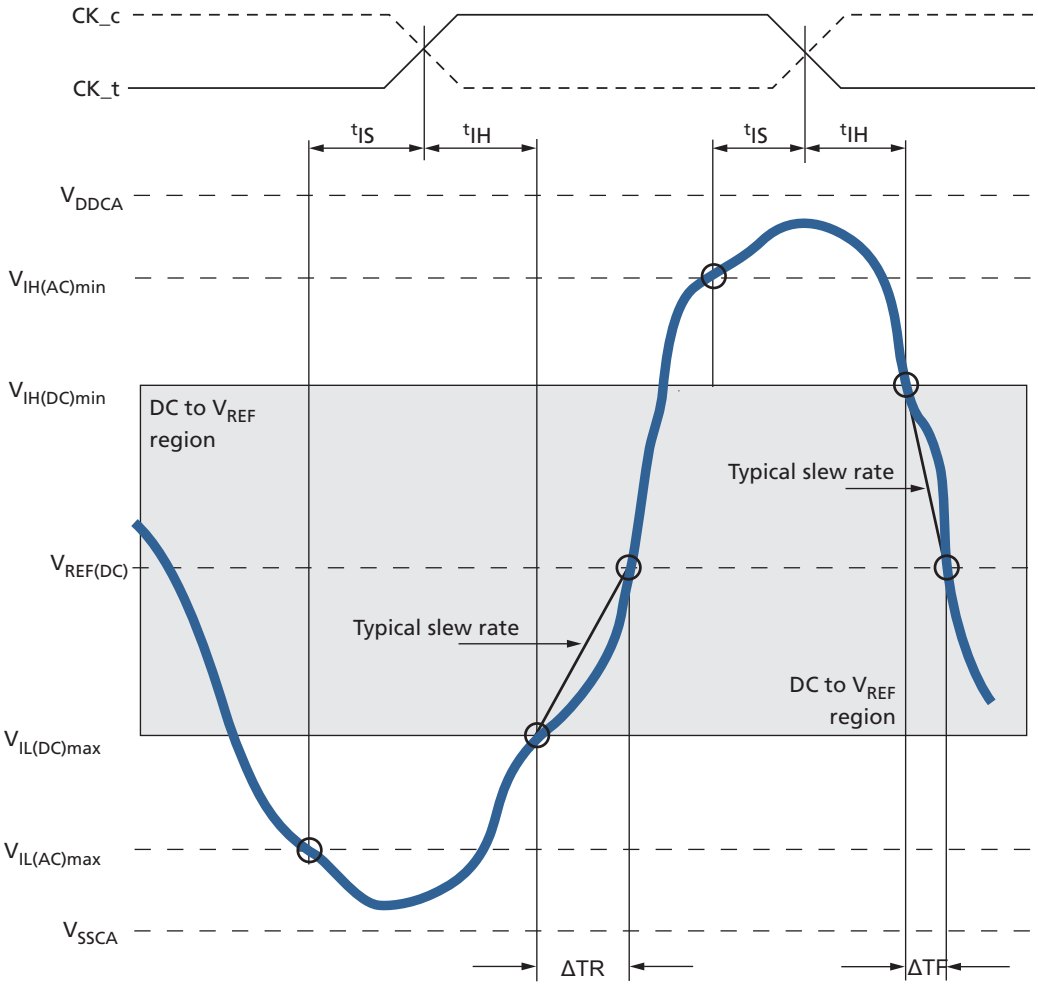


Figure 61: Typical Slew Rate – ^{t}IH for CA and CS_n Relative to Clock



$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

Figure 62: Tangent Line – ^{t}IS for CA and CS_n Relative to Clock

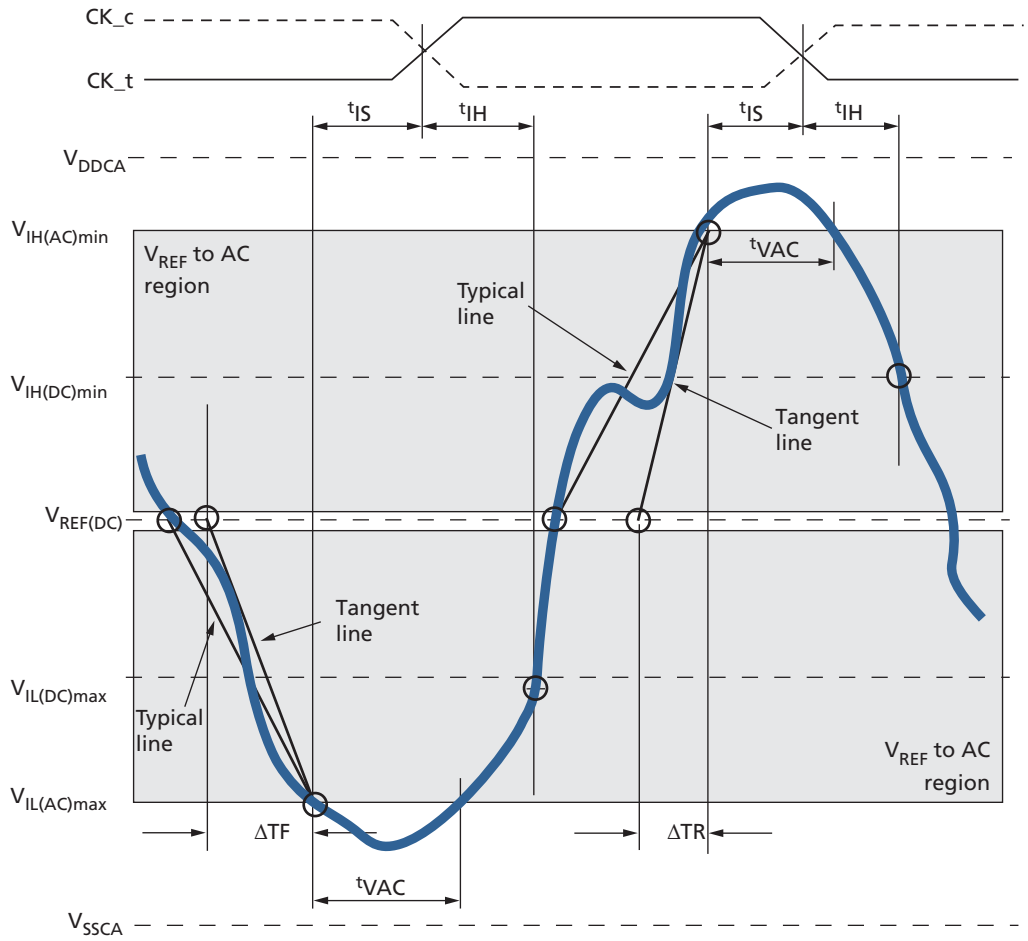
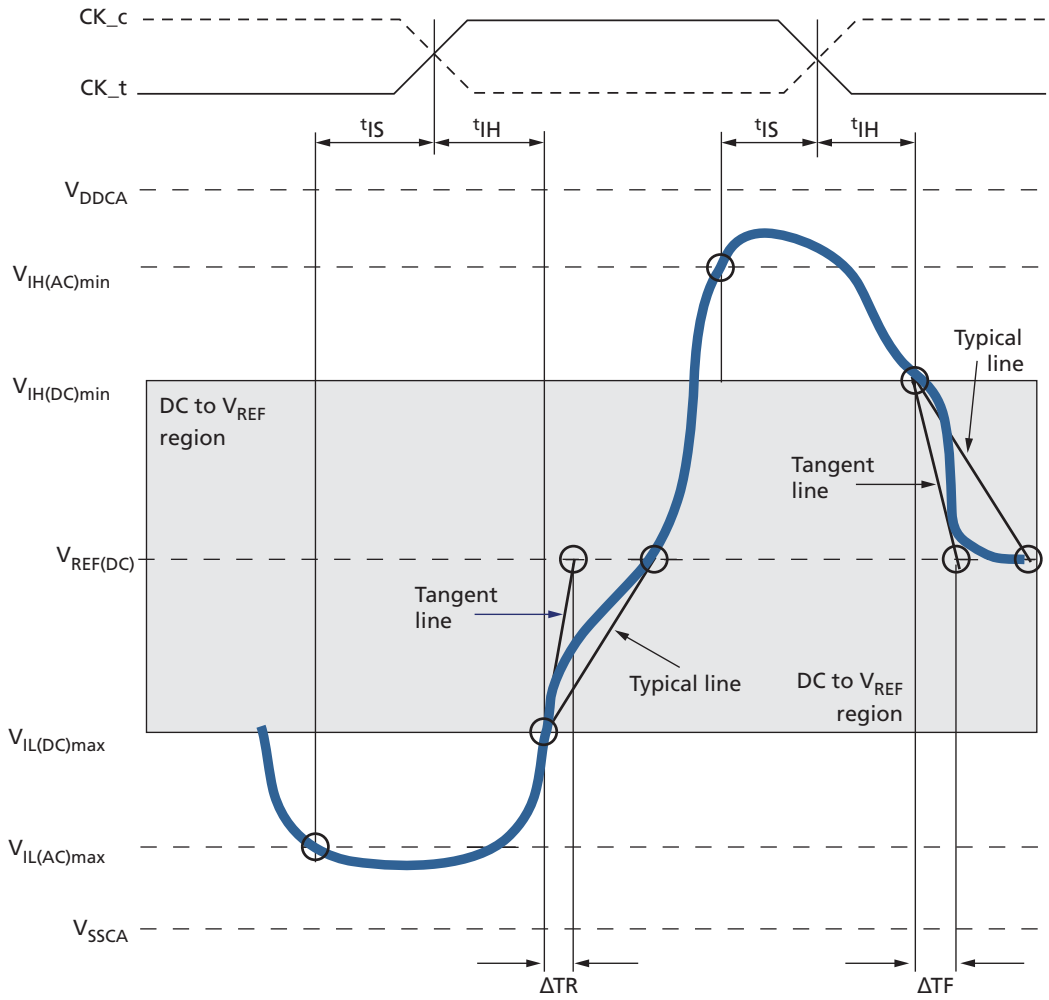


Figure 63: Tangent Line – ^{t}IH for CA and CS_n Relative to Clock



$$\text{Hold slew rate falling signal} = \frac{\text{tangent line } [V_{IH(DC)min} - V_{REF(DC)}]}{\Delta TF}$$

$$\text{Hold slew rate rising signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)max}]}{\Delta TR}$$

Table 33: Data Setup and Hold Base Values

Parameter	Data Rate				Reference
	1333	1600	1866	2133	
^{t}DS (base)	100	75	–	–	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ±150mV
^{t}DS (base)	–	–	62.5	–	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ±135mV
^{t}DH (base)	125	100	80	–	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ±100mV

Note: 1. AC/DC referenced for 2 V/ns DQ, DM slew rate, and 4 V/ns differential DQS slew rate and nominal V_{IX} .

Table 34: Derating Values for AC/DC-Based ^{t}DS/^{t}DH (AC150)

Δ^{t}DS, Δ^{t}DH derating in ps

		Δ^{t}DS, Δ^{t}DH Derating in [ps] AC/DC-based AC150 Threshold -> $V_{IH(ac)} = V_{REF(dc)}$ + 150mV, $V_{IL(ac)} = V_{REF(dc)}$ - 150mV DC100 Threshold -> $V_{IH(dc)} = V_{REF(dc)}$ + 100mV, $V_{IL(dc)} = V_{REF(dc)}$ - 100mV											
		DQS_t, DQS_c Differential Slew Rate											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
DQ, DM slew rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25		
	3.0			25	17	25	17	25	17	25	17	38	29
	2.0					0	0	0	0	**0**	**0**	13	13
	1.5							–25	–17	–25	–17	–12	–4

Note: 1. Shaded cells are not supported.

Table 35: Derating Values for AC/DC-Based ^{t}DS/^{t}DH (AC135)

Δ^{t}DS, Δ^{t}DH derating in ps

		Δ^{t}DS, Δ^{t}DH Derating in [ps] AC/DC-based AC135 Threshold -> $V_{IH(ac)} = V_{REF(dc)}$ + 135mV, $V_{IL(ac)} = V_{REF(dc)}$ - 135mV DC100 Threshold -> $V_{IH(dc)} = V_{REF(dc)}$ + 100mV, $V_{IL(dc)} = V_{REF(dc)}$ - 100mV											
		DQS_t, DQS_c Differential Slew Rate											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
DQ, DM slew rate V/ns	4.0	34	25	34	25	34	25	34	25	34	25		
	3.0			23	17	23	17	23	17	23	17	34	29
	2.0					0	0	0	0	**0**	**0**	11	13
	1.5							–23	–17	–23	–17	–12	–4

Note: 1. Shaded cells are not supported.

Table 36: Required Time for Valid Transition – $^{t}VAC > V_{IH(AC)}$ or $< V_{IL(AC)}$

Slew Rate (V/ns)	^{t}VAC at 150mV (ps) 1333 Mb/s		^{t}VAC at 150mV (ps) 1600 Mb/s		^{t}VAC at 135mV (ps) 1866 Mb/s		^{t}VAC at 135mV (ps) 2133 Mb/s	
	Min	Max	Min	Max	Min	Max	Min	Max
>4.0	58	–	48	–	40	–	34	–
4.0	58	–	48	–	40	–	34	–
3.5	56	–	46	–	39	–	33	–
3.0	53	–	43	–	36	–	30	–
2.5	50	–	40	–	33	–	27	–
2.0	45	–	35	–	29	–	23	–
1.5	37	–	27	–	21	–	15	–
<1.5	37	–	27	–	21	–	15	–

Figure 64: Typical Slew Rate and ^{t}VAC – ^{t}DS for DQ Relative to Strobe

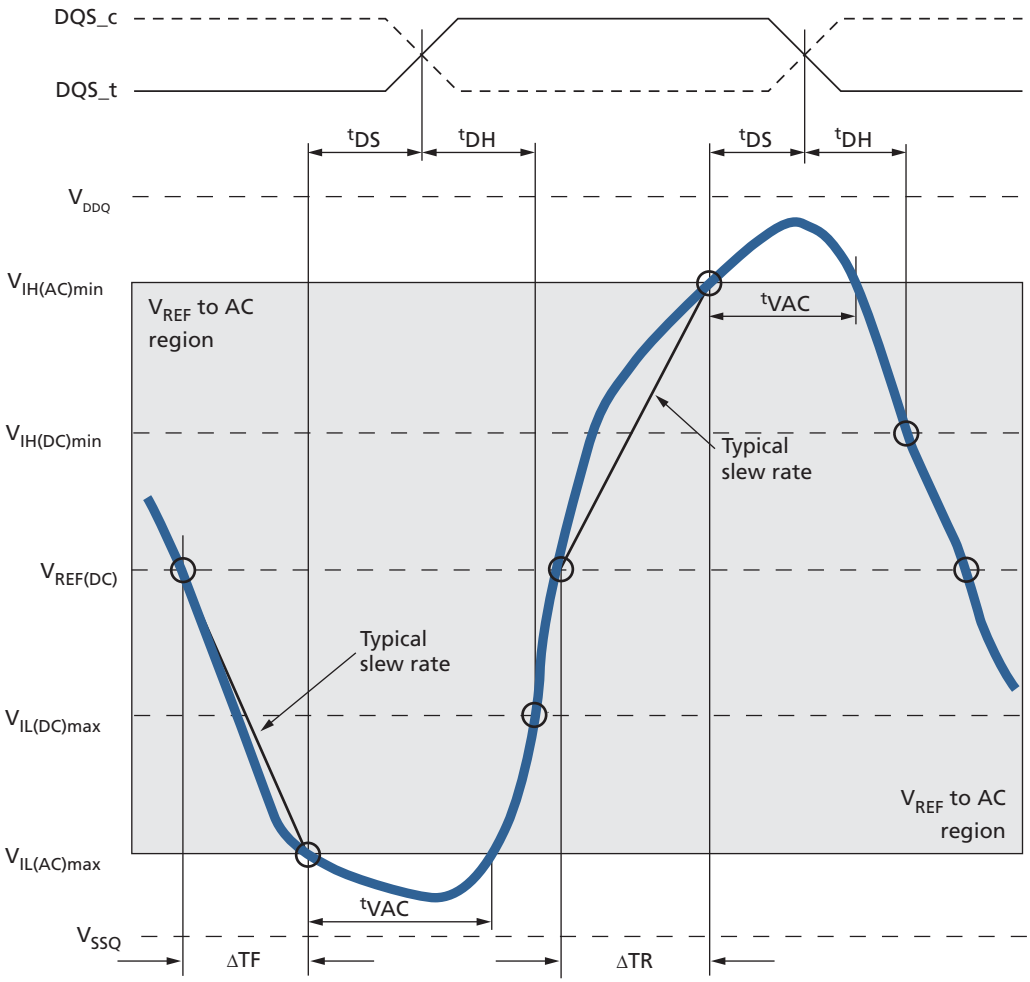


Figure 65: Typical Slew Rate – ^{t}DH for DQ Relative to Strobe

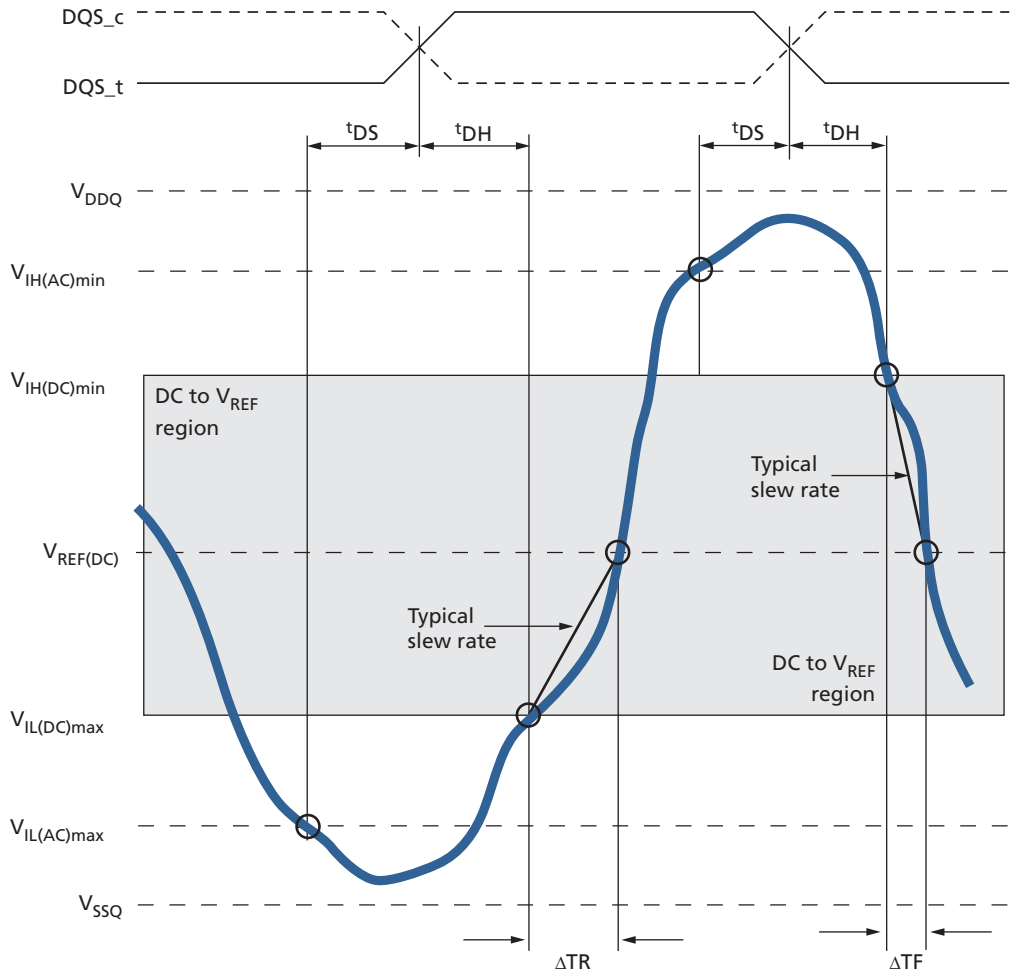


Figure 66: Tangent Line – ^{t}DS for DQ with Respect to Strobe

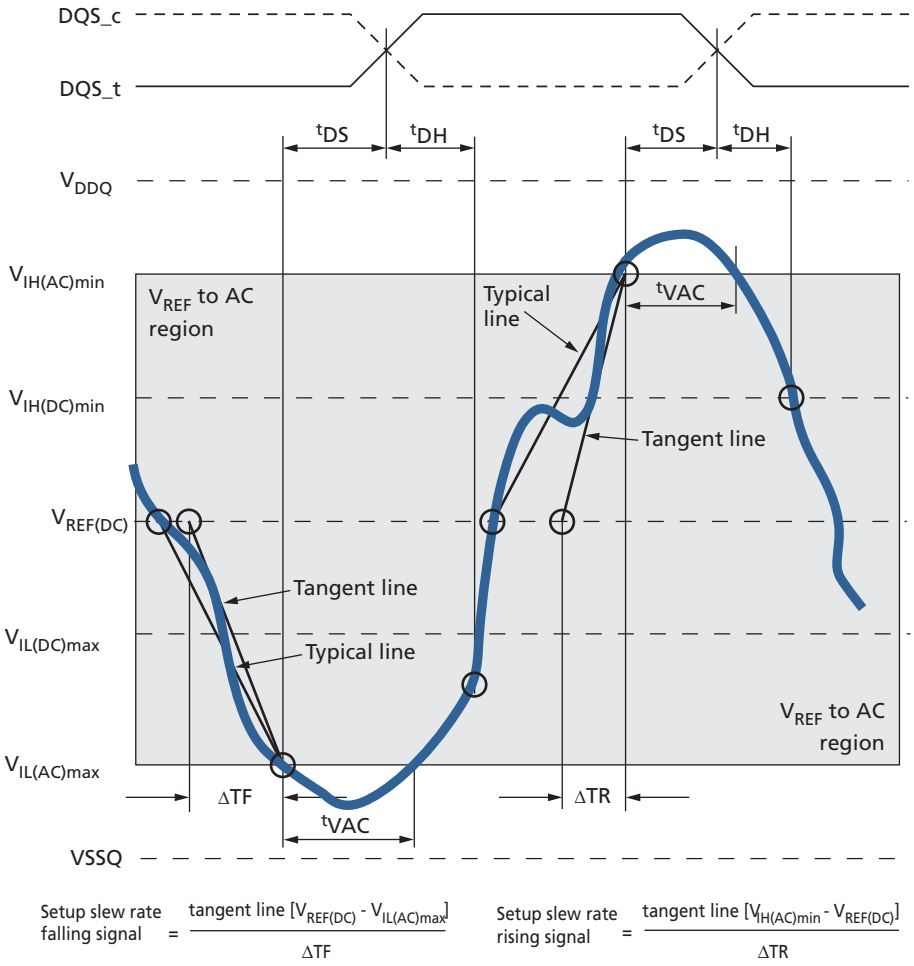
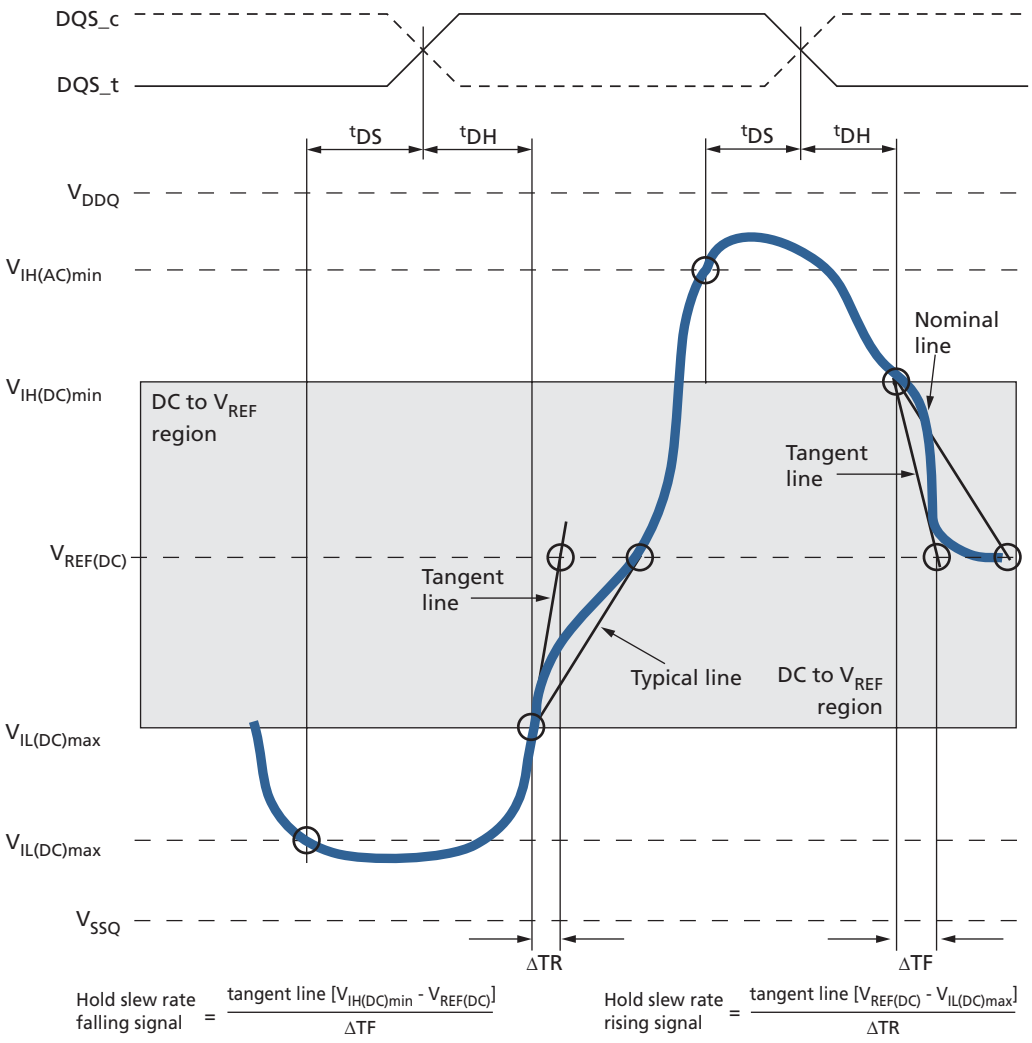


Figure 67: Tangent Line – ^{t}DH for DQ with Respect to Strobe



History

V0.1 – 9/28

- Initial release